



MAINTENANCE

TR-22 Television Tape Recorder

VIDEO AND FM SYSTEMS



RADIO CORPORATION OF AMERICA

IB-31621-1

BROADCAST AND TELEVISION EQUIPMENT

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TR-22 Television Tape Recorder

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GENERAL DESCRIPTION

INTRODUCTION

This instruction book covers two major systems of the TR-22; the Video System and the Monochrome Automatic Timing Corrector System (ATC).

The function of the Video System is to convert the incoming composite video signal to a frequency modulated signal for recording on tape and in playback mode to restore the tape FM to its original format. The function of the Monochrome Automatic Timing Corrector System is to eliminate line-by-line timing errors in the video output of a television tape recorder during playback mode. If uncorrected, these errors appear in the picture as geometric distortion and jitter. ATC does not replace the circuits which normally affect picture geometry but removes imperfections remaining after these circuits have performed their functions. The following paragraphs present a summary of the video processes performed by this equipment.

VIDEO RECORDING PROCESS

In the record mode (see figure 1) the incoming video signal is amplified, pre-emphasized, and converted to a double sideband fm signal extending from 1 mc to 10 mc. This signal is applied simultaneously to four individual recording amplifier channels, and then, through transfer relay contacts and slip rings, to the four video heads in the headwheel. The heads act as vestigial sideband filters so that the signal actually recorded extends from 1 to 7 mc. Each of the four channels contain an adjustable delay line and a level control. The delay lines permit electrical correction of timing errors resulting from lack of quadrature, or spacing of the video heads exactly 90 degrees apart on the headwheel. The level controls permit individual adjustment of the current supplied to each head so that the tape is just saturated.

A multi-position switch is provided to permit selecting the desired fm standards for color, monochrome, or special applications. As shown in figure 1 this switch simultaneously selects carrier frequency, deviation, pre-emphasis and post-emphasis and crystal reference circuits for checking carrier frequency and deviation. A clamp circuit in the modulator clamps the video input so that the modulator output is at the carrier frequency when the incoming video signal is

at the tip of horizontal sync. The maximum deviation from this sync tip frequency or carrier is determined by the amplitude of the video signal at the white peaks.

To permit monitoring during recording, the modulator output is fed to the playback system where it is subjected to limiting, demodulation, deemphasis, amplification, and signal processing. The processed video signal is fed to the selector switches for the CRO and picture monitor.

A selector switch is provided to permit making rf copies of tapes being played back on another machine. When this switch is in the RF COPY position the modulator is disconnected and the incoming rf is fed to the four record amplified channels. An rf copy playback circuit is also provided.

VIDEO PLAYBACK PROCESS

(Video Path)

In the playback mode (see figure 1) the tracks are read sequentially by the four video heads and the fm signals are fed through the slip rings and transfer relay contacts to four fm amplifier channels. Each channel has an adjustable delay line for correction of quadrature errors, and gain and equalization controls to compensate for variations in response of the individual heads. The four fm signals are then reassembled into a continuous signal by an electronic switcher. An overlap of about three TV lines exists between the end of each track and the start of the next track. The overlap is eliminated by performing the switching operation during the first horizontal sync period in the overlap interval.

The continuous fm signal is then equalized, limited and demodulated, and the resulting video signal amplified, de-emphasized and processed. The video signal is then passed through a 2.5 microsecond delay line to the monochrome ATC circuit, where time base stability is restored to eliminate geometric distortion and jitter. If monochrome ATC is not desired, a switch permits bypassing the circuit by relays to feed the video control circuits from another demodulator output. From the monochrome ATC circuit the video signal passes to the video control section and then to the video output amplifiers.

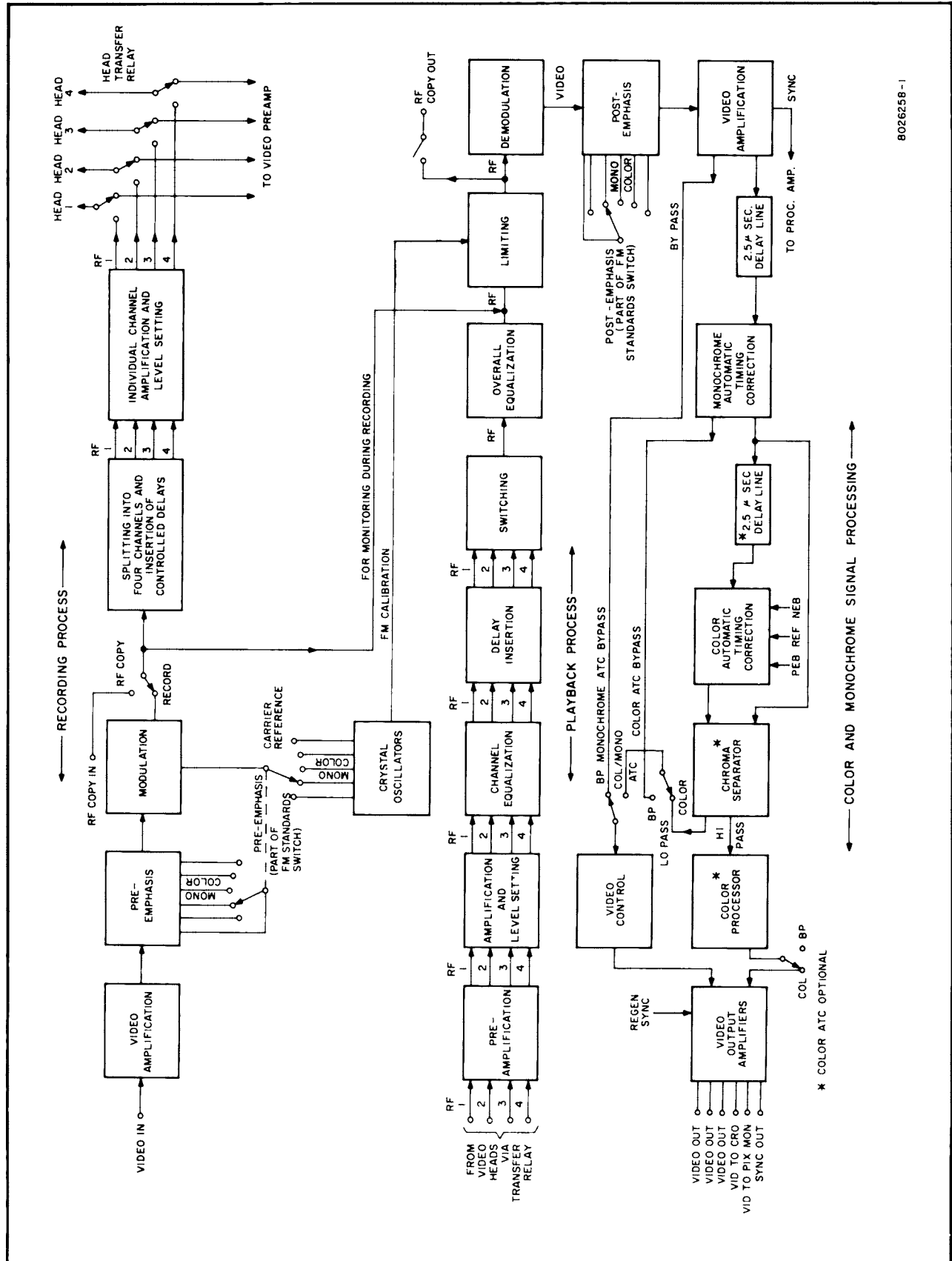


Figure 1—Block Diagram showing Video Recording and Playback Processes

If the machine contains color ATC, then the video signal passes from the monochrome ATC through a second 2.5 microsecond delay line to the color ATC section. The signal is then fed to the chroma separator which separates the low frequency and the high frequency (chroma) components of the color ATC video signal so that they may be independently processed before being recombined. The separated high frequency signal is fed to special processing circuitry, while the low frequency signal is fed to the monochrome processing circuits via the monochrome ATC reference module and the bypass relays. The color processor circuit performs two general functions; it generates the positive error signal and negative error signal potentials, and clamps the blanking interval of the chroma signal from the chroma separator so that

regenerated sync and regenerated burst may be inserted. From here the color video signal passes to the video amplifiers which provide isolated outputs to the outgoing lines, CRO, and picture monitor.

A selector switch is provided to permit using the recorder as the master (playback) machine for making rf copies of pre-recorded tapes. When this switch is in the RF COPY position it feeds the rf signal originating on the tape being played back, after limiting and amplification, to the rf copy output jack, which is connected to the rf copy input of the slave (recording) machine.

Table 1 is a listing of the modules used in the Video and FM Systems.

TABLE 1. LIST OF MODULES

<i>No.</i>	<i>Description</i>	<i>No.</i>	<i>Description</i>
103	Video Input	223A	ATC Delay
116A	Video Preamplifier	225	ATC Error
131B	Video Control	226B	ATC Reference
132	FM Equalizer	227B	Horizontal AFC
203B	Demodulator	228A	Vertical Advance
205A	FM Standards	230B	Sync Logic
207B-S	Modulator	233B	Video Output
211A-214A	Record Amplifier	302A	FM Reference
215A-218A	Playback Amplifier	303A	Demodulator Output
		318B	FM Switcher

VIDEO SYSTEM

DESCRIPTION

To simplify the description, the video system will be divided into two subsystems, (1) video/FM, and (2) signal processing. The first part of the description will include all but the five modules shown in the signal processing group. The second part of the description will be confined to the latter. Figure 2 is a functional block diagram of the Video System.

VIDEO/FM SUBSYSTEM

(Refer to the video/FM subsystem block diagram, figure 3.)

RECORD

Composite video is applied to the Video Input (module 103). Here the level is set and the video signal is distributed to four outputs. Two go to the monitors, picture and CRO; one is a spare and the remaining output goes to the FM Standards (module 205A). A sync separator is included on the Video Input module which strips sync from the incoming video and feeds it to the Modulator (module 207B-S).

In the FM Standards module the recording standard, monochrome or color, is selected and the proper

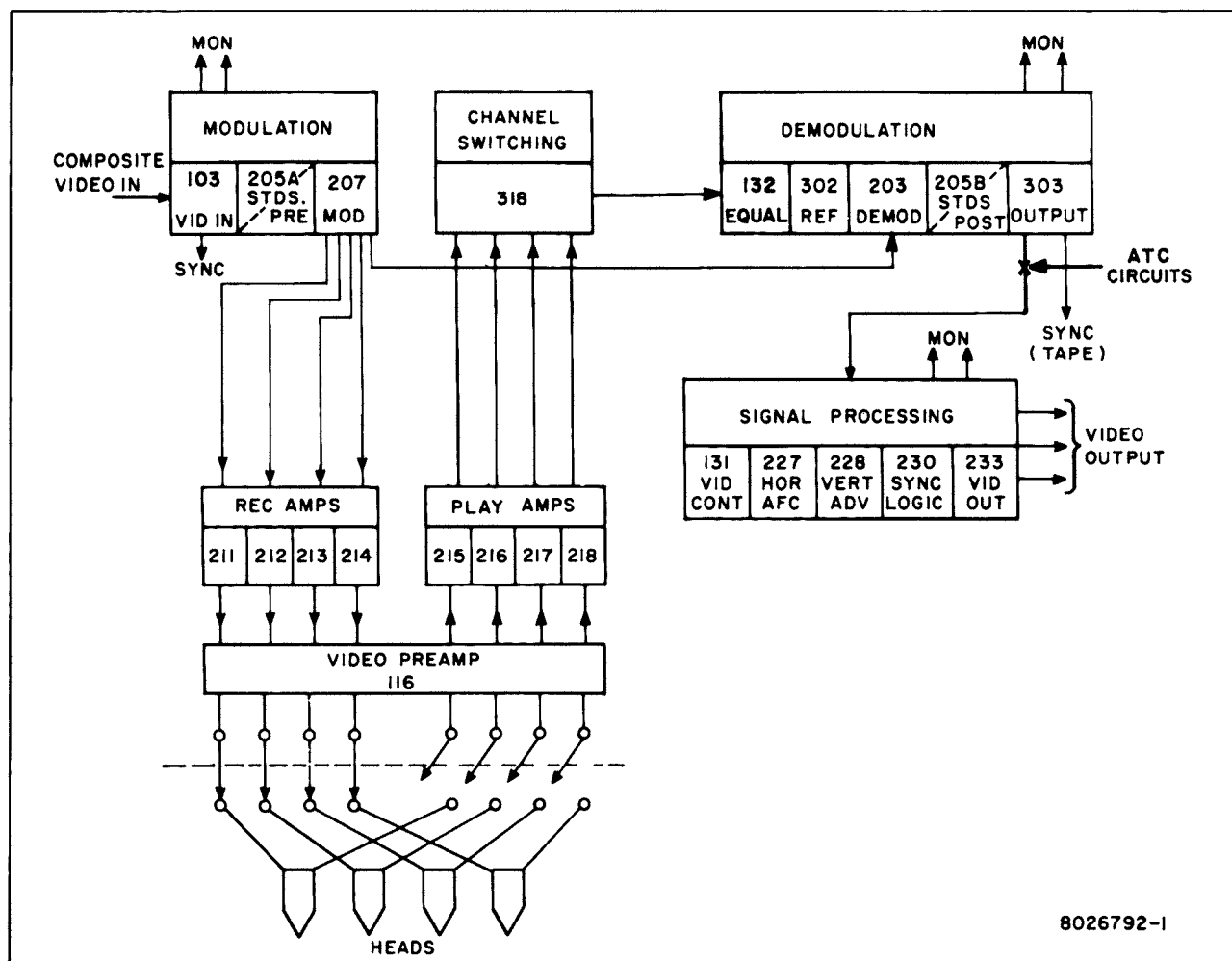


Figure 2—Simplified Video Functional, TR-22 TV Tape Recorder

amount of pre-emphasis is added to the signal. This module together with the Modulator (module 207B-S) establishes the deviation of the frequency modulated output of the latter.

The pre-emphasized video is fed to the Modulator and clamped at sync tip level. Video is converted to a frequency modulated signal, the deviation of which is a function of the amplitude of the video signal. Switching facilities are provided on the Modulator to enable RF copies to be made. In RF Copy mode, the oscillator circuits of the Modulator are disabled and the output of another recorder can be fed through the Modulator's amplifier circuits and subsequently be re-recorded.

From the Modulator the signal goes simultaneously to the four Record Amplifier (modules 211A, 212A, 213A, 214A) whereby the magnitude of the signal

currents of each channel is increased to a level suitable for driving the magnetic heads. A level control on each module permits optimum adjustment of the signal current of each channel. Each circuit contains an adjustable delay line to compensate for errors in the mechanical displacement of the magnetic heads from exactly 90 degrees around the circumference of the headwheel.

The output of the Record Amplifiers is coupled through the head transfer relay on the Video Preamplifier (module 116A) to the slip rings on the headwheel. A metering and an indicator current circuit is included on this module. The metering circuit enables the record current of each head to be evaluated on the multimeter. The indicator circuit provides a visual warning if one or more head currents are missing by causing the HD-I. (head current) indicator lamp to light.

PLAYBACK

In the Playback Amplifiers are playback delay circuits. Each module has a delay amplifier circuit to which the outputs of the Playback Amplifier is fed. The delay circuits contain adjustable delay lines which serve the same purpose as those on the Record Amplifier modules, i.e., to compensate for head quadrature error.

signal during the head to tape transfer. From the FM Equalizer the signal goes to the Demodulator (module 203B). Here it passes through several stages of limiting where symmetrical clipping of the positive and negative peaks takes place. Switching circuits at the input to this module allow the FM reference frequencies from module 302A, representing sync tip and peak white regions, to be injected into the signal before limiting. From the Limiter section the signal goes to the Demodulator section.

The Demodulator detects the video information in the FM signal. The resulting output is a signal that is a replica of the original video modulating signal. From the Demodulator the signal goes to the post-emphasis section of the FM Standards module. Here post-emphasis is introduced so that the video components are restored to the same relative level they were before pre-emphasis. The output then goes to the Demodulator Output (module 303A).

The Demodulator Output module is basically a video distribution amplifier supplying video to four outputs. Included on this module are a sync separator circuit and a sync sensing circuit. The principal video output goes to the Video Control (module 131B) which is part of the Signal Processing subsystem. One

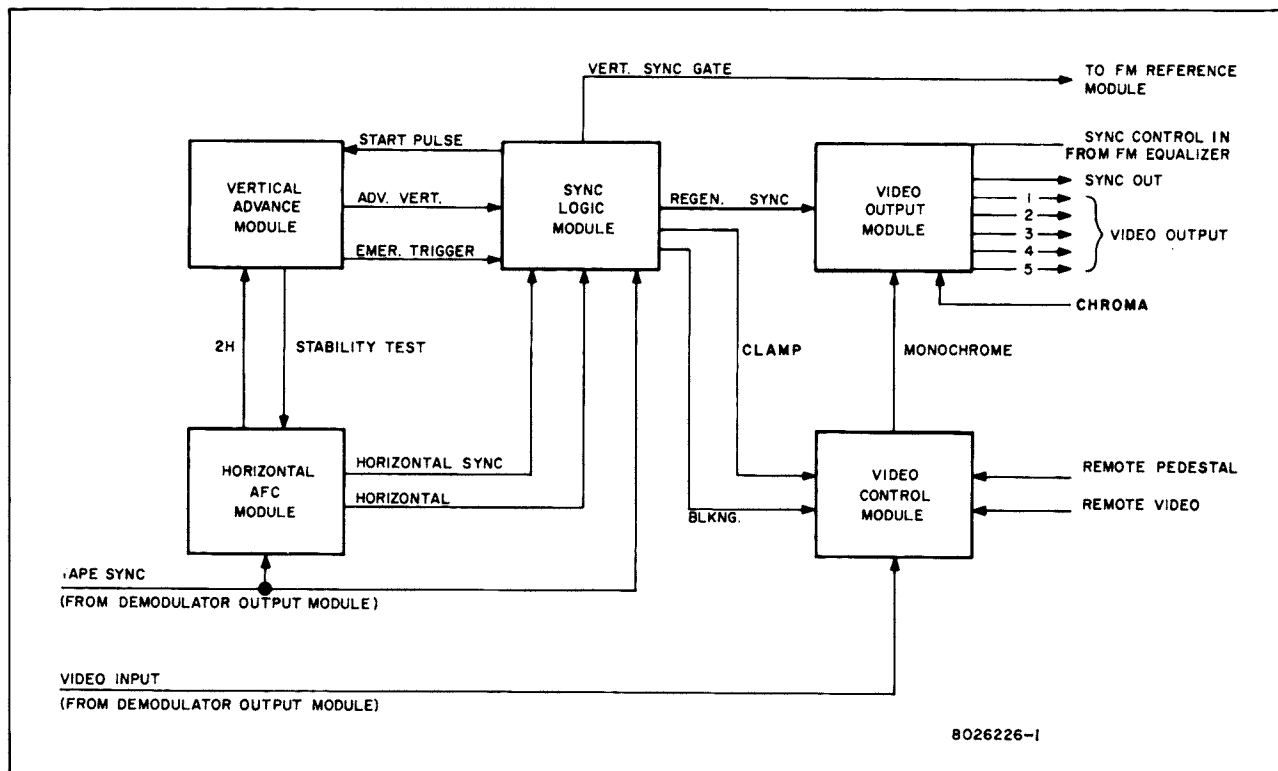


Figure 4—Block Diagram, Signal Processing Subsystem

output is a spare and of the remaining two, one goes to the CRO monitor and the other goes to the picture monitor. The sync separator furnishes sync to the Horizontal AFC (module 227B) and to the Tape Sync Processor (module 317). The former is also part of the Signal Processing Subsystem. The sync sensing circuit supplies a control signal to the Guide Servo (module 221) that allows the guide servo control to be operated automatically, as long as sync is present. The sync separator also feeds sync to ATC ERROR (module 225). Refer to discussion on ATC and diagrams in IB-31616-4.

INTERNATIONAL STANDARDS

The Demodulator and the FM Standards modules used in the TR-22 also operate on international standards.

SIGNAL PROCESSING SUBSYSTEM

The function of the monochrome signal processing subsystem is to restore all components of the video signal to insure that the output signal is a standard video signal suitable for transmission. The video signal is clamped to set the proper dc level, new blanking is added, present sync is removed and new

added. When the video signal enters the processing modules the sync pulse may be deformed with noise spikes and switching transients during the blanking interval. The signal processing subsystem provides a video output signal with a clean and adjustable black level and a clean horizontal sync interval. The processing includes complete regeneration of horizontal sync, horizontal and vertical blanking, and reinsertion of the vertical interval. The clean horizontal interval eliminates misclamping in stabilizing and transmitter amplifiers, which tends to occur due to the noise in the area below black level.

As shown in the block diagram, figure 4, the processing subsystem consists of five modules.

The three pulse-forming modules, Horizontal AFC, Vertical Advance, and Sync Logic, form a sync timing and regeneration system. These three modules are closely interlinked functionally and physically to produce blanking, gated horizontal sync, and regenerated sync. The blanking pulses needed for both monochrome and color tape recording systems must be regenerated from the sync pulse. The remaining two modules handle the video component. It is in the Video Output module that all signal elements are combined to form the new outgoing composite video signal.

The Horizontal AFC module regenerates blanking and horizontal sync, both of which are supplied to the Sync Logic module. The Horizontal AFC module generates a 31.5 KC square wave. This signal is used to automatically control the phase and frequency of the new 15.75 KC signal with respect to tape sync reference. The 31.5 KC square wave is also used to drive the Vertical Advance module.

The Vertical Advance module generates a 3.5H pulse and an emergency trigger pulse. The 3.5H pulse is used as a trigger in determining the leading edge of vertical blanking, which is generated in the Sync Logic module. The emergency trigger pulse insures continuation of precise timing of the vertical blanking interval, should there be an interruption in the normal 3.5H trigger action.

The video signal from the Demodulator Output (module 303A) is applied to the Video Control module. Here it is amplified to a level suitable for stable clamping. Blanking is added and the video signal is then fed to the Video Output module. A means for remotely controlling the level of video is provided on the Video Control module.

The Video Output module combines the video sig-

nal and the regenerated sync to form the composite video signal. This signal is available at five separate outputs. An output for regenerated sync is also provided.

Most of the circuitry in the three pulse-forming modules consist of simple time constant changes in order to obtain the correct pulse widths needed for the different TV standards. The Vertical Advance module contains the circuitry necessary to change the timing of the 3.5H pulse so that it is compatible with 405- and 625-line standards. This circuitry includes an additional transistor stage, a miscount amplifier, for driving the first counter when on 625-line standards. The switch used in selecting the different TV standards is now located on this module. In the Horizontal AFC module, switching changes the time constant components in the 2H master oscillator and the horizontal square wave multivibrator circuits, two transistors are used as a starting circuit for the 2H oscillator.

The descriptions of the pulse-forming modules are based on the 525-line system. Where required additional information, simplified schematic diagrams and waveforms are included to cover other standards.

MODULE CIRCUIT DESCRIPTIONS

Each module is treated separately in the following circuit descriptions. Block diagrams and simplified schematics accompany each description. A series of waveforms, keyed to various points on the simplified schematics by letters, is included for each module.

VIDEO INPUT (Module 103)

The Video Input module (see block diagram, figure 5) distributes the composite video input to four video lines in the TR-22 and supplies sync that has been stripped from the incoming video to the Modulator (module 207B-S) and the Reference Generator (module 312).

The Video Input module consists of an input stage with gain control, a feedback pair, four series-output amplifiers each driving a terminated line, and a sync separator circuit. A 15-volt regulator stage is also included to supply the necessary 15-volt dc operating voltages.

The output of one amplifier drives the line to the FM Standards (module 205) and supplies composite video to the input of the sync separator circuit. This

stage also feeds video to the parallel-connected inputs of the other three video output amplifiers. Two of the three remaining output amplifiers drive lines going to the picture monitor and the CRO; the output of the fourth output amplifier drives the spare video output line.

The composite video input is applied to pins 17 or 18 of the Video Input module (see figure 6) via one of the two coaxial input jacks, 12J1 or 12J2 on the TR-22. These jacks are connected together at a point within the Video Input module so that the input signal can be looped through the TR-22 or terminated at the unused jack. The first two stages, Q15, Q1, both emitter followers, constitute the input circuit which is designed to accommodate high voltage tube equipment.

The signal is coupled through C15 to the base of Q15 and is then fed directly from the emitter to the base of Q1. The feedback circuit between Q1 and Q15 presents a high input resistance that makes possible the use of a high voltage input coupling capacitor (C15) of reasonable size without sacrificing low fre-

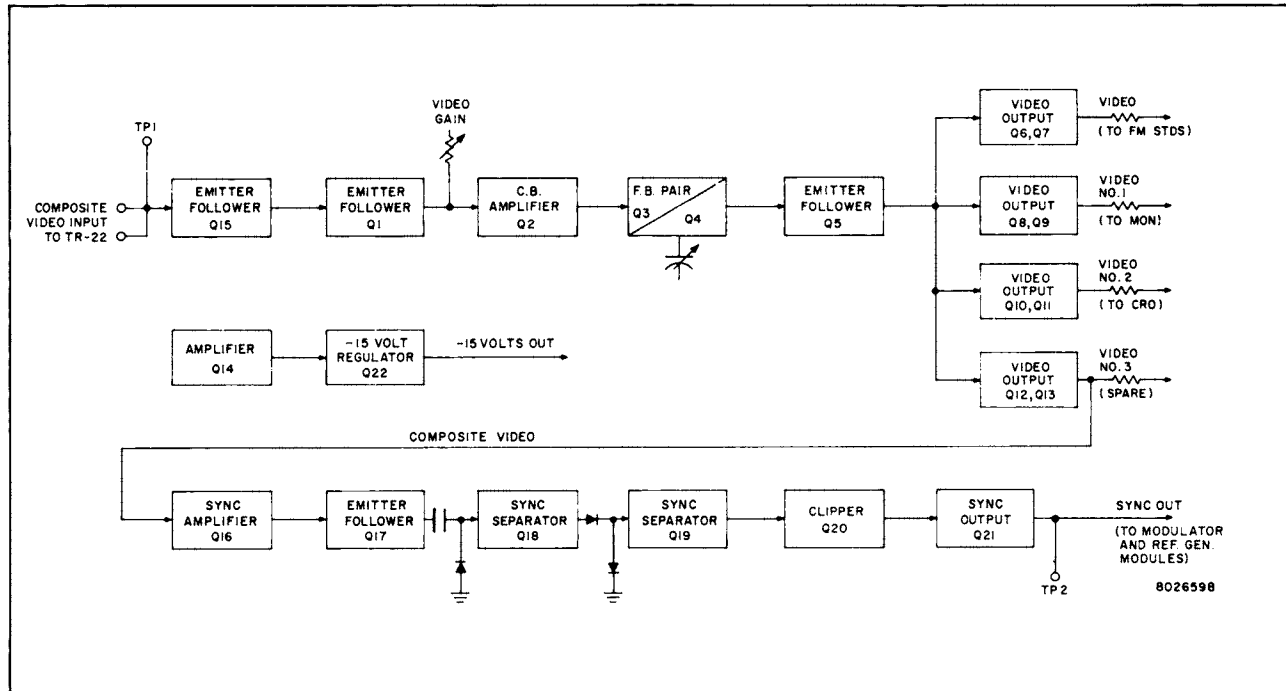


Figure 5—Block Diagram, Video Input Module

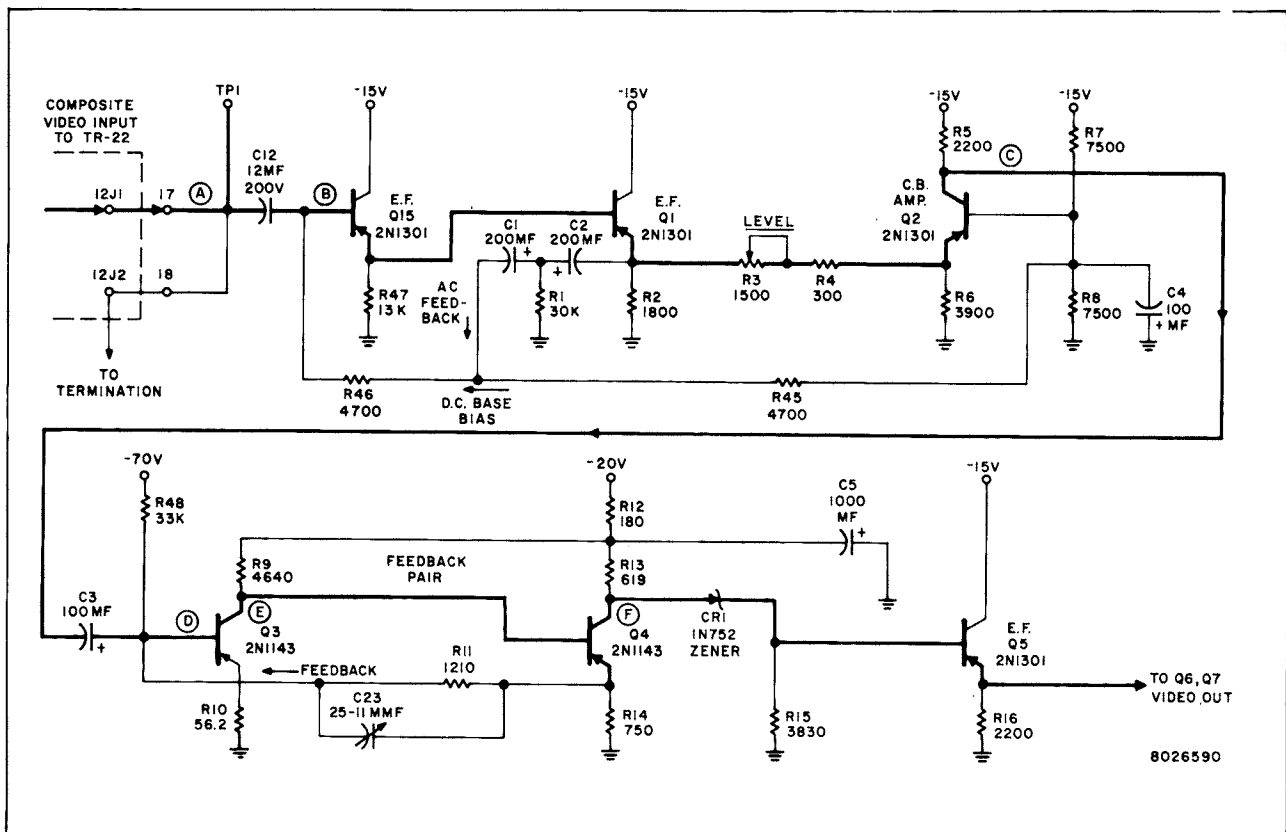


Figure 6—Video Input, Gain Control and Feedback Pair Circuits

quency performance. The signal fed back from the emitter of Q1 through C2 and C1 to R46 is in phase with, and almost equal in amplitude to, the input on the base of Q15. Because the signal voltage on each end of R46 is nearly identical, very little current flows through the resistor. Therefore the apparent input resistance is very high, being over ten times the actual resistance of R46. Resistor R45 provides isolation and in conjunction with R46 forms a voltage divider supplying dc bias to Q15. The output from the emitter of Q1 is coupled through R3, the video gain potentiometer, and R4 to the emitter of Q2. The amplitude of the signal current applied to Q2 is determined by the series resistance presented by R3.

The output from the collector of Q2 is coupled through C3 to the base of Q3, the input half of a feedback pair (see figure 7). From the collector of Q3, the signal is fed directly to the base of Q4, the output half of the feedback amplifier. The feedback signal, which is out-of-phase with the input, is taken off the emitter of Q4 and fed through variable capacitor C23 and R11 to the base of Q3.

Variable capacitor C23 is a frequency response control and does not require adjustment during normal operation or routine maintenance. It is provided to

compensate for differences in transistors in case of replacement, and is adjusted to obtain a gradual high frequency roll-off in the region above 5 mc.

The signal at the collector of Q4 is directly coupled through Zener diode CR1 to the base of Q5. Diode CR1 furnished proper bias to Q5 without introducing signal loss. Resistor R15 biases CR1 to the correct operating current.

From the emitter of Q5, the signal is fed directly to the base of Q6, one half of the first video series output amplifier (see figure 8). The signal is taken off the collector of Q6 and coupled through C6 to the base of Q7, the other half of the amplifier. The signal polarities and amplitudes at Q6, Q7, where video output is obtained, are such that the voltage gain of the pair is unity and the output impedance very low. The signal is fed simultaneously to the remaining three output amplifiers (Q8, Q9; Q10, Q11; and Q12, Q13), the sync amplifier, Q10, and the FM Standards (module 205A). The line going to the latter is sending-end terminated in 75 ohms which is formed by the output impedance of Q6, Q7 in series with the 68 ohms of R23.

The remaining three series output amplifiers are identical to the first-mentioned amplifier, with each

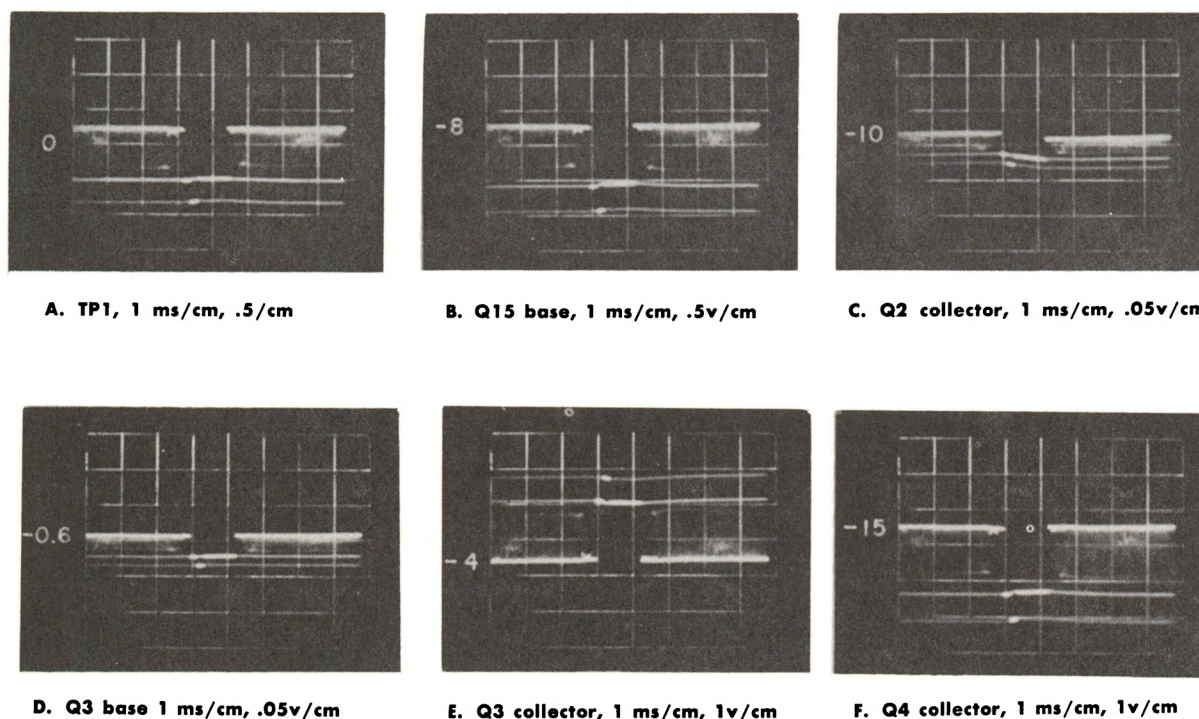


Figure 7—Typical Waveforms; Video Input, Gain Control and Feedback Pair Circuits

driving a separate terminated output line. Amplifier Q8, Q9 drives the line to the picture monitor, amplifier Q10, Q11 the line to the CRO, and amplifier Q12, Q13 goes to the spare video line.

The input to the sync separator section is a sync amplifier stage consisting of Q16, a common base amplifier, and Q17, an emitter follower (see figure 10). Video from the first video output amplifier, Q6, Q7, is coupled through C16 to the emitter of Q16. Here the signal is amplified so that at the output the signal is on the order of 9 volts. This signal appears on the base of Q17, which, being an emitter follower, minimizes the collector loading on Q16 and provides a low impedance source for the next circuit. The output of Q16 is fed through the bias and coupling network,

C18, L1, R53 and R54, to an emitter follower, Q18.

Diode CR2 in the base of Q18 acts as dc restorer by clamping the tips of sync. Before CR2 can conduct heavily, however, the sync tip must go .8 volt negative, to overcome the forward voltage drop across the diode. The effect of this, then, is to clamp the sync tip at $-.8$ volt. The signal on the base of Q18 goes from $-.8$ volt to some positive value, depending on the amplitude of the video signal. However, the signal on the emitter of Q18 in following the positive-going excursion cannot go beyond $+1.2$ volts, because of CR3 and CR4. At this level, $+1.2$ volts, the forward voltage drop across these two diodes is reached. The diodes then conduct, holding the emitter at $+1.2$ volts. The base signal continues in a positive direc-

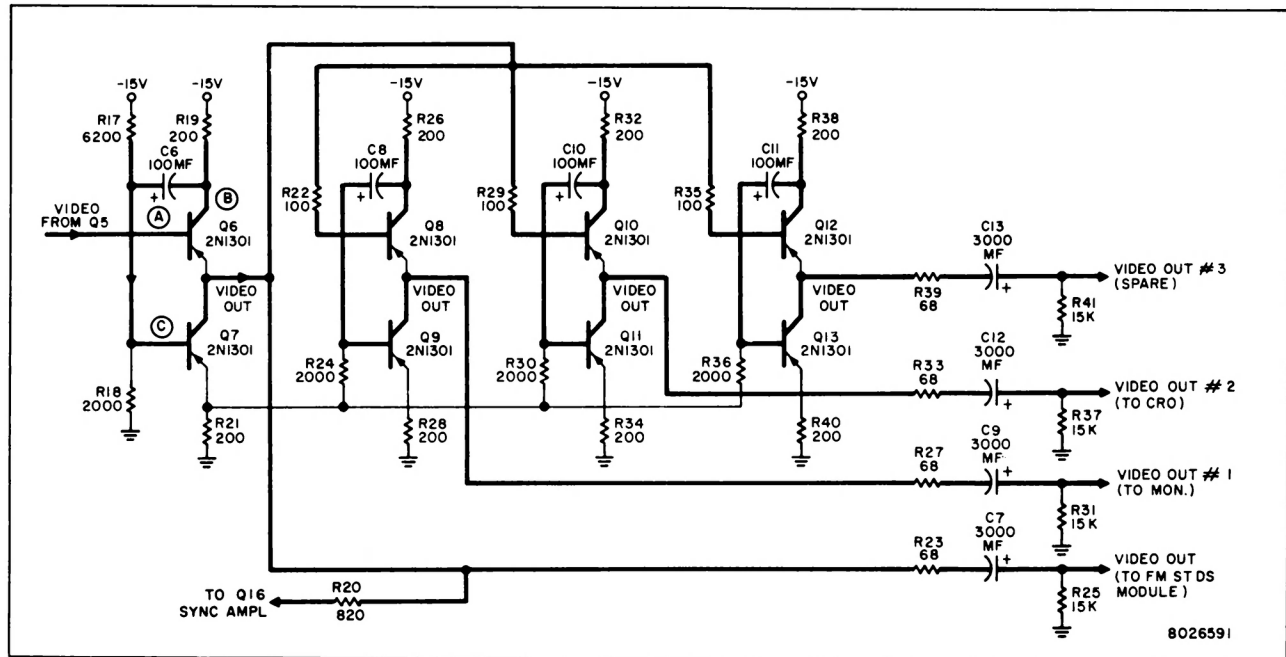


Figure 8—Video Output Amplifier Circuits

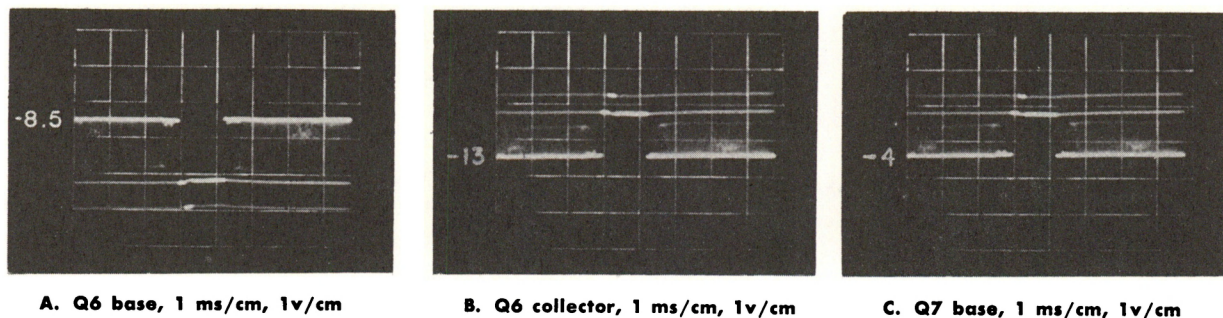


Figure 9—Typical Waveforms; Video Output Amplifier Circuits

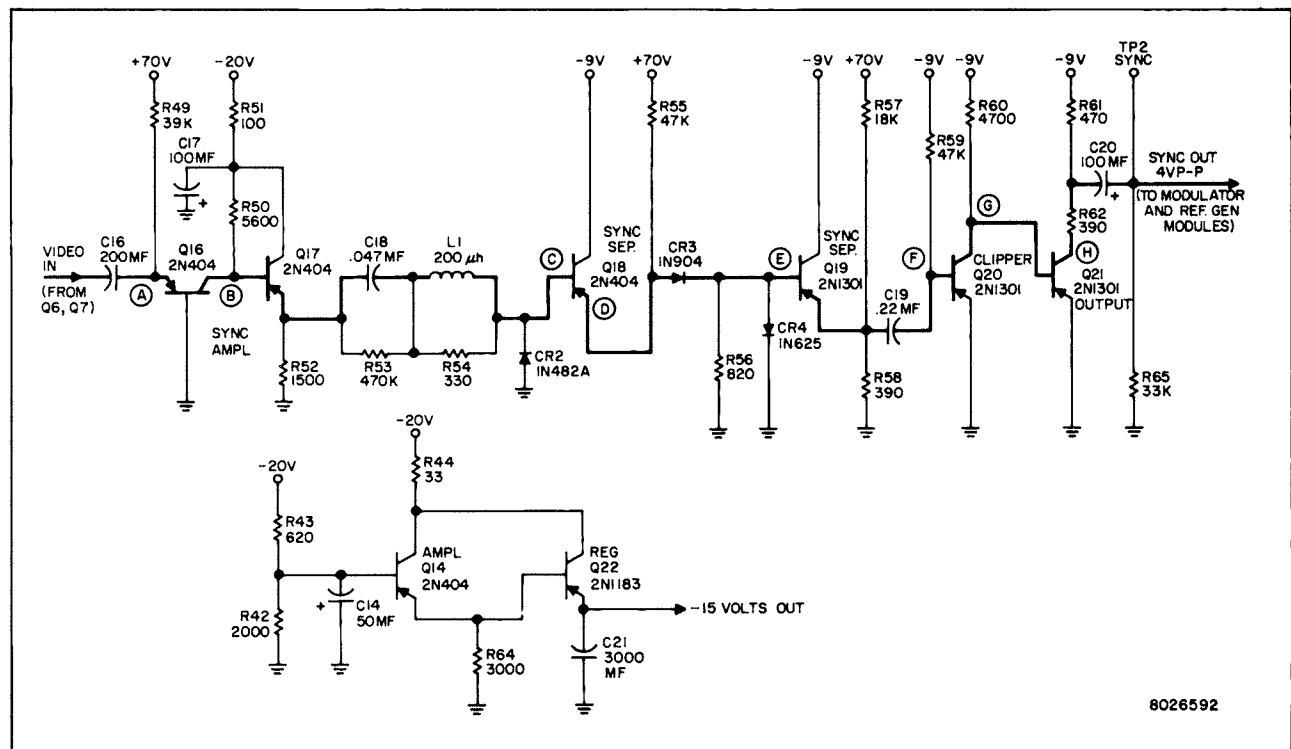


Figure 10—Sync Separator and -15 Volt Regulator Circuits

tion, cutting off Q18. The emitter excursion of Q18, therefore, follows the signal on its base only for a short interval beginning at the tip of sync. The rest of the signal, i.e., video, blanking, and the remainder of sync, is clipped due to Q18 being driven to cutoff and the shunting effect caused by the conduction of CR3 and CR4. Although sync at the emitter of Q18 extends from -0.6 volt to $+1.2$ volts, CR3 will not conduct the negative portion of this signal thus stripping off the part representing the region near the tip of the input sync signal. Only that portion of sync that extends from 0 to $+0.6$ volts appears across CR2; therefore, this is the amplitude range of the signal appearing on the base of Q19. The signal at this point represents only a small segment near the center of the input sync.

The output of Q19 is fed to the base of Q20 which, in cascade with Q21, forms the clipper and output stage. The level of the sync output from Q21 is 4 volts peak-to-peak. This signal is taken across R26, part of the collector load, and coupled through C20 to the unterminated sync output line which feeds the Modulator (module 207) and the Reference Generator (module 312).

The -15 volt dc operating voltage is furnished by the -15 volt regulator stage, which consists of

Q14 and Q22. The base of Q14 is biased to approximately -15 volts. This voltage is developed across R34 and R35 from the -20 volt supply. The emitter of Q14 is at nearly the same potential as the base and this voltage appears as the bias on the base of Q22. Since the base of Q22 is at -15 volts, the output voltage appearing on the emitter is virtually the same potential. Because Q22 exhibits the low output impedance of an emitter follower, the output voltage will remain constant regardless of load variations.

FM STANDARDS (Module 205A)

The FM Standards module provides pre-emphasis (high frequency boost) for the video signal being recorded and post-emphasis (high frequency roll-off) for the video signal during playback, on monochrome or color standards. This module together with the Modulator (module 207BS) establishes the deviation of the frequency modulated signal, and also, in conjunction with the FM Reference (module 302A) selects crystal controlled reference frequencies for calibration purposes. Selection of the appropriate standard is made by means of a five-position rotary switch which is controlled from the front panel of the module. Although all of the switch positions are in use, some selections are duplicated; therefore the same function appears on more than one position. For

International Standards, internal switching automatically changes equalization, deviation and reference crystals in accordance with line standards selected at the Vertical Advance (module 228A).

The post-emphasis curves for monochrome and color standards are shown in figures 12 and 13, respectively.

As shown in the block diagram, figure 14, the pre-emphasis and post-emphasis stages are independent of each other, although the circuitry of both is similar. A different attenuator network is employed to establish the pre-emphasis and post-emphasis frequency response characteristic for each monochrome or color standard.

STANDARD SELECTOR SWITCH S1

A brief functional description of each of the five

sections of S1 is given below.

Section A is used to select the network appropriate to the standard chosen for recording the video signal.

Section B closes the circuit of the appropriate standards lamp along the row of mode indicators above the PLAY control panel.

Section C provides a -26V control signal to select appropriate reference crystals in FM Reference (module 302A) for use in establishing frequency deviation between the sync tip and peak white components of the signal.

Section D supplies the dc control voltage to the Modulator (module 207B-S) that is used to determine the approximate level of the sync tip frequency.

Section E is used to select the network appropriate to the standard chosen for playback.

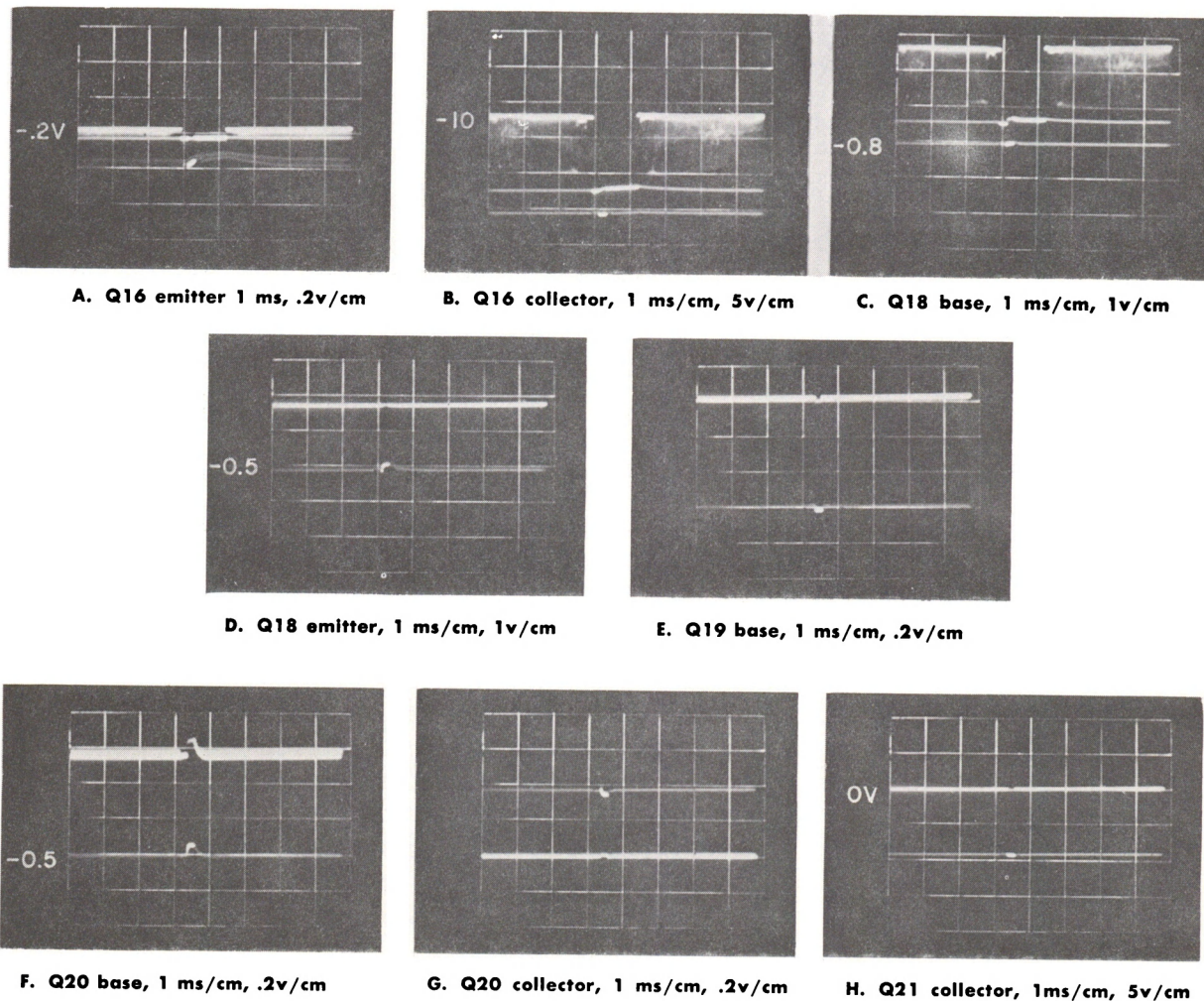


Figure 11—Typical Waveforms; Sync Separator Circuit

Major elements comprising the FM Standards video circuits are shown in the block diagram, (figure 14). The pre-emphasis section incorporates an emitter follower, Q1, to drive an equalizer network through TV Standards relay, K3. The network selected depends on the state of K3 and the position of FM STDS switch S1. The relay is controlled by the TV STANDARDS switch located on the front panel of Vertical Advance (module 228A), and S1 is set from the front panel of the FM Standards module. Thus, selection of a network depends both on the television standards (405/525 or 625/819) and on the FM standard (monochrome or color). The output of the equalizer is fed through an emitter follower isolation stage, Q6, then to a feedback amplifier, Q7, Q8, where signal level lost in the equalizer is recovered. Another emitter follower, Q10, provides a low impedance drive source for the coaxial line to the modulator video input. A nearly identical circuit configuration is used in the post-emphasis section.

When a standard is chosen, the FM Standards module video and control circuits perform the following functions:

1. Select correct high frequency boost for pre-emphasis required.
2. Set modulator video drive for correct peak-to-peak deviation.
3. Set Modulator sync tip frequency to preset value.
4. Select correct pair of FM Reference crystals.
5. Select correct high frequency roll-off for post-emphasis required to complement pre-emphasis.
6. Amplify video output of Demodulator to standard level.
7. Activate tally lights to indicate standard selected.

PRE-EMPHASIS SECTION

Video from the Video Input (module 103) is fed at a one volt level to a 75 ohm termination consisting of R11, R5 and DEVIATION control R5, as shown in schematic diagram, figure 15. The DEVIATION potentiometer is a screwdriver adjustment accessible from the front panel. It sets carrier swing, that is, FM deviation, by controlling the amplitude of the

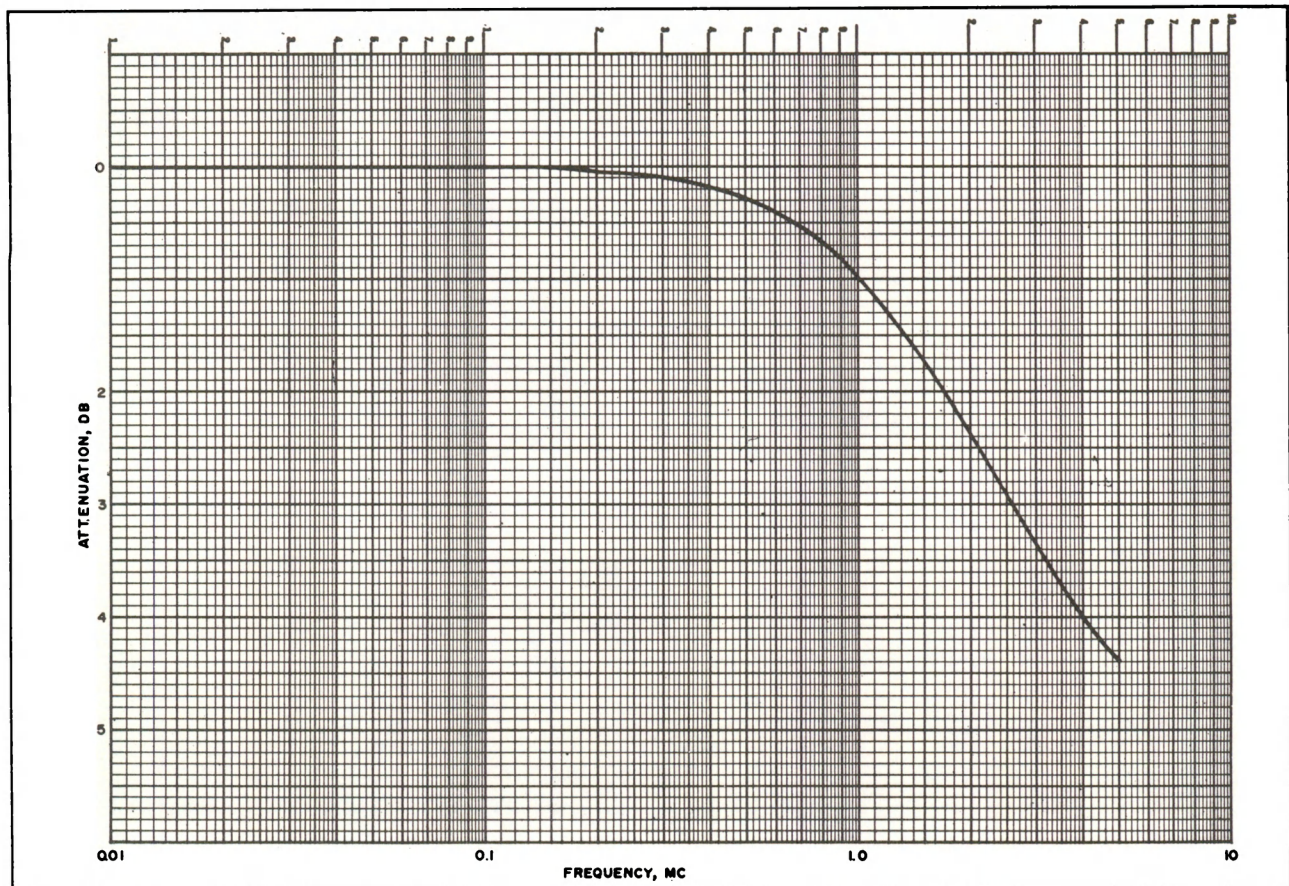


Figure 12—Post-emphasis Curve for Monochrome Standards

video drive to the Modulator. A d-c return for Q1 base current is provided by R11, and R4 in series with R5.

The pre-emphasis equalizer selected by K3 and S1K or S1L is driven by emitter follower Q1. The equalizer is simply a voltage divider consisting of R33 in series with an inductive impedance to ground. Output is taken from across the impedance, which has a magnitude proportional to frequency. Therefore at low frequencies, the transmission through the divider, from Q1 emitter to Q6 base, is low because of the shunting effect of the impedance. However, at higher

frequencies, the impedance increases, raising the transmission through the divider. The net effect is a high frequency boost. In addition to frequency-selective attenuation, each impedance introduces a nonselective loss, the amount of which depends upon the deviation for the standard selected. Thus, once deviation has been correctly set on any one standard, and a new standard is subsequently selected, modulator video drive will be modified by nonselective attenuation in accordance with new deviation requirements. Relative attenuation and frequency equalization for each standard are presented in Table 2.

TABLE 2. ATTENUATION AND EQUALIZATION LEVELS

<i>Function</i>	<i>Pre/Post Emphasis</i>	<i>Deviation MC</i>	<i>Relative Pre-Emphasis L. F. Gain, db</i>	<i>Relative Post-Emphasis L. F. Gain, db</i>
405/525 Mono	4 db @ 4 mc	2.52	0	0
525/819 Mono	4 db @ 4 mc	1.8	-2.9	+2.9
Color	9.7 db @ 4 mc	0.9	-8.94	+8.94

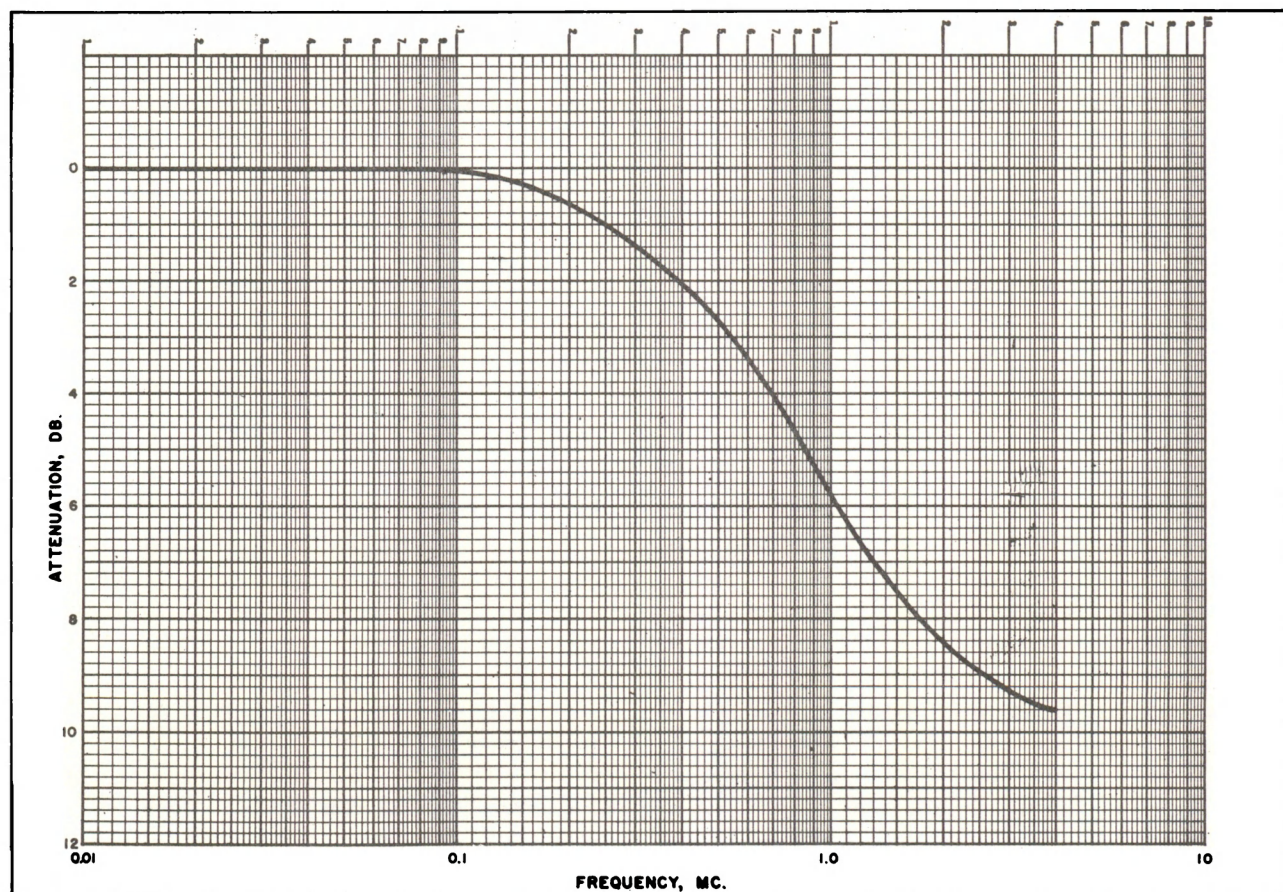


Figure 13—Post-emphasis Curve for Color Standards

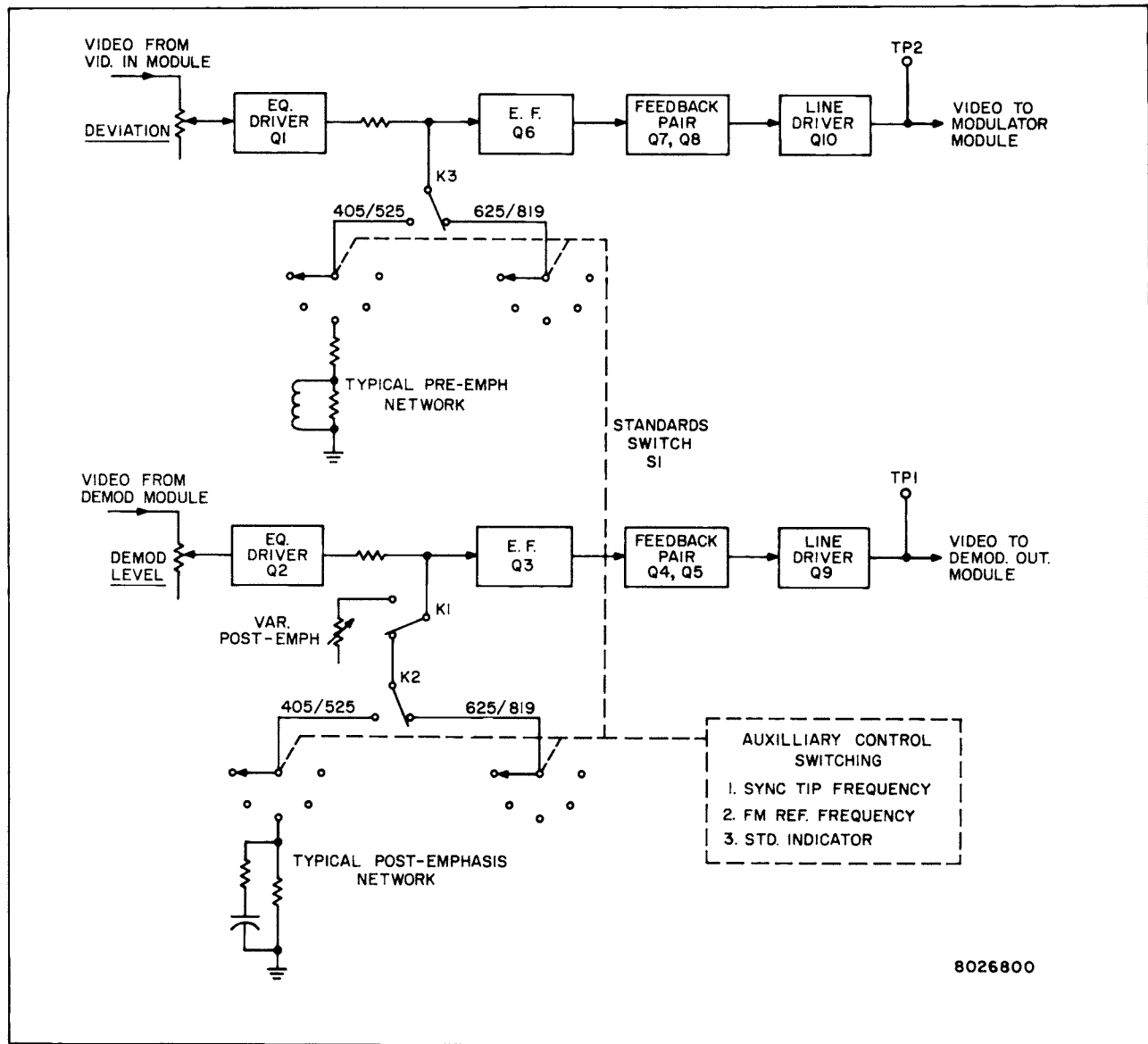
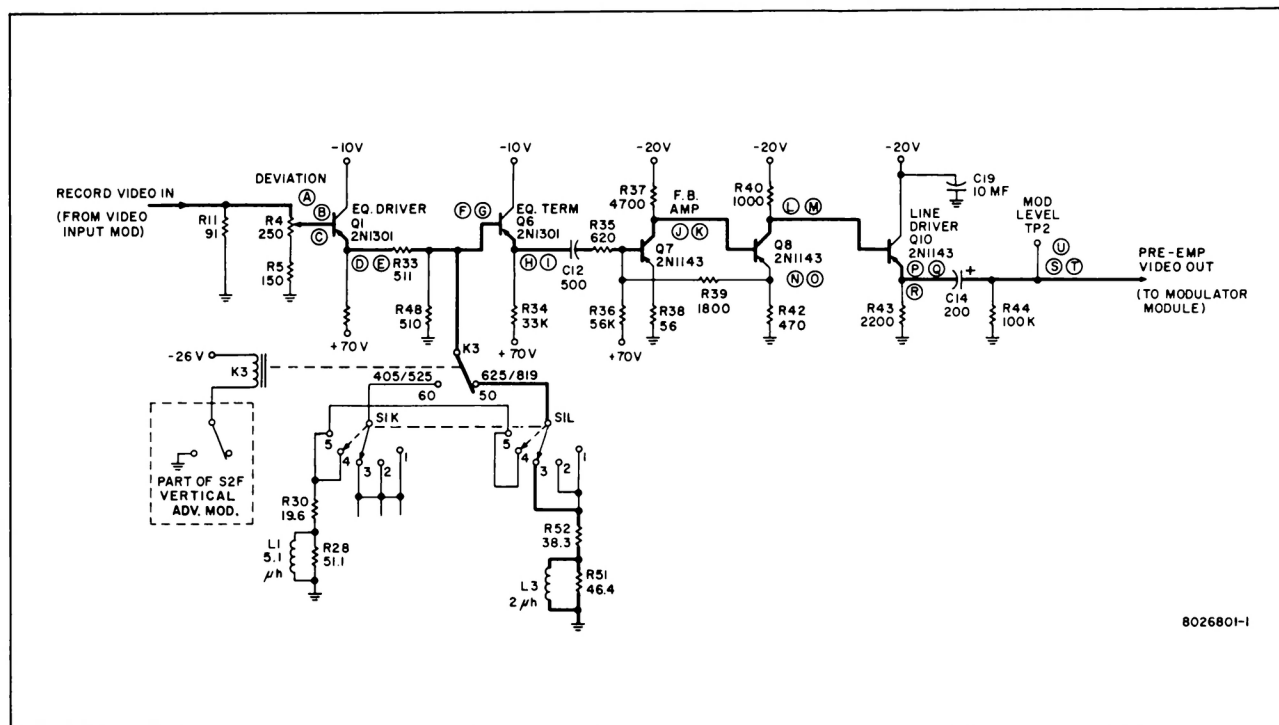


Figure 14—Block Diagram, FM Standards Module

All of the equalizer circuits connected to S1L are associated with 625/819 standards, while all networks connected to S1K are associated with 405/525 standards. Either section is selected by K3, which is shown in its unenergized state in figure 15. The return circuit of the coil in K3 is controlled by the TV STANDARDS switch in the Vertical Advance module so that it is ungrounded whenever 625 or 819 standards are selected. In this state the equalizer section selected by S1L is made functional. When 405 or 525 standards are selected, the relay return is grounded by the TV STANDARDS switch, energizing the relay coil, and causing the equalizer selected by S1K to be effective. Thus, the pre-emphasis ultimately depends on

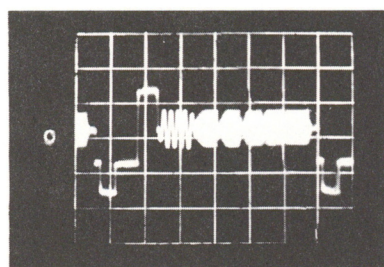
both the position of the FM STDS selector and the TV STANDARDS switches. Although the former switch has five positions, only two standards are available (STD MONO, and STD COLOR) therefore some switch positions provide duplicate functions.

Emitter follower Q6 minimizes capacitive loading on the equalizer and provides sufficient signal current to drive R35, the input terminating resistor of feedback pair Q7, Q8. This feedback amplifier is direct coupled to line driver Q10 for good low frequency response and to stabilize d-c conditions. Emitter follower Q10 minimizes loading of Q8 collector, and drives the unterminated output line at a 0.5 volt level.

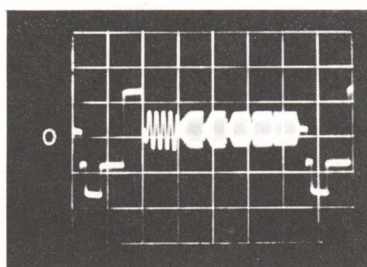


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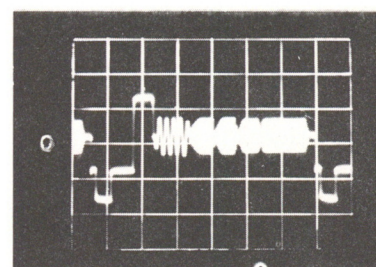
Figure 15—Equalization, Feedback Amplifier and Line Driver Circuits (Pre-emphasis Section)



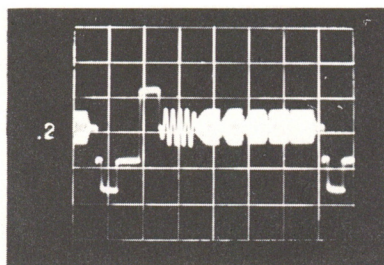
A. Q1 base, 10 μ s/cm, .2v/cm, mono, 525



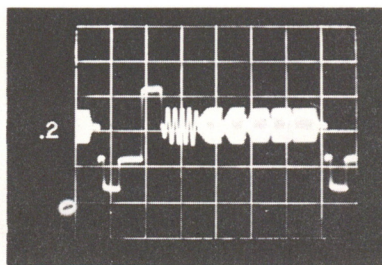
B. Q1 base, 10 μ s/cm, .2v/cm, mono, 625



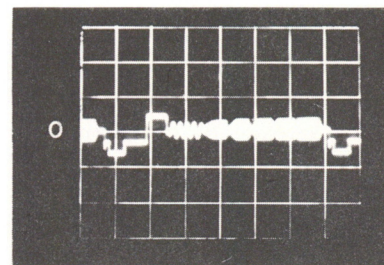
C. Q1 base, 10 μ s/cm, .2v/cm, color, 525



D. Q1 emitter, 10 μ s/cm, .2v/cm, mono, 525

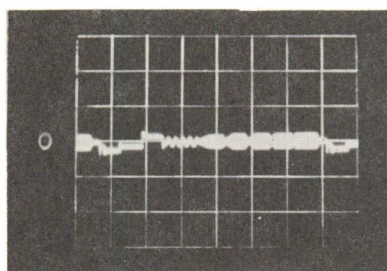


E. Q1 emitter, 10 μ s/cm, .2v/cm, color, 525

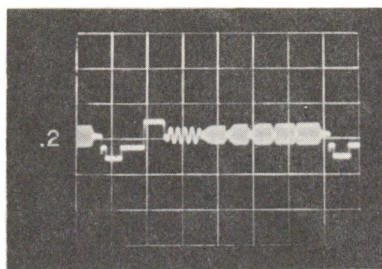


F. Q6 base, 10 μ s/cm, .05v/cm, mono, 525

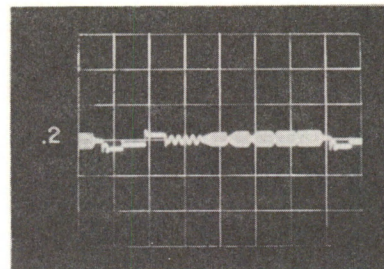
Figure 16—Typical Waveforms; Equalization, Feedback Amplifier and Line Driver Circuits (Pre-emphasis Section)



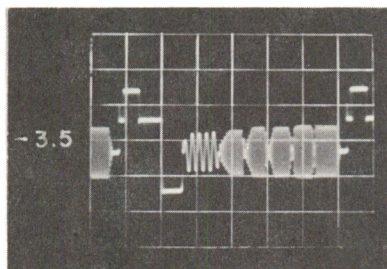
G. Q6 base, 10 $\mu\text{s}/\text{cm}$, .05v/cm



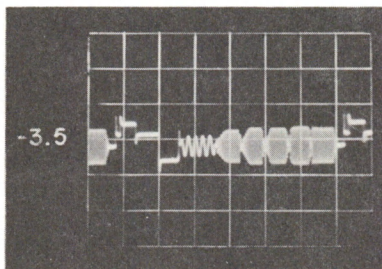
H. Q6 emitter, 10 $\mu\text{s}/\text{cm}$, .05v/cm, mono, 525



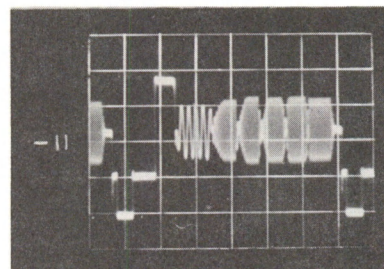
I. Q6 emitter, 10 $\mu\text{s}/\text{cm}$, .05v/cm, color, 525



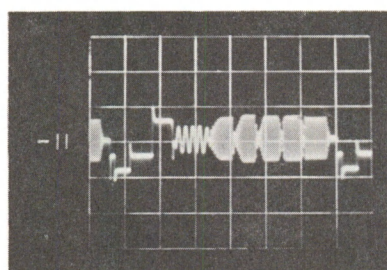
J. Q7 collector, 10 $\mu\text{s}/\text{cm}$, .05v/cm, mono, 525



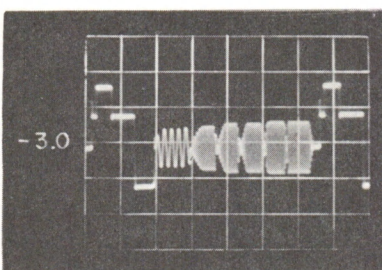
K. Q7 collector, 10 $\mu\text{s}/\text{cm}$, .05v/cm, color, 525



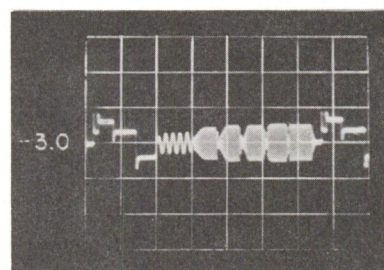
L. Q8 collector, 10 $\mu\text{s}/\text{cm}$, .01v/cm, mono, 525



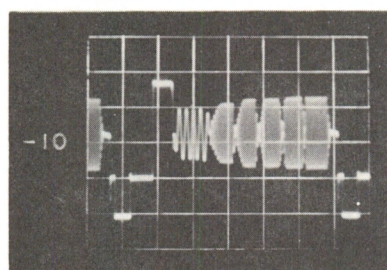
M. Q8 collector, 10 $\mu\text{s}/\text{cm}$, .01v/cm, color, 525



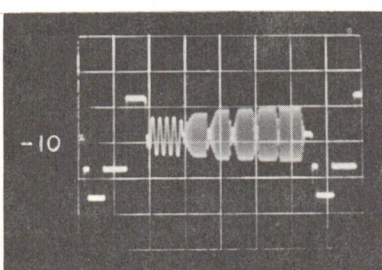
N. Q8 emitter, 10 $\mu\text{s}/\text{cm}$, .05v/cm, mono, 525



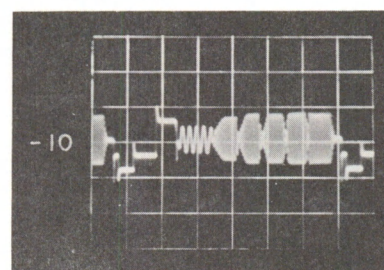
O. Q8 emitter, 10 $\mu\text{s}/\text{cm}$, .05v/cm, color, 525



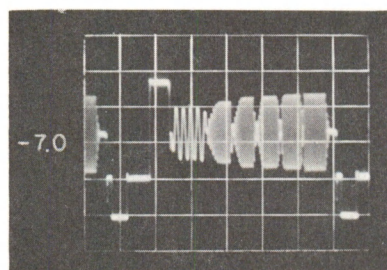
P. Q10 emitter, 10 $\mu\text{s}/\text{cm}$, .01v/cm, mono, 525



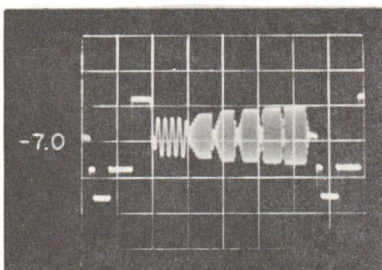
Q. Q10 emitter, 10 $\mu\text{s}/\text{cm}$, .01v/cm, mono, 625



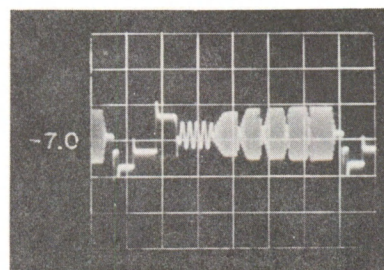
R. Q10 emitter, 10 $\mu\text{s}/\text{cm}$, .01v/cm, color, 525



S. TP2, 10 $\mu\text{s}/\text{cm}$, .1v/cm, mono, 525



T. TP2, 10 $\mu\text{s}/\text{cm}$, .1v/cm, mono, 625



U. TP2, 10 $\mu\text{s}/\text{cm}$, .1v/cm, color

Figure 16—Typical Waveforms; Equalization, Feedback Amplifier and Line Driver Circuits (Pre-emphasis Section) (Continued)

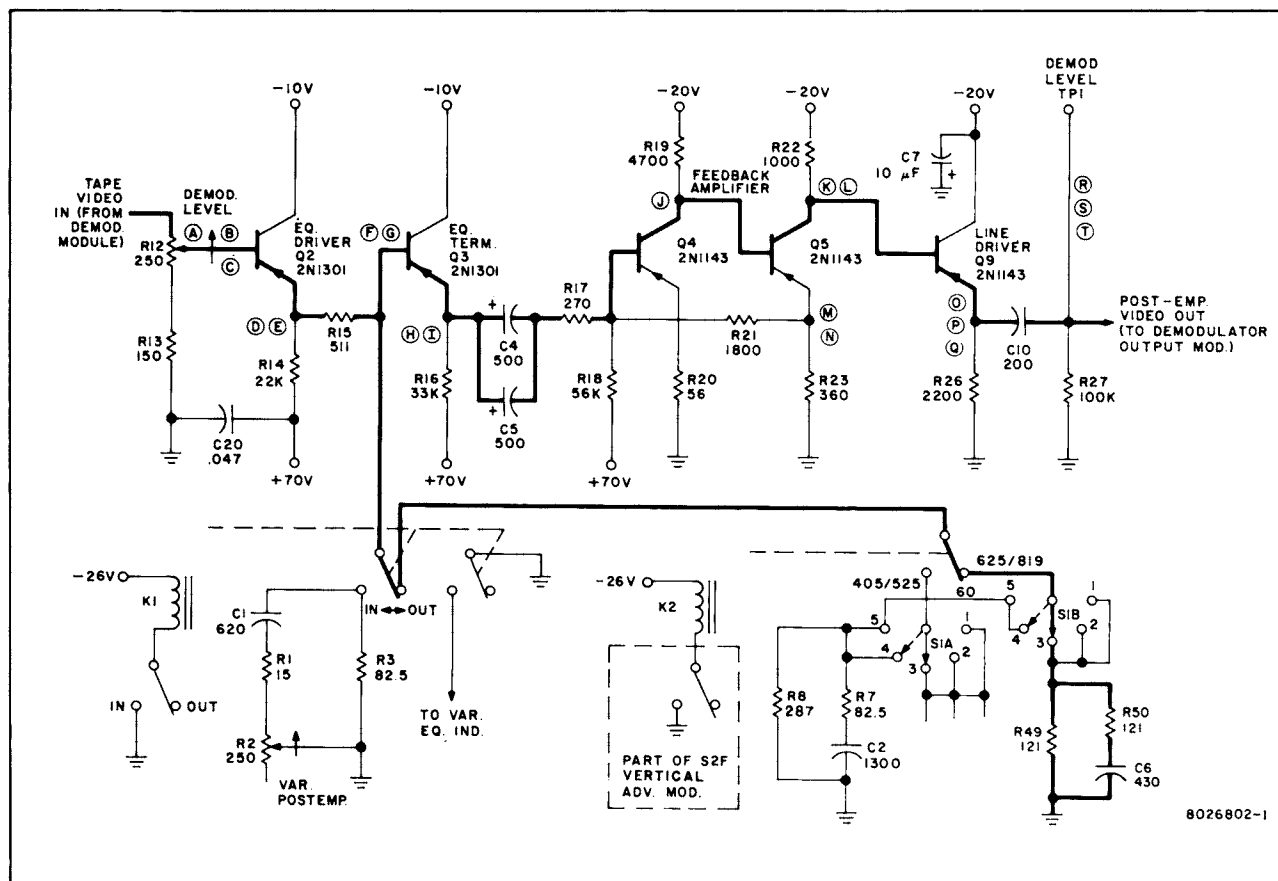


Figure 17—Equalization, Feedback Amplifier Line Driver Circuits (Post-emphasis Section)

POST-EMPHASIS SECTION

The circuitry of the post-emphasis section is almost identical with that of the pre-emphasis section described above, therefore, only areas where there are distinct differences will be described.

Refer to the simplified schematic figure 17 and to typical waveforms on figure 18. Video from the Demodulator (module 203B), still with high frequency pre-emphasis introduced before modulation, is fed at a 1.0-volt level to the DEMOD LEVEL control, R12. This control is a screwdriver adjustment located on the front panel. The purpose of the DEMOD LEVEL potentiometer is to compensate for variations in Demodulator sensitivity and permit precise setting of output level.

Emitter follower Q2 drives the post-emphasis network selected by K2 and S1A or S1B. This network is a voltage divider consisting of R15 in series with a capacitive impedance to ground. Transmission

through the divider decreases with frequency because of the greater shunting effect of the capacity at higher frequencies. Furthermore, the transmission of the post-emphasis network exactly complements that of the pre-emphasis network, both with respect to frequency selective and nonselective transmission. This may be seen by observation of Table 2. Relay K2 is energized in the same way as described for pre-emphasis selector relay, K3, depending on the position of the Vertical Advance TV STANDARDS switch. From the output of the equalizer the signal is handled in the same manner as in the pre-emphasis section, although the total gain is higher to provide an output level of 2.0 volts.

Variable post-emphasis is incorporated to permit the response of a monochrome signal to be varied somewhat in order to accommodate nonstandard tapes. The variable equalizer is activated by K1, which is energized through VAR POST EMPH switch S2, overriding whatever fixed standard is selected by S1.

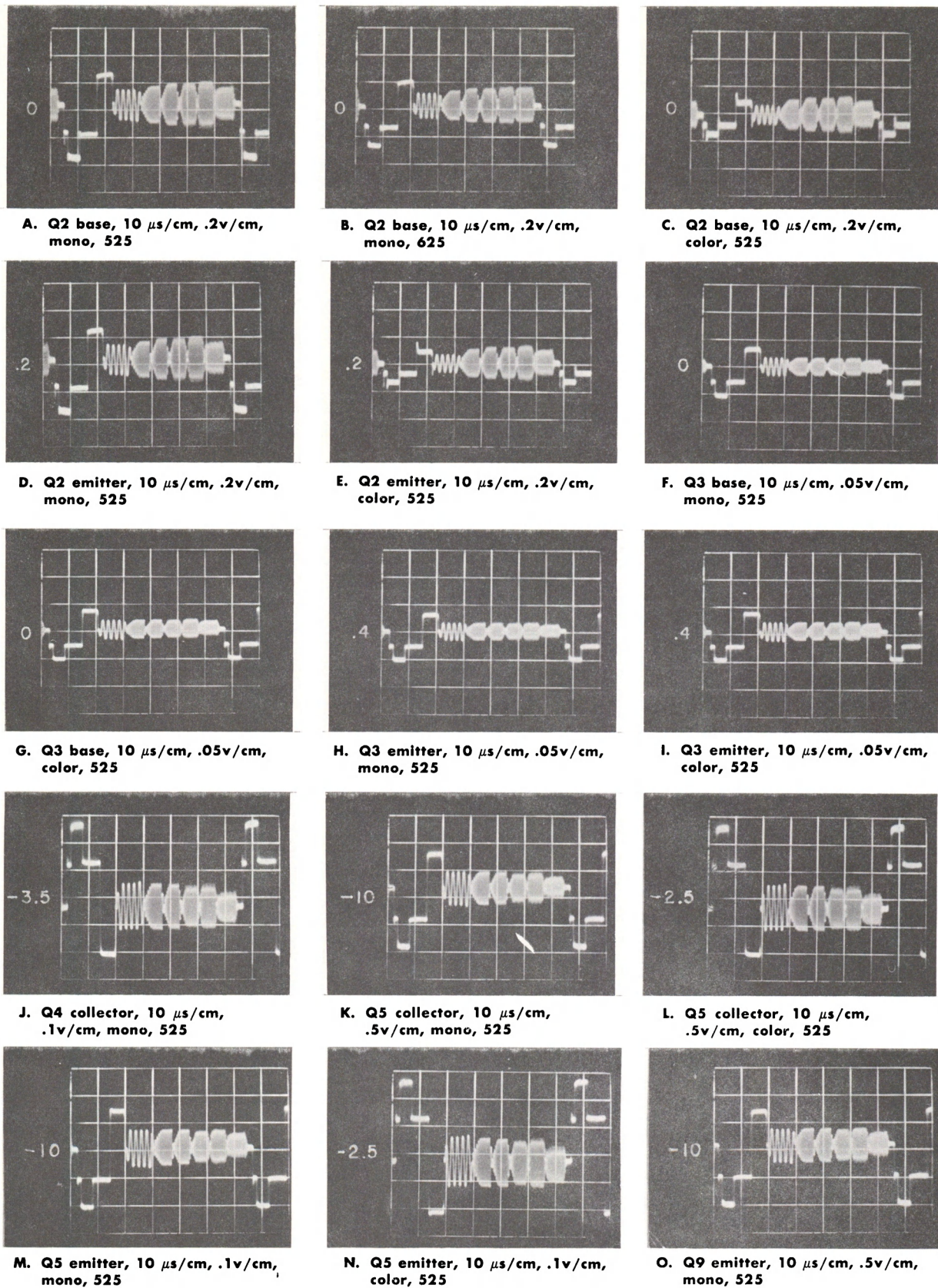


Figure 18—Typical Waveforms; Equalization, Feedback Amplifier and Line Driver Circuits (Post-emphasis Section)

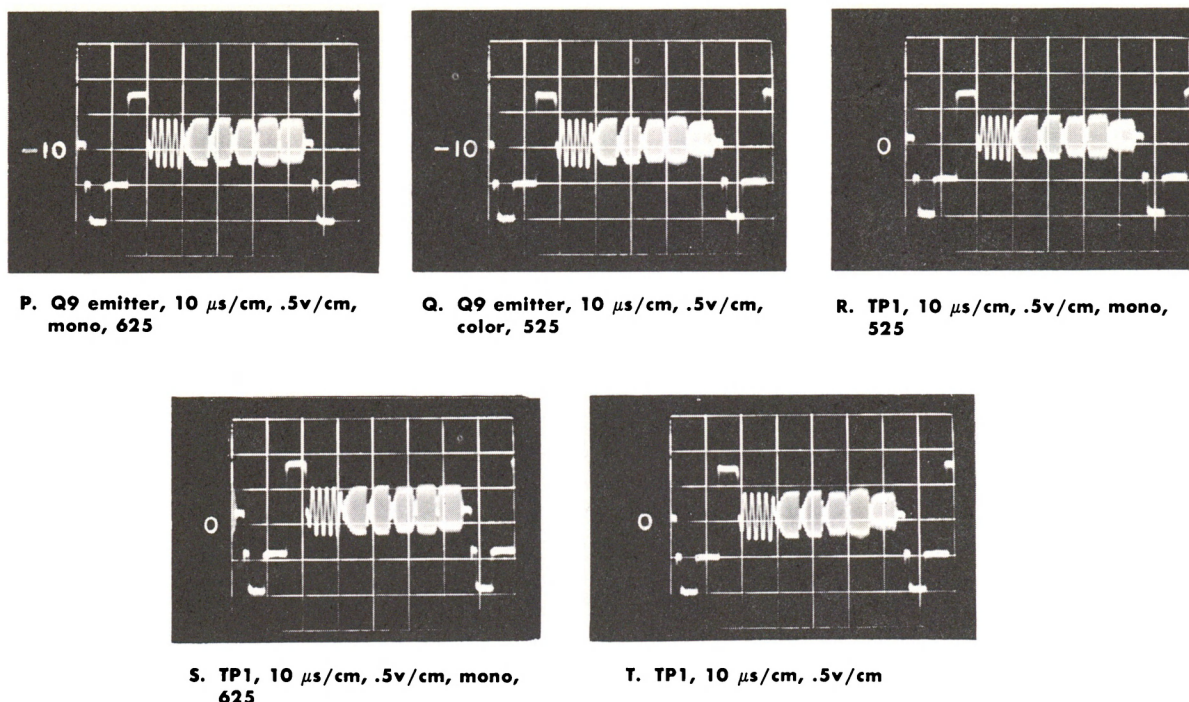


Figure 18—Typical Waveforms; Equalization, Feedback Amplifier and Line Driver Circuits (Post-emphasis Section) (Continued)

CONTROL CIRCUITS

Two sections of STDS switch, S1, are used for switching pre-emphasis equalization, and two are used for post-emphasis selection, as described before. As shown in simplified schematic figure 19, another section, S1E, functions in an indicator facility by grounding the appropriate return circuit of standards indicator lamps 5DS23-24.

FM Reference crystals and Modulator preset sync tip frequency are switched by means of S1C and S1D in conjunction with d-c control signals from the Vertical Advance module. The control signals, designated VI SP and VN SP, are either -20 volts or ground potential, depending on the position of the TV STANDARDS switch in the Vertical Advance. This relation is depicted by the chart in figure 19. The VI SP bus is switched by S1C to any one of five terminals designated "50 FIELD". Similarly, the VN SP bus is switched by S1D to one of another group of five terminals designated "60 FIELD". A third group of four terminals, designated REF MODE, is connected to reference crystal switching transistors in the FM Reference (module 302A) and to SYNC TIP FREQ PRESET controls R53-R56 used to preset Mod-

ulator sync tip frequency. At any given time only one terminal in the 50 FIELD and 60 FIELD groups will be at -20 V; all the others will be at ground potential.

In effect then, the five terminals in the 50 FIELD group and in the 60 FIELD group correspond to the five positions of S1, representing deviation limits. Which of the groups contains the terminal at -20 V depends on the TV STANDARD selected. Jumper connections, from the 50 and 60 FIELD terminals to the REF MODE terminals, transfer -20 V to the appropriate SYNC TIP FREQ PRESET control and reference frequency crystal switches. Diodes CR5-8, in series with each sync tip control prevent the -20 V potential at the active control from feeding back to the three inactive REF MODE buses. Diodes CR3, CR4 prevent -20 V from being short circuited under conditions where VI SP and VN SP buses are interconnected in the control system.

Jumper wires are installed as shown in figure 19. The first three positions of STDS switch S1 are used for STD MONO.

Note from the chart in figure 19 that when 625 or 819 TV STANDARDS are selected, VN SP is ground potential and VI SP is -20 V. The negative VI SP

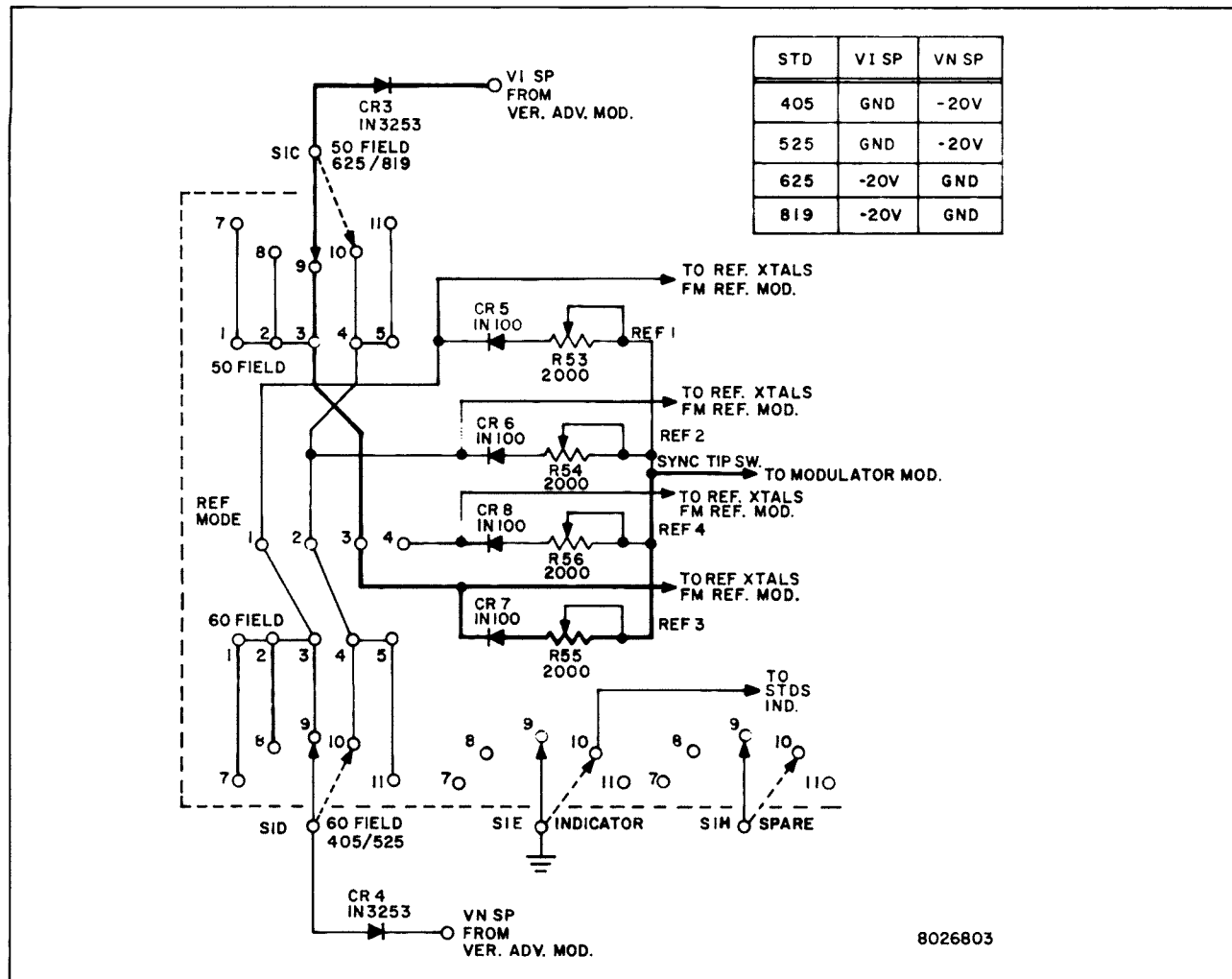


Figure 19—Simplified Schematic, Control Circuits

voltage causes CR3 to conduct, allowing current to pass through S1C-9 to 50 FIELD terminal 3 which is, in turn, jumpered to REF MODE terminal 3. This activates the pair of crystals in the FM Reference module associated with 625 standard monochrome deviation (5.0 mc and 6.8 mc) and develops a voltage across R55, which is adjusted for correct sync tip frequency (5.0 mc). Diodes CR5, CR6 and CR8 are reversed biased.

To change operation from 625 standards to 525, the TV STANDARDS switch is merely rotated to 525. Relays K2 and K3 are then energized, switching out the 625 pre- and post-emphasis networks, and switching in the 525 networks. Simultaneously, the VI SP and VN SP buses change state, the former becoming grounded and the latter -20V. Now CR4, which had been cutoff, is made to conduct current from the VN SP bus through S1D-9 to 60 FIELD terminal 3, and through a jumper to REF MODE terminal 1.

This changes the Modulator sync tip frequency to the value established by R53 and permits activation of appropriate reference frequency crystals (4.28 mc and 6.8 mc). Diodes CR3, CR6, CR7 and CR8 are cut off.

If color operation is required, S1 is rotated to STD COLOR (dashed lines, figure 19). The VN SP bus, which is still -20V, continues to cause CR4 to conduct. Current now passes through CR4 to S1D-10, to 60 FIELD terminal 4, and by jumper to REF MODE terminal 2. This permits crystals associated with color deviation (5.5 mc and 6.50 mc) to be activated. Also, sync tip frequency is changed to the correct preset value of 5.5 mc by current conducted through CR6 to R54. Note that on color standards, both the VI SP bus and VN SP bus are connected together through CR3 and CR4, respectively, to REF MODE terminal 2. A short circuiting of the -20V VN SP potential by the grounded VI SP is prevented by CR3, which is cut off by the negative voltage at REF MODE terminal 2.

CONTROL CIRCUIT SET-UP CONNECTIONS

Although normal connections are suitable for most requirements, unique individual needs or new standards may necessitate changes in jumper wiring. This will be most easily accomplished by considering the following factors:

1. The numbers on the 50 and 60 FIELD terminals correspond to STDS switch, S1 position, i.e., terminal 1 is associated on either 50 or 60 FIELD standard with the extreme counterclockwise position of S1.

2. The numbers on the REF MODE terminals correspond to pairs of deviation reference crystals in the FR Reference (module 302A), i.e., terminal 1 is associated with Y1, Y10 in module 302A. Numbers applied to SYNC TIP FREQ PRESET controls also correspond to REF MODE terminal numbers.

In making new jumper connections, first determine what switch positions are to activate a given REF MODE. Then decide which TV STANDARD is to apply to the switch positions selected. Connect a jumper to the desired REF MODE terminal from either the 50 or 60 FIELD terminals corresponding to S1 switch positions which are to activate that particular REF MODE. In cases where a REF MODE is to be active on both 50 and 60 FIELD standards, such as the normal color connections, proceed as follows: Connect jumpers to the desired REF MODE terminals from 50 FIELD terminals corresponding to selected switch positions and from the associated 60 FIELD terminals.

MODULATOR (Module 207B-S)

GENERAL

The video signal is not directly recorded on tape because of limitations on linearity and useable frequency spectrum imposed by magnetic components of the record/playback system. Instead, a signal is generated that is constant in amplitude, but with the frequency varying according to the amplitude fluctuations of the video components. This frequency modulated signal is produced by the Modulator. (Refer to the block diagram, figure 20).

Pre-emphasized video from the FM Standards (module 205A) is amplified and clamped at sync tip to an adjustable dc potential. The clamped video is then direct coupled to two pairs of variable capacitance diodes. These diodes, when reverse biased, appear as capacitors, the amount of capacity being an inverse function of the bias. One pair of diodes is used in the tuned circuit of a high frequency oscillator

to produce an output of 60 mc. The other pair is used in a relatively lower frequency oscillator to provide an output of 55.72 mc. Video and diode polarities are such that a white-going video transition causes a decrease in capacity of the pair of diodes associated with the high frequency oscillator (HFO), while increasing the capacity of the pair that tune the low frequency oscillator (LFO). Therefore, an increase in video brightness level increases the HFO frequency a corresponding amount, and simultaneously decreases the LFO frequency the same amount. In effect, the two oscillators are driven in push-pull by the video components of the signal.

The oscillator outputs are heterodyned in a doubly balanced diode mixer that cancels the original HFO and LFO frequencies. At the output of the mixer appears only the modulation products or sum and difference frequencies. The output of the mixer is amplified and then fed to a low pass filter which eliminates all of the modulation products except the oscillator difference frequency and FM sidebands. The signal finally obtained has a frequency directly related to the instantaneous amplitude of the video input signal.

The reference of the FM signal is the sync tip frequency. This is determined by a dc potential to which sync is clamped, and this is adjusted primarily by a variable resistor in the FM Standards (module 205A). A vernier adjustment is also available on the Modulator front panel. The peak deviation from sync tip reference depends on peak video amplitude, and is adjusted by the DEVIATION control on the front panel of the FM Standards module.

Clamp keying pulses are generated from the leading edges of separated sync from the Video Input (module 103).

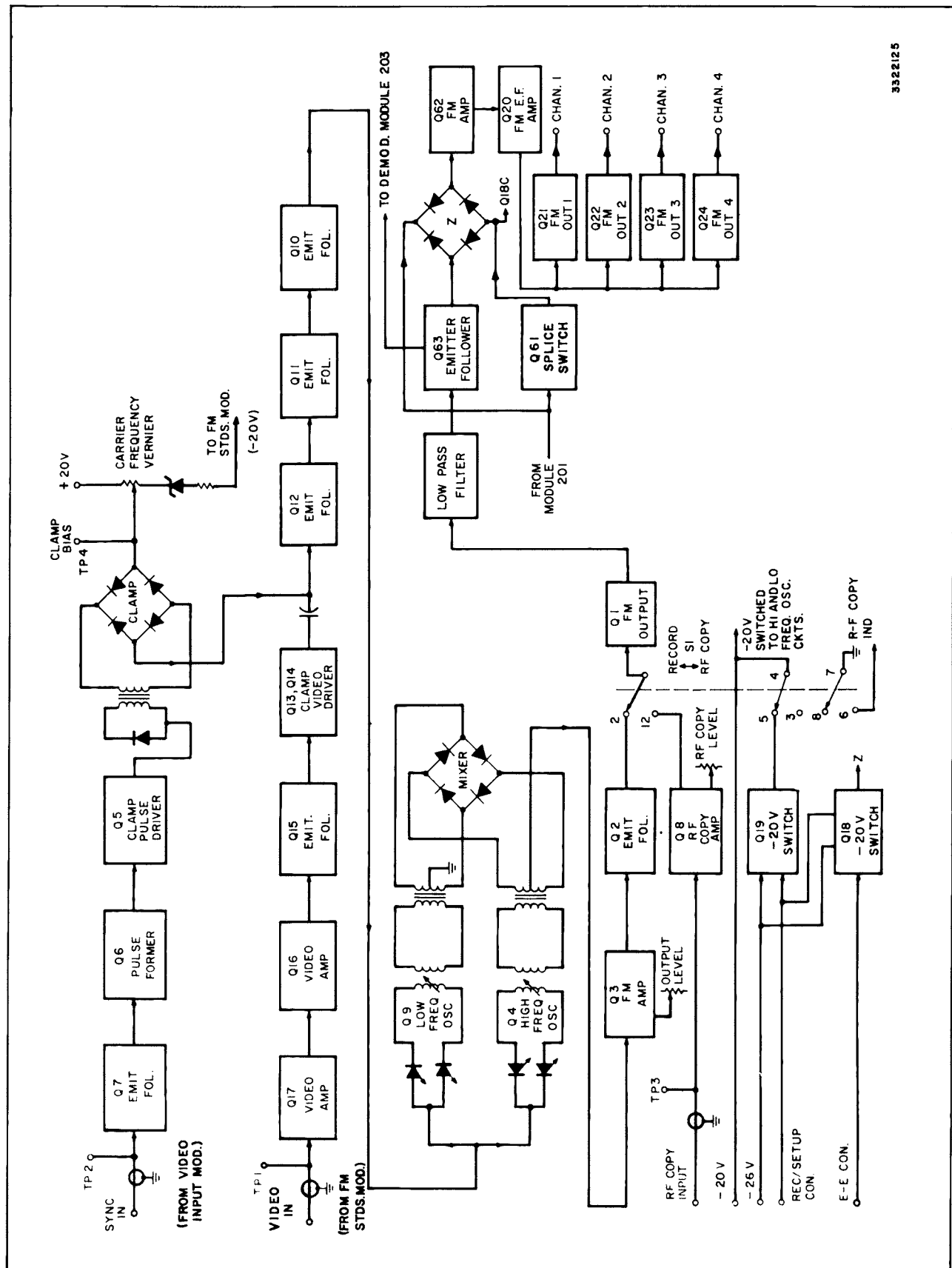
The modulator contains electronic switching to disable the oscillator in PLAY mode.

An R-F COPY facility is provided to enable making a dub of another recording without the necessity of demodulating the playback FM.

CIRCUIT

Video Amplifiers, Clamp Driver and Oscillator Driver

As shown in figure 21, pre-emphasized video is fed from the FM Standards (module 205A) to the base of Q17, an emitter follower. The level of the signal at this point is approximately .2 volt per megacycle of FM deviation. Thus the video amplitude at the base of Q17 will be about .5 volt when a standard mono-



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Figure 20—Block Diagram, Modulator Module

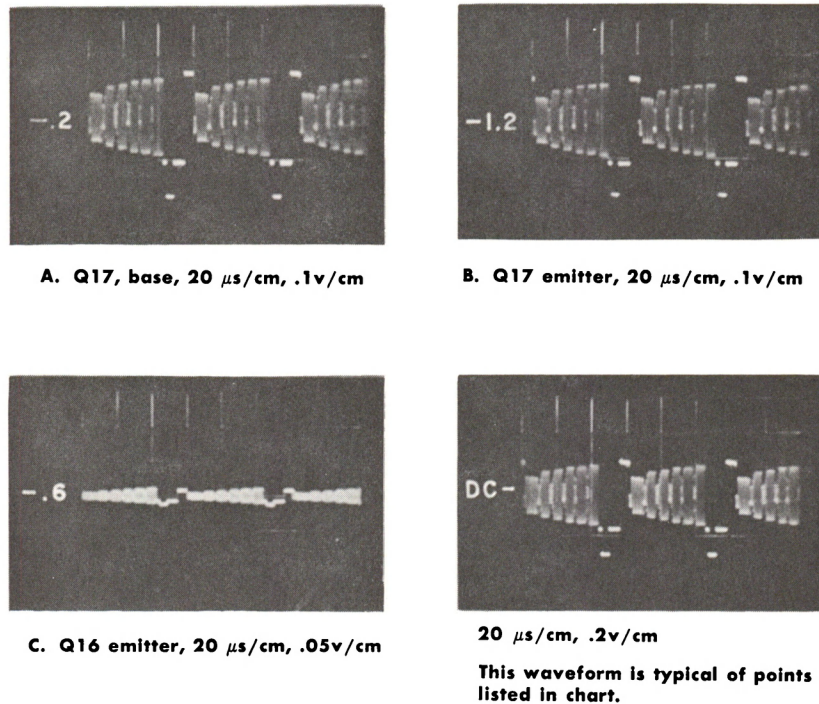


Figure 22—Typical Waveforms; Video Amplifiers, Clamp Video Drivers and Oscillator Driver Circuits

The clamp video drivers, Q13, Q14, are emitter followers connected to form a complementary-symmetry amplifier, the output of which drives the clamp coupling capacitor, C48. A dc reference voltage which clamps the tip of sync is added to the video signal at the output side of C48. The dc reference voltage is interposed in the signal by means of the clamp quad Z2, which is switched on for a short period during the horizontal sync interval.

The complementary-symmetry arrangement enables the clamp coupling capacitor, C48, to quickly follow sudden changes in potential caused by errors in black level during the horizontal sync interval. Errors typically result from sudden brightness changes in picture content, switching disturbances, or spurious low frequency interference. Since one transistor is an NPN and the other a PNP, a spurious surge will have an equal but opposite effect on each transistor. One will be driven into saturation while the other goes to cut-off as C48 charges or discharges, as required, through the clamp diodes in order to maintain the sync tip at the dc reference level.

Under normal signal conditions, Q13 and Q14, in effect, operate in parallel with the output on their emitters following in phase the positive and negative signal excursions. By virtue of the direct coupling existing between the collector of Q16 and the bases of Q13 and Q14, a +10 volt bias is supplied to the bases by the voltage divider formed by R69 and R71.

A quiescent current of approximately 3 ma flows through Q13 and Q14. This is obtained in Q13 by returning the emitter to ground through R67. And similarly in Q14 by placing R68 in series with the emitter to the +20 volt supply. This idling current eliminates crossover distortion that is otherwise characteristic of a complementary-symmetry emitter follower circuit. Coupling capacitor C49 provides isolation between the two emitters, thus preventing small differences in dc potential from upsetting the quiescent bias conditions.

After being clamped, the video is fed to the base of Q12, an emitter follower. The level of the video at this point is higher than that subsequently required

for proper deviation, in order to lessen the effects of unbalance in the clamp quad diodes. Transistor Q12 along with the following two emitter followers, Q11 and Q10, form a direct coupled cascade amplifier. The purpose of the three cascaded emitter followers is to reduce loading on the clamp coupling capacitor, C48, and to provide a low impedance drive source for the variable capacitance diodes. (The latter are in the tank circuits of the high and the low frequency oscillators, Q4 and Q9, respectively.) An attenuator consisting of R64 and R65 in the emitter of Q11 reduces the video to the level necessary for proper deviation. Capacitor C51 in parallel with R64 boosts the high frequency response about 1 db at 4 mc. The amplitude of the video output at the emitter of Q10 is approximately 1.2 volts per megacycle of deviation, or 3 volts for a standard monochrome signal of 2.5 mc.

High and Low Frequency Oscillators

From the emitter of Q10, the signal is direct coupled through CR6-CR9 to two pairs of variable capacitance diodes, CR1, CR2 in the tank circuit of the high frequency oscillator, Q4, and CR4, CR5 in the tank circuit of the low frequency oscillator, Q9 (figure 23). The operation of both oscillators is the same except that the reactance of each pair of variable capacitance diodes varies in opposite directions to the applied video signal.

The low frequency oscillator, Q9, is connected in a Colpitts configuration. A resonant circuit consisting of L10 in parallel with CR4, CR5 is ac coupled from the collector to the base. The feedback voltage is developed across the voltage divider formed by C40 and C41, the amount of feedback being determined by C41. DC bias is established by emitter resistor R55, and base bias by R53 and R54. The dc operating voltage is supplied to this stage from the -20 volt switched bus through rf choke L9 to the emitter return. Block capacitors C42 and C43 isolate the fixed bias on the variable capacitance diodes from ground.

Bias for CR4 and CR5 is supplied from two sources, one fixed, the other variable. The fixed source is the voltage divider consisting of R58 and R59 which is returned to +20 volts. The bias developed across this divider is a constant positive dc potential which is fed to the cathodes of CR4 and CR5 through isolation resistors R56 and R57. The variable bias source is the video drive which is coupled from Q10 through CR6-CR9 and fed through r-f choke L11 to the anodes of CR4 and CR5. This bias is comprised of two components, one being the video itself and the other a nega-

tive dc potential that is derived from the adjustable reference potential to which sync is clamped.

Diodes CR4 and CR5 remain reverse biased at all times. In conjunction with L10, they tune the low frequency oscillator, Q9, by exhibiting a varying reactance that is determined by the instantaneous value of the applied video signal. The reactance characteristics of the diodes is such that an increase in reverse bias causes a decrease in capacity, thus raising the output frequency of the oscillator. Since sync is the most negative part of the video signal, the oscillator frequency will be highest during this portion of the picture, becoming lower as the signal swings towards the more positive, white region.

The same video signal is simultaneously applied through r-f choke L8 to the variable capacitance diodes, CR1 and CR2, of the high frequency oscillator Q4. However, in contrast to the low frequency oscillator, the signal is fed to the cathodes of CR1 and CR2, and a fixed high negative bias is fed to the anodes through isolation resistors R21 and R22. The fixed bias is developed across the voltage divider formed by R25 and R26, which is returned to the -20 volts switched bus.

The output of the high frequency oscillator, as opposed to that of the low frequency oscillator, is lower in frequency during the sync interval, becoming higher as the video signal swings towards the more positive white (higher negative bias) region. As shown in figure 24, the video signal in its excursion from peak white to sync tip modulates the two oscillators in opposite directions, i.e., as the frequency of one oscillator increases, the frequency of the other decreases. The output frequencies diverge during white-going video transitions and converge during black-going transitions. The difference between the two oscillators is extracted by the mixer (as described later), resulting in the FM signal that is ultimately recorded.

The diode bias and oscillator frequencies typical of standard monochrome operation which are depicted graphically in figure 24 are not exactly representative of the modulator, in that they do not show the curvature characteristic of the actual circuit. This is of no practical significance, however, because the push-pull modulation of the oscillator tends to cancel nonlinearity over the entire range of operation.

As noted earlier, the variable bias applied to the variable capacitance diodes, in the tank circuit of the oscillators, consists of a video component and a nega-

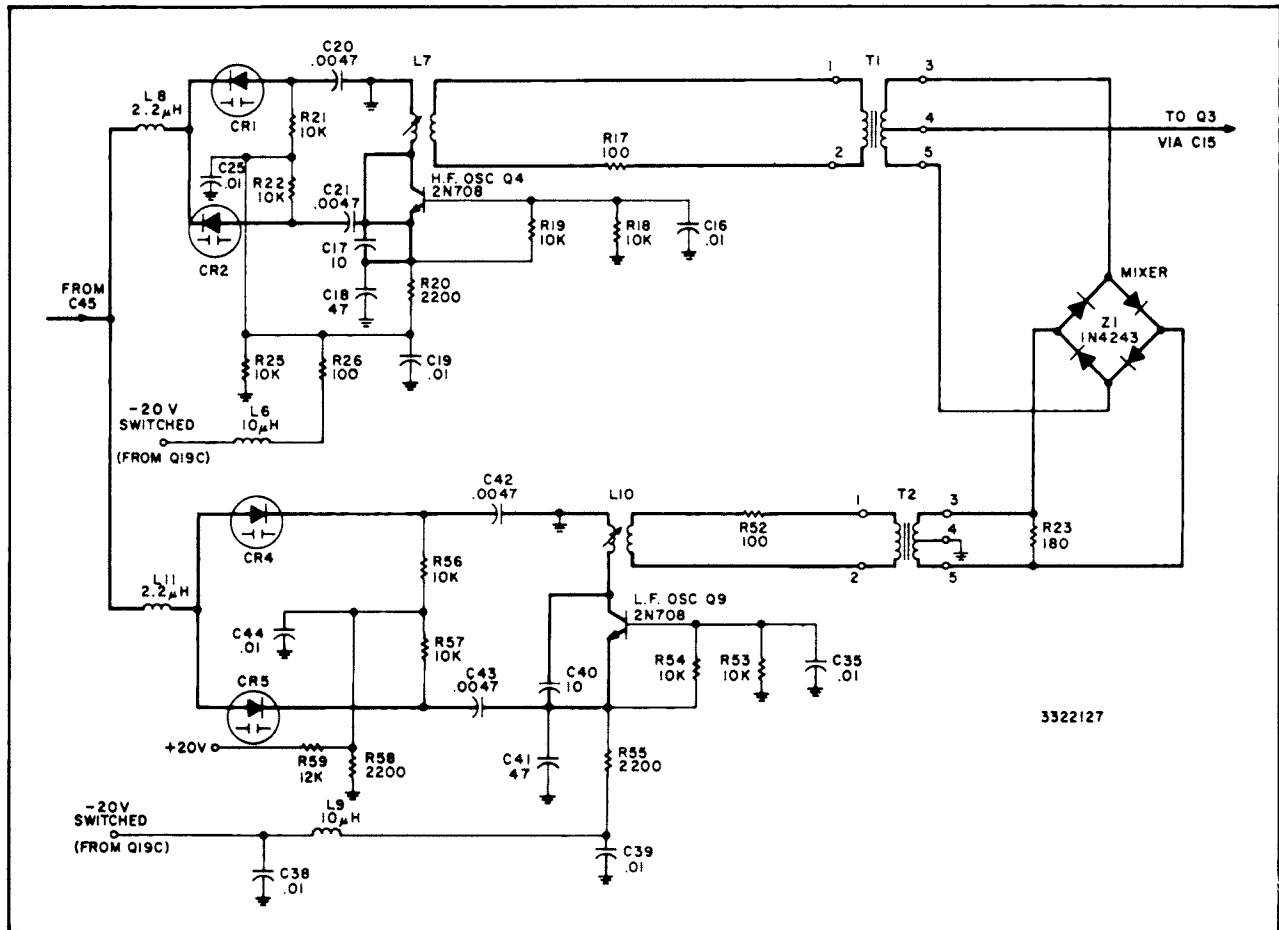


Figure 23—High and Low Frequency Oscillators and Quad Mixer Circuits

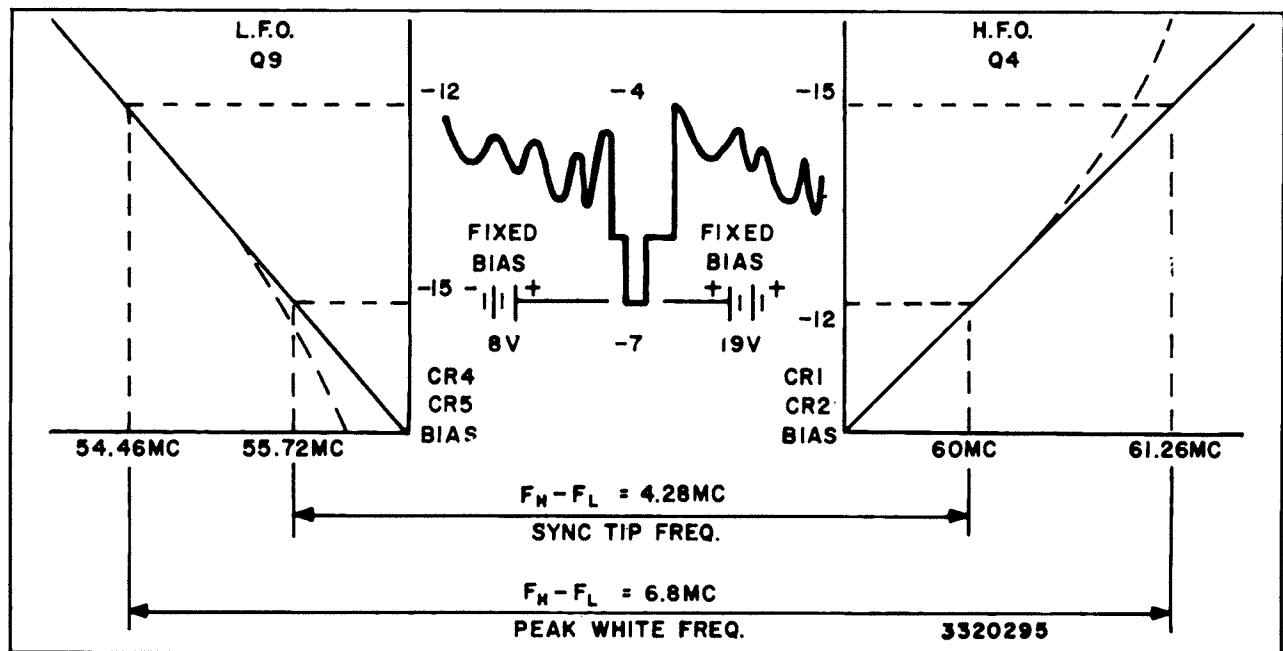


Figure 24—Modulation Transfer Characteristics

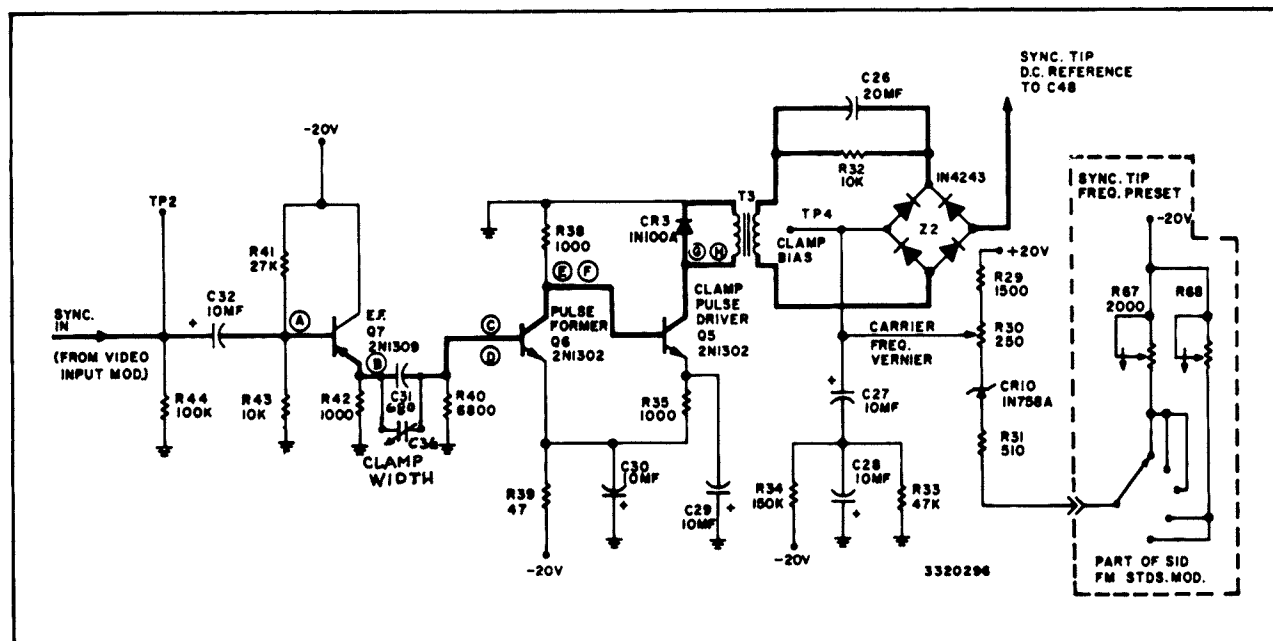


Figure 25—Pulse Former and Sync Tip Clamp Circuits

tive dc component. The source of the video component is, of course, the video input signal. Not so obvious is the origin of the dc component; therefore, the next part of this discussion will cover the manner in which the dc potential is obtained and its effect on the output frequency of the oscillators.

Variable DC Bias

The dc potential depends upon the sync tip reference, and is available as the CLAMP BIAS (TP4) which is passed by the clamp quad, Z2 (figure 25). The clamp bias, or reference voltage is determined by a voltage divider between -20 volts and $+20$ volts. The divider is comprised of R29, R30, Zener diode CR10, R31, and R67. Potentiometer R30 is a screwdriver adjustment on the front panel of the Modulator designated CARRIER FREQ VERNIER. Resistor R67 is one of the SYNC TIP FREQ PRESET potentiometers which are internal controls on the FM Standards module.

Adjusting either the CARRIER FREQ VERNIER or the SYNC TIP FREQ PRESET causes a shift in the clamp reference voltage that is transferred to the variable capacitance diodes. The resulting change in dc bias causes a change in the reactance of the diodes. This, in turn, produces a corresponding frequency change in that portion of the modulator output frequency that represents the sync tip region (figure 27). Since all other frequency components of the video waveform occupy various levels that bear a fixed rela-

tion to sync, the frequencies represented by these levels will also be displaced to the same degree as sync.

A similar change in output frequency can be produced by tuning coils L7 and L10 in the collector circuits of the high and low frequency oscillators, respectively. These coils, however, are not intended as operational controls, and they should not be adjusted during set-up or routine maintenance.

Thus, in the modulation process as described here, deviation depends on the amplitude of the video signal fed into the Modulator, and carrier frequency is determined by the setting of a dc potential in the FM Standards module in conjunction with a vernier adjustment on the Modulator.

Bias Stabilization

To return to diodes CR6-CR9 (figure 21). The chief function of these diodes is to compensate for an increase in ambient temperature which causes the carrier frequency to have a tendency to drift. Due to the physical properties of semi-conductors, temperature variations produce changes in the internal voltage drops across the junctions of the variable capacitance diodes. These internal voltage changes appear as spurious bias variations. In this case, an increase in temperature will cause the dc bias on the variable capacitance diodes to become more positive, tending to produce an increase in frequency. The parameters of the temperature stabilization diodes are such that the

dc bias fed to the variable capacitance diodes is modified by the amount that counteracts drift. Negligible impedance to the video signal is offered by the diodes, since they conduct constantly and are by-passed by coupling capacitor C45. Forward bias is applied to the diodes by the current flow through the voltage divider formed by R27 and R28 from the +70 volts.

Mixer

The output from the high frequency oscillator, Q4, and the low frequency oscillator, Q9, is link-coupled through transformers T1 and T2, respectively, to the diode mixer, Z1 (figure 23). The secondaries of T1 and T2 are balanced, with each supplying push-pull drive to the ring-connected diodes of Z1.

The mixer output is taken off the center tapped secondaries of T1 and T2, where, due to the balanced nature of the transformers, there is no voltage developed at the original input frequencies. Between the center tap and the top and bottom of each secondary, however, a voltage is developed that is the product of modulation resulting from non-linear operation on the input signals by the mixer diodes. These modulation products are the sidebands or sum and difference frequencies of the oscillator inputs.

The upper sidebands, which represent the sum frequencies, are relatively low in amplitude since they are in the region of 100 mc. However, these signals can be disregarded, since it is the lower sidebands or difference frequencies, which are in the 1 to 5 mc

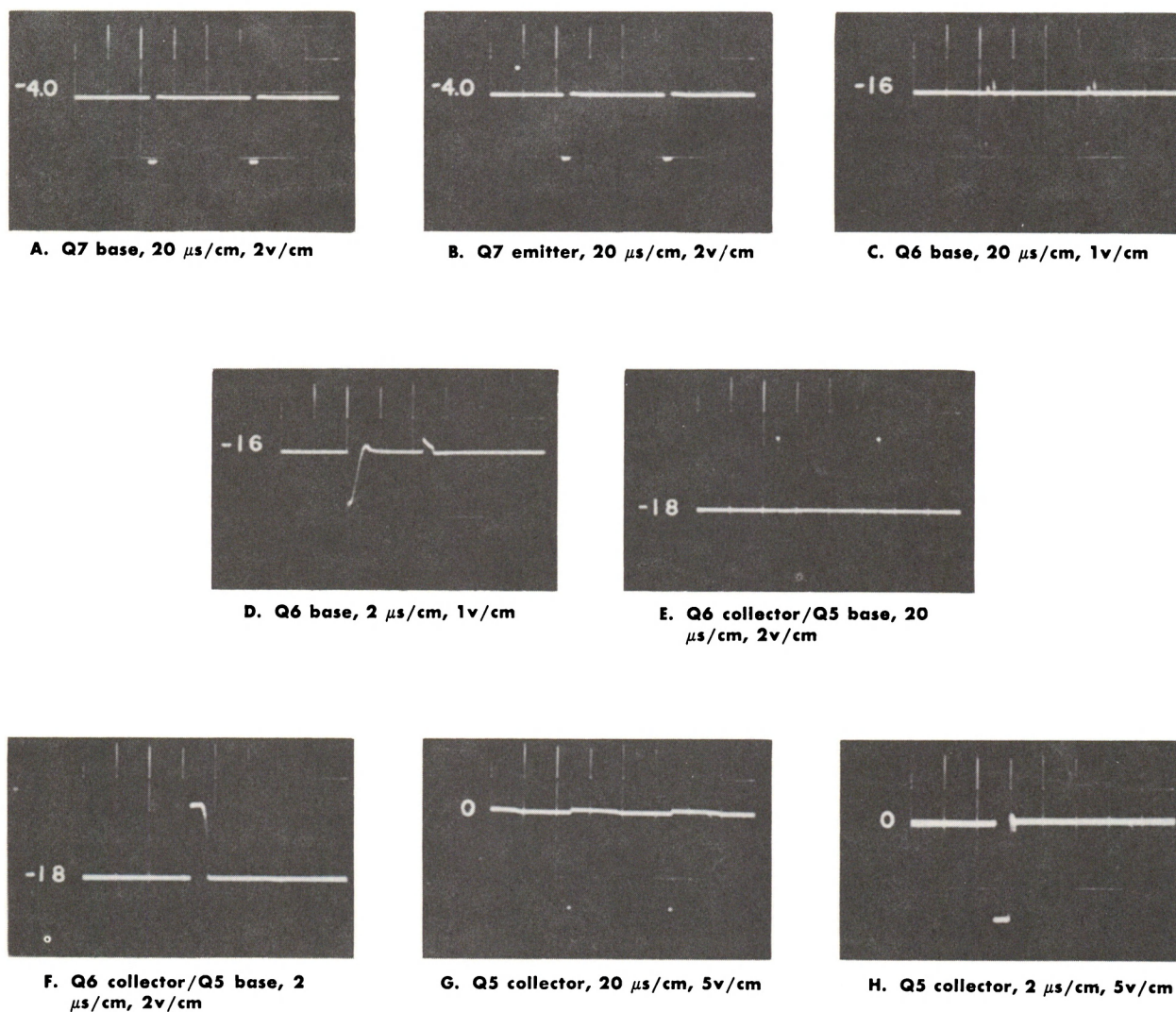


Figure 26—Typical Waveforms; Pulse Former and Sync Tip Clamp Circuits

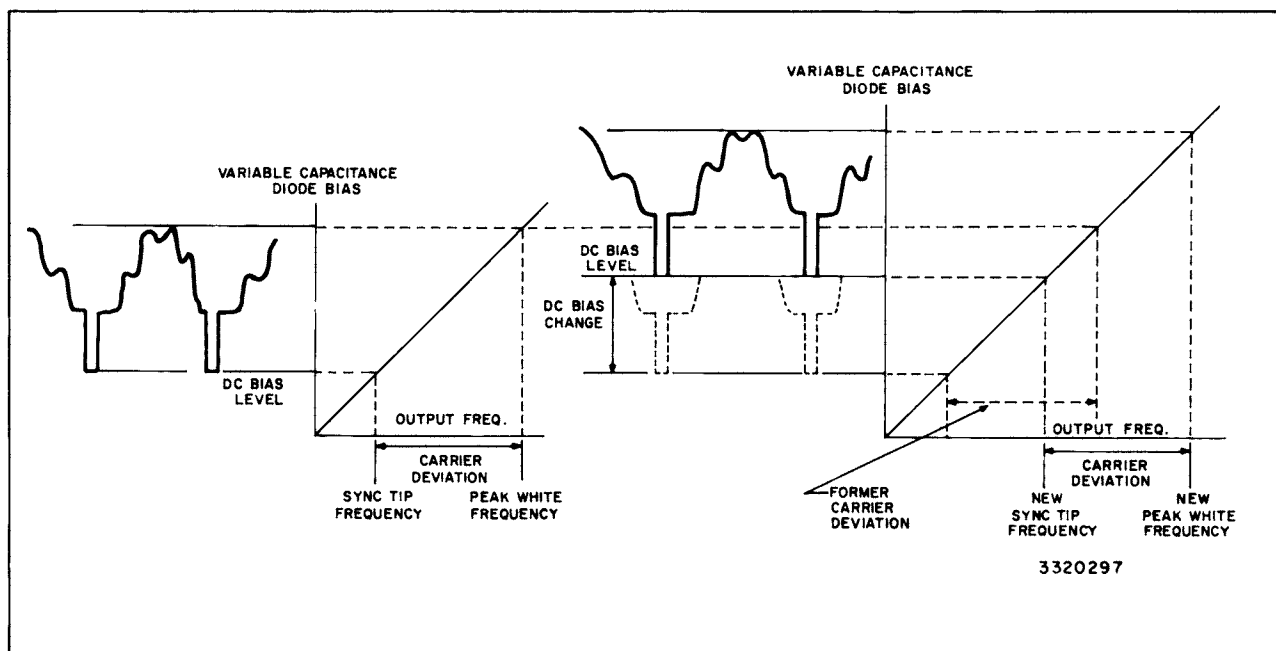


Figure 27—Effect of DC Bias on Carrier Frequency

range, that are desired. The peak-to-peak amplitude of the lower sidebands is .5 volt and this signal is coupled through C15 to the base of Q3, the FM amplifier (figure 28).

FM Amplifier, R-F Copy Amplifier and FM Output

Maximum gain of Q3 is about 4 and this is determined by R14 in the emitter circuit. The gain of this stage can be controlled by varying the amount of degeneration in the emitter with R15, the OUTPUT LEVEL potentiometer, in conjunction with C14. The dc operating conditions are set by bias resistors R13, R16 and the total emitter resistance consisting of R9, R14, and R15 in series with the -20 volts.

The amplified FM output at the collector of Q3 is coupled through C13 to the base of Q2, an emitter follower, which isolates the collector of Q3 from capacitive loading by the following stages. Peaking coil L5, in series with R10, the collector load of Q3, provides compensation for the stray capacitance shunting the collector circuit.

The output from the emitter of Q2 drives one pole of S1, the RECORD/R-F COPY switch. Two other stages, Q8, the R-F Copy amplifier, and Q18, Q19, the -20 volt switch, drive other poles on S1.

The R-F Copy amplifier, Q8, amplifies the FM signal from another recorder. This stage permits a tape to be copied without first having to demodulate the

FM signal to video then convert it to FM again in the recording process. The operation of Q8 is similar to that of the Q3, the FM amplifier, except that the output of the former is FM originating in another recorder, while the output of the latter is FM generated within the Modulator itself.

The signal from either amplifier is selected by S1 and coupled through C1 to the base of the FM output stage, Q1, an emitter follower. In addition to selecting the FM signal for recording, S1 when in the R-F COPY position performs two other functions. One, it disables the high (Q4) and the low (Q9) frequency oscillators by removing the dc operating voltage, -20 volts switched, from these stages; two, it energizes the R-F COPY indicator lamp above the PLAY control panel.

In the normal RECORD mode, FM output level is adjusted by means of R15, the OUTPUT LEVEL potentiometer. In the R-F COPY mode, the output level is adjusted by means of R49, the R-F COPY LEVEL potentiometer. Both are internal controls.

The purpose of the -20 switch, Q18, Q19, is to electronically enable or disable the Modulator, according to the mode in which the TR-22 is being operated. A functional analysis of the -20 switch will be given later.

The FM output from the emitter of Q1 is coupled through a source terminating resistor, R2, and capacitor C9 to drive a low pass filter. The cut-off frequency

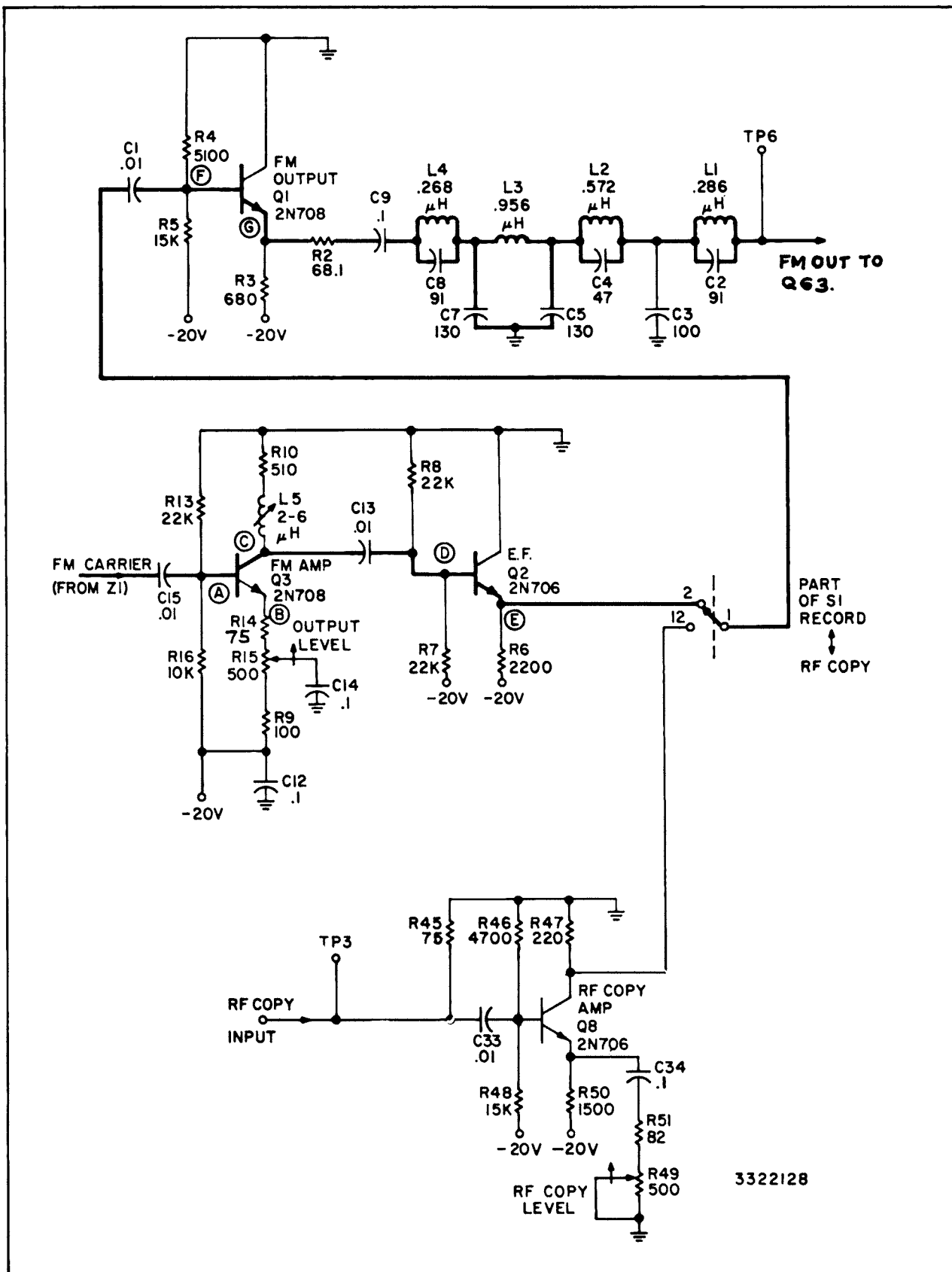
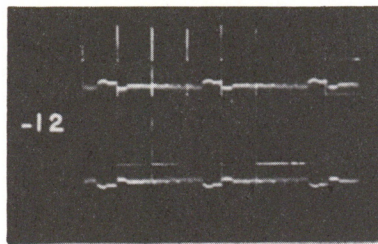
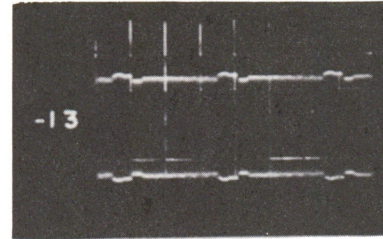


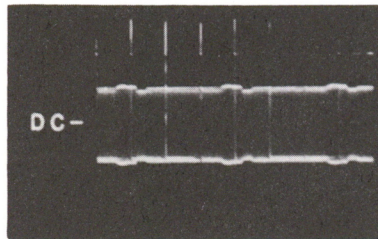
Figure 28—FM Amplifiers, FM Output and R-F Copy Circuits (Modulator 207B-S)



A. Q3 base, 20 $\mu\text{s}/\text{cm}$, .1v/cm.



B. Q3 emitter, 20 $\mu\text{s}/\text{cm}$, .1v/cm.



20 $\mu\text{s}/\text{cm}$, .05v/cm.

This waveform is typical of points listed in chart.

KEY	LOCATION	AC AXIS
C	Q3C	— 1.5v
D	Q2B	— 9.8v
E	Q2E	— 10.5v
F	Q1B	— 5.0v
G	Q1E	— 5.7v

Figure 29—Typical Waveforms; FM Amplifiers, FM Output and R-F Copy Circuits (Modulator 207B-S)

of the filter is 25 mc, which is sufficiently low to eliminate any oscillator frequency components not cancelled in the balanced mixer, as well as the upper sideband frequency components produced by the mixer. However, the bandwidth of the filter is broad enough to permit transmission of all sidebands necessary for wideband recording.

The modulator has circuits added to enable the machine to be modified for electronic splicing without further changes to the module. These circuits are in the form of Q61, Q62, Q63 and the switcher quad (Z). In normal operation the quad passes FM from Q63 and the low pass filter, to Q62 and Q20 emitter follower. Q21 through Q24 are identical output amplifiers used to feed FM signals to the four Record Amplifiers.

Splice Auxiliary Board for Module 207B-S (Refer to figures 19 and 29)

The output of the low-pass filter is coupled via capacitor SAC3 to the base of emitter-follower Q63. Emitter-follower Q63 divides the signal into two

paths: one path goes to the limiter section of the Demodulator module 203B, the other path is to the input side of the switcher quad Z. When the switcher quad is turned on by a —20 volt switch composed of Q18 and Q19 and the splice record control circuits (in module 201), the signal is applied through resistor SAR11 to the base of FM amplifier Q62. FM amplifier Q62 drives the base of emitter-follower Q20, which in turn, drives emitter followers Q21, Q22, Q23, Q24. The outputs from emitter-followers Q21, Q22, Q23, Q24 are applied to four Record Amplifiers (Modules 211, 212, 213, 214).

Sync Tip Clamp

The operation of the clamp pulse former and the sync tip clamp circuitry (figure 25) is as follows:

Separated sync at 4 volts peak-to-peak from the Video Input (module 103) is coupled through C32 to the base of Q7, an emitter follower. Transistor Q7 is biased with base bias resistors R41, R43 and emitter resistor R42. A reproduction of sync, but from a low impedance source, appears at the emitter of Q7. The

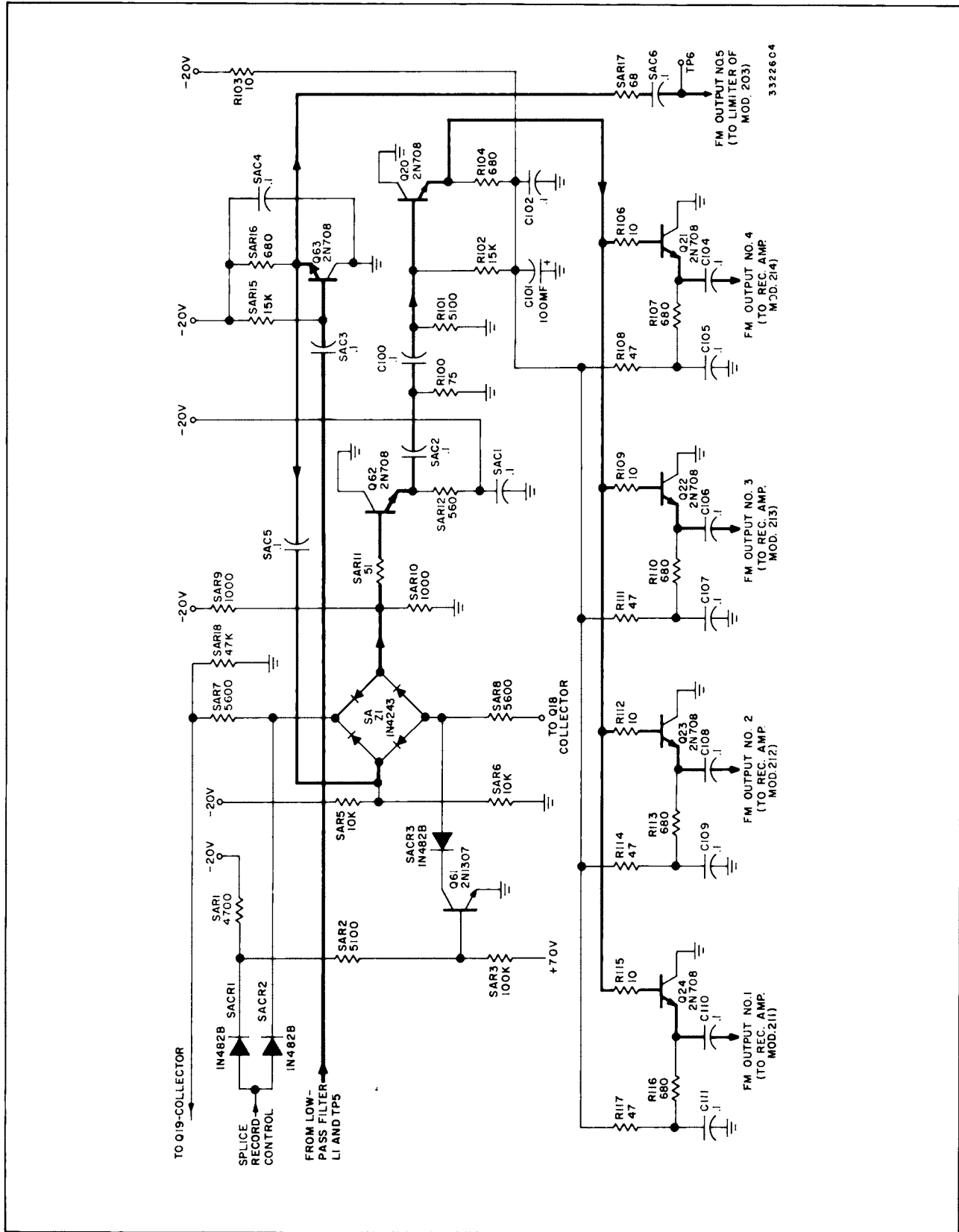


Figure 30—FM Output Line Drivers (Modulator 207B-S)

pulse former, Q6, is normally saturated because of the high positive base current resulting from the -20 volts emitter potential and the grounded base return resistor, R40. Under these conditions the collector potential of Q6 is also approximately -20 volts.

When a sync or an equalizing pulse occurs at the emitter of Q7, the negative-going leading edge is coupled through C31 and C36 to the base of Q6, cutting off Q6 and permitting the collector potential to move towards ground. Immediately following the negative-going excursion of the pulse, the base of Q6 begins to return to ground, as C31 and C36 charges through R40. The time constant of C31, C36, R40 is such that the base of Q6 approaches ground in about 1.0 microsecond. When the potential on the base becomes sufficiently close to ground, Q6 saturates and the collector goes to approximately -20 volts.

The base of Q5 is direct coupled to the collector of Q6. Resistor R38 serves as the collector load for Q6 and as the base bias resistor for Q5.

Transistor Q5 is cut off during the picture interval, which is the period that Q6 is saturated with its collector at -20 volts. With Q5 cut off, no current flows in the primary of T3.

During the 1.0 microsecond interval following the negative going transition of the leading edge of sync (when Q6 is cut off), the base of Q5 is returned to ground through R38 and Q5 is driven into saturation. When this occurs a heavy current flows in the secondary of T3.

Each time Q5 is saturated, a pulse of emitter current flows through R35, resulting in a series of voltage drops across this resistor that are averaged by the storage capabilities of C29. The average voltage drop is only about 3 volts, which is not enough to appreciably reduce the peak current through T3, but it is sufficient to insure complete cutoff of Q5 when required. In addition, R35 limits dissipation in Q5. Diode CR5 suppresses the positive inductive spike that occurs at the collector of Q5 when the latter is cut off.

Under steady state conditions, the primary of T3 is switched across 16.5 volts for 1.4 microseconds every time a horizontal timing pulse occurs. The polarity of T3 is such that during the current pulse the junction of the anodes of diode quad Z2 are driven positive and the junction of the cathodes are driven negative. Therefore all of the diodes in the quad conduct very heavily for 1.4 microseconds during every horizontal sync and equalizing pulse. During the 1.4 microsecond interval, the clamp coupling capacitor,

C48 (figure 20) is connected through the low impedance of the conducting quad to the source of the reference clamp bias (TP4).

If there is any error in the potential on the coupling capacitor, C48, due to low frequency distortion such as hum, tilt or a sudden brightness change, C48 will be immediately charged or discharged through the clamp quad to the clamp bias potential. At the end of the 1.4 microsecond interval, the quad is disconnected and C48 passes the next line of video that follows at the conclusion of the sync pulse. As the line of video ends and the next sync pulse occurs, the cycle is repeated and the sync tip level will be once again compared with the reference bias.

The clamp quad is held in cutoff condition by the charge stored in C26 which results in a reverse bias that is almost equal in amplitude to that of the clamp pulse (about 15 volts). Discharge resistor R32 determines the peak on the pulse current when the clamp is operating on a signal that has no error.

The clamp bias is derived from a voltage divider, as described earlier. This divider is bypassed by C27 in series, but in opposite polarity, with C28. This arrangement is necessary because the polarity of the clamp bias may be either positive or negative. The back-to-back connection of the capacitors in conjunction with the negative bias developed across voltage divider R33, R34 insures proper polarizing potential, regardless of the polarity of the clamp bias.

-20 Volts Switch

The purpose of the -20 volts switch circuit is to electronically enable or disable the high (Q4) and the low (Q9) frequency oscillators, according to the mode in which the TR-22 is being operated, or to the function selected by means of S1, the RECORD/R-F COPY switch.

As shown in figure 31, the -20 volts switch consists of two transistors, Q18, a PNP, and Q19, an NPN. When the TR-22 is in the STANDBY, WIND or STOP mode, and the DEMOD switch (on the PLAY control panel) is in PLAY, a positive voltage is applied via the E-to-E control bus to the base of Q18, the PNP. This cuts off Q18 and the collector goes to -26 volts, to which it is connected by a voltage divider comprised of R80 and R81. The base of Q19, the NPN, is connected to the junction of these two resistors, therefore, it too is cut off since the base voltage (-26 volts) is now more negative than that on the emitter (-20 volts). With Q19 cut off, the -20 volts supply to the high and the low frequency

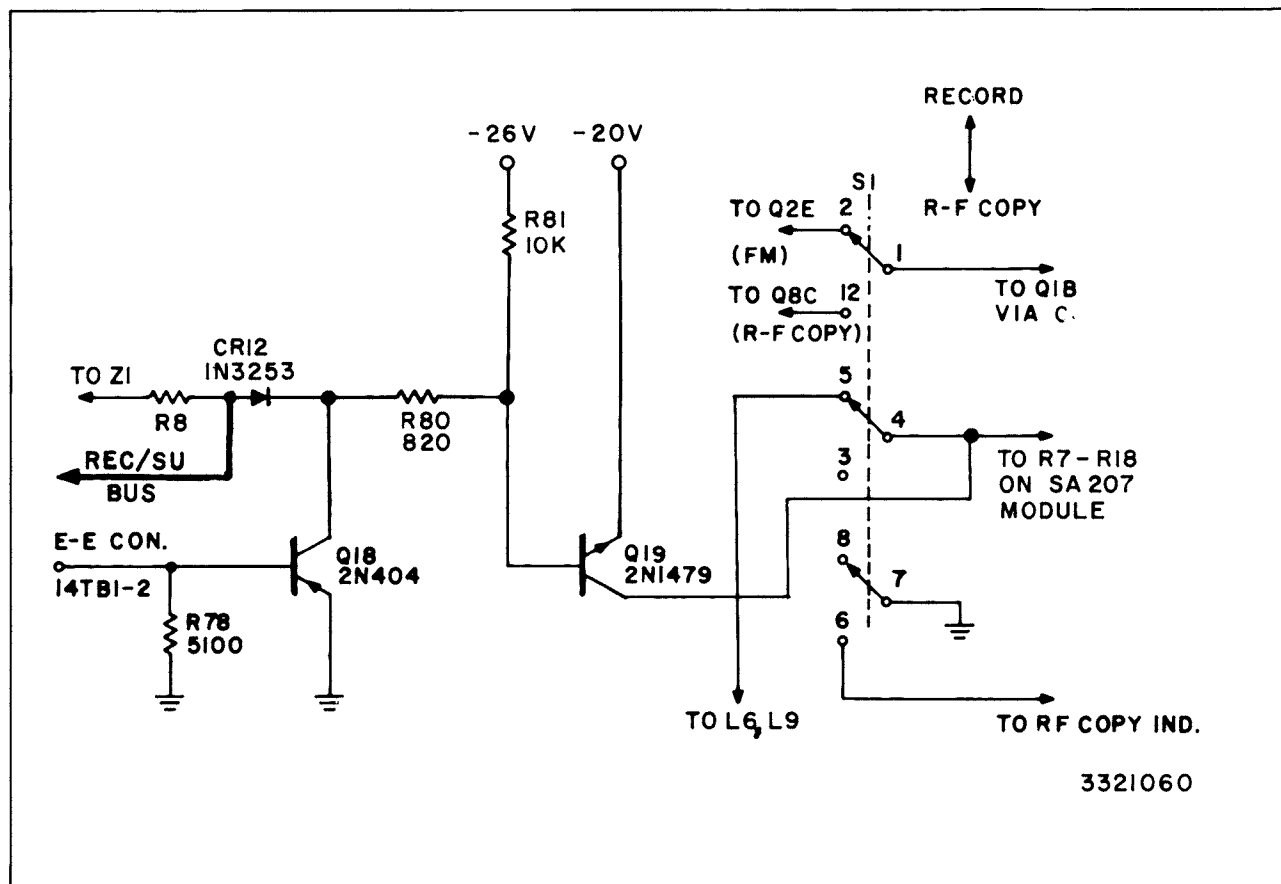


Figure 31—20 Volt Switch

oscillator circuits is opened. When the DEMOD switch is in MOD, a negative voltage is fed via the E-E control bus to the base of Q18 and Q18 saturates. With B18 saturated, R80 is grounded and the voltage developed across R80 is applied to the base of Q19. Since this voltage is positive with respect to the -20 volts on the emitter of Q19, the latter is driven into saturation, closing the -20 volts supply circuit to the high and the low frequency oscillator stages.

When the TR-22 is in the PLAY mode, the Modulator is disabled regardless of the function (PLAY or MOD) selected by the DEMOD switch.

When the RECORD or SETUP mode is selected, the E-to-E control bus is bypassed and Q18 has no part in the operation of the -20 volt switch. In this mode, the RECORD/SETUP control bus is grounded, and current flows through the voltage divider consisting of R80 and R81. The voltage at the junction R80 and R81 appears on the base of Q19, and since this voltage is positive with respect to the voltage on the emitter, Q19 is driven into saturation. When this occurs, -20 volts is applied to the high and the low

frequency oscillator circuits.

When the TR-22 is in the RECORD or SETUP modes, the DEMOD switch is not effective.

The positive dc operating voltage (+20 volts) is developed across Zener diode CR11, which in conjunction with R77 forms a voltage divider across the +70 volt bus. Diode CR11 serves as a shunt-connected regulator.

ADJUSTMENTS

Instructions for aligning the video amplifier, Q16, Q17, the FM amplifier, Q3, and the high and low frequency oscillators, Q4 and Q9, respectively, are given in the procedure below. The adjustments covered in this procedure are not part of routine maintenance and should be performed only if a component affecting response is replaced in one of these stages, or if for some other reason realignment of a stage becomes necessary. When such is the case, refer to that part of the procedure appropriate to the stage requiring realignment.

Video Amplifier Alignment

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) including dual trace plug-in unit and low capacity probes.

Sweep generator with good response to 10 mc.

4700 ohm resistor.

75 ohm resistor.

1. Place the EQUIPMENT POWER circuit breaker in the OFF position.

2. (a) Remove the Modulator (module 207B-S) from the TR-22.

(b) Disconnect C51, a 22pF capacitor between the base of Q10 and the emitter of Q11.

(c) Refer to the figure 32, and disable clamp Z2 by disconnecting the leads marked "X"; then connect the 4700 ohm resistor across the terminals shown in the sketch.

(d) Mount the modulator in an extender and insert it in the TR-22.

3. Disconnect the video coaxial lead from terminals 17-1 on connector 207-J1 on the rear of the TR-22; then connect the 75 ohm resistor across these two terminals.

4. Turn the EQUIPMENT POWER circuit breaker ON; place the TR-22 in the E-E mode of operation; switch the STD selector on the FM Standards (module 205A) to MONO, and switch the RECORD R-F

COPY selector on the Modulator to RECORD.

5. Connect the output of the sweep generator to terminals 17-1 on connector 207-J. Set the sweep rate for 0 to 10 mc and adjust the gain of the generator to obtain an output not in excess of .4 volt peak-to-peak.

6. Connect one oscilloscope probe to Q17 base and the other to Q10 emitter. While observing the signal at these two points, adjust the core of L12 to obtain optimum response. Some discontinuity will appear in the sweep envelope near 6.8 mc, but up to this point, the response should be flat $\pm 5\%$. At 4 mc the response will exhibit a 1 db rise when C51 is reconnected.

7. Disconnect the 4700 and 75 ohm resistors and restore all connections for normal operation.

FM Amplifier Alignment

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) including dual trace plug-in unit and low capacity probes.

Sweep generator with good response to 20 mc and a 75 ohm terminating resistor.

1. Place the EQUIPMENT POWER circuit breaker in the OFF position.

2. (a) Remove the Modulator (module 207B-S) from the TR-22.

(b). Disconnect C15 from T1-4; connect the 75 ohm termination resistor between the free end of C15 and ground.

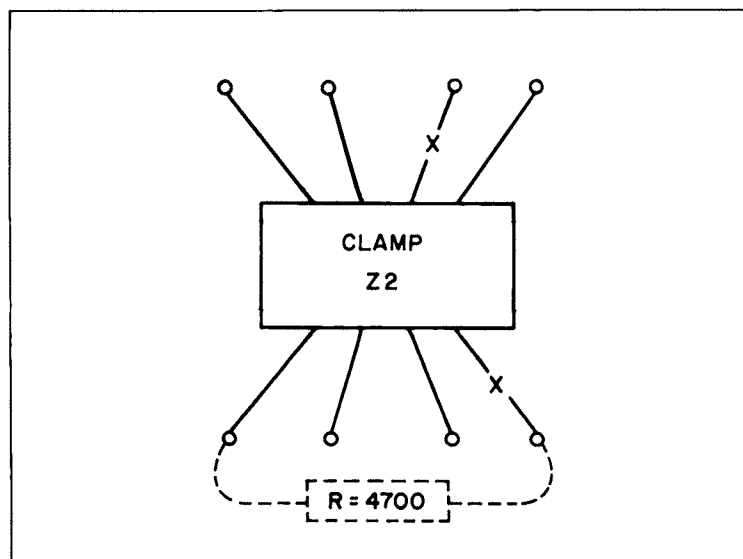


Figure 32—Test Setup

(c) Mount the Modulator in an extender and insert it in the TR-22.

3. Turn the EQUIPMENT POWER circuit breaker ON; place the TR-22 in the E-E mode of operation; switch the STD selector on the FM Standards (module 205A) to MONO, and switch the RECORD/R-F COPY selector on the Modulator to RECORD.

4. Connect the output of the sweep generator across the 75 ohm termination on C15. Set the sweep rate for 0 to 20 mc and adjust the gain of the generator to obtain an output of 1 volt peak-to-peak.

5. Connect one oscilloscope probe to the input side of C15 and the other to Q1 emitter. While observing the signal at these two points, adjust the core of L5 for a response that is flat within $\pm 5\%$ up to 15 mc.

6. Disconnect the 75 ohm resistor and restore all connections for normal operation.

High and Low Frequency Oscillator Alignment

Recommended Test Equipment

VTVM.

Grid dip meter or sensitive absorption wavemeter.

1. Apply a composite video signal to the input of the TR-22.

2. Set the CARRIER FREQ VERNIER (R30), on the front panel of the Modulator, to center of range.

3. Place the EQUIPMENT POWER circuit breaker in the OFF position.

4. Carefully remove the video coaxial lead from terminals 17-1 of connector 207-J1 on the rear of the TR-22.

5. (a) Remove the FM Standards (module 205A) from the TR-22.

(b) Locate the SYNC TIP FREQ PRESET potentiometer designated REF 1, which is one of four on the underside of the module board near the rear. REF 2 and REF 4 are mounted directly on the board. REF 1 and REF 3 are mounted on top of REF 2 and REF 4, respectively.

(c) Mount the FM Standards in an extender and insert it in the TR-22.

(d) Connect the VTVM to TP4 (CLAMP BIAS) on the front of the Modulator.

(e) Place the EQUIPMENT POWER circuit breaker in the ON position.

(f) Observe the VTVM and adjust REF 1 for zero volts.

(g) Place the EQUIPMENT POWER circuit breaker in the OFF position.

(h) Disconnect the VTVM and replace the FM Standards in the TR-22.

6. (a) Mount the Modulator in an extender and insert it in the TR-22.

(b) Place the EQUIPMENT POWER circuit breaker in the ON position.

(c) Set the grid dip meter or absorption wavemeter to 60 mc and couple it loosely to the high frequency oscillator coil, L7.

(d) Adjust the core of L7 until the oscillator is tuned to 60 mc.

(e) Set the meter to 55.72 mc and couple it loosely to the low frequency oscillator coil, L10. Adjust the core of L10 until the oscillator is tuned to approximately 55.72 mc. Final tuning will be accomplished in step 9.

7. (a) Place the EQUIPMENT POWER circuit breaker in the OFF position.

(b) Re-connect the video coaxial lead to terminals 17-1 of connector 207-J1.

(c) Place the EQUIPMENT POWER circuit breaker in the ON position.

8. Press the VID and VER buttons on the CRO monitor; press the DEMOD OUT button below the CRO monitor to select the signal for display.

9. (a) Press and release the FM REF button on the FM Reference (module 302A) several times while observing the CRO. Each time the button is pressed, either the sync tip reference marker (A, figure 33) or the peak white reference marker (B, figure 33) will appear in the vertical blanking area between the two fields.

(b) Release and press the FM REF button until the sync tip reference marker appears, then hold the button down. While observing the CRO, readjust the core of L10 until the tip of sync is as close as possible to the zero axis of the reference marker.

10. Remove the extender and replace the Modulator in the TR-22.

11. Again observe the sync tip on the CRO, as described in step 9, and if there is a slight shift indi-

cated in the sync tip, make a touch-up adjustment with the CARRIER FREQ VERNIER to restore it to the proper level.

NOTE

In figure 33, waveforms A and B show the result of correct oscillator alignment and waveform C that of improper alignment. When the oscillators are correctly aligned, the tip of sync is on the same level as the zero axis of the sync tip reference marker (see A). Slight misalignment will result in a small displacement of the reference marker which may be corrected by the CARRIER FREQ VERNIER. The result of severe misalignment is shown in C. When this condition exists, the deviation band may be moved so far up the frequency spectrum that the sync tip reference is driven off the bottom of the CRO display. Further evidence of this is an erratic up and down motion of the signal display on the CRO as the FM REF button is pressed and released. In this case the sync tip is so far from the correct frequency that it may be beyond the range of the CARRIER FREQ VERNIER and needs to be restored by realigning the low frequency oscillator.

RECORD AMPLIFIERS (Modules 211A, 212A, 213A, 214A)

There are four identical Record Amplifiers, one for each record channel. The purpose of the Record Amplifiers is to provide the correct amount of delay to offset any irregularities in head quadrature and to amplify the FM signals driving the magnetic heads,

during the recording process.

From a functional standpoint, the circuitry of the Record Amplifiers can be divided into two sections. One section contains the delay circuits and the other contains the amplifier circuits. Accordingly, each section will be considered separately in the following description, and since all four modules are identical, only one will be discussed.

DELAY SECTION

To obtain optimum results when recording, the effective spacing between the four magnetic heads on the headwheel theoretically should be exactly ninety degrees. The effective spacing can be adjusted either mechanically or electrically, and both of these methods are employed on the TR-22. During the manufacturing process, the heads are mechanically spaced on the headwheel to within a few seconds of the correct ninety degree position. Then, in the TR-22, final adjustments are made electrically by means of the adjustable delays to compensate for the remaining error in head quadrature.

To illustrate the function of the delay line, a headwheel with the No. 2 head incorrectly positioned by an angle equal to "x" seconds is shown in figure 34.

A recording made with this headwheel and then played back by another with the heads perfectly

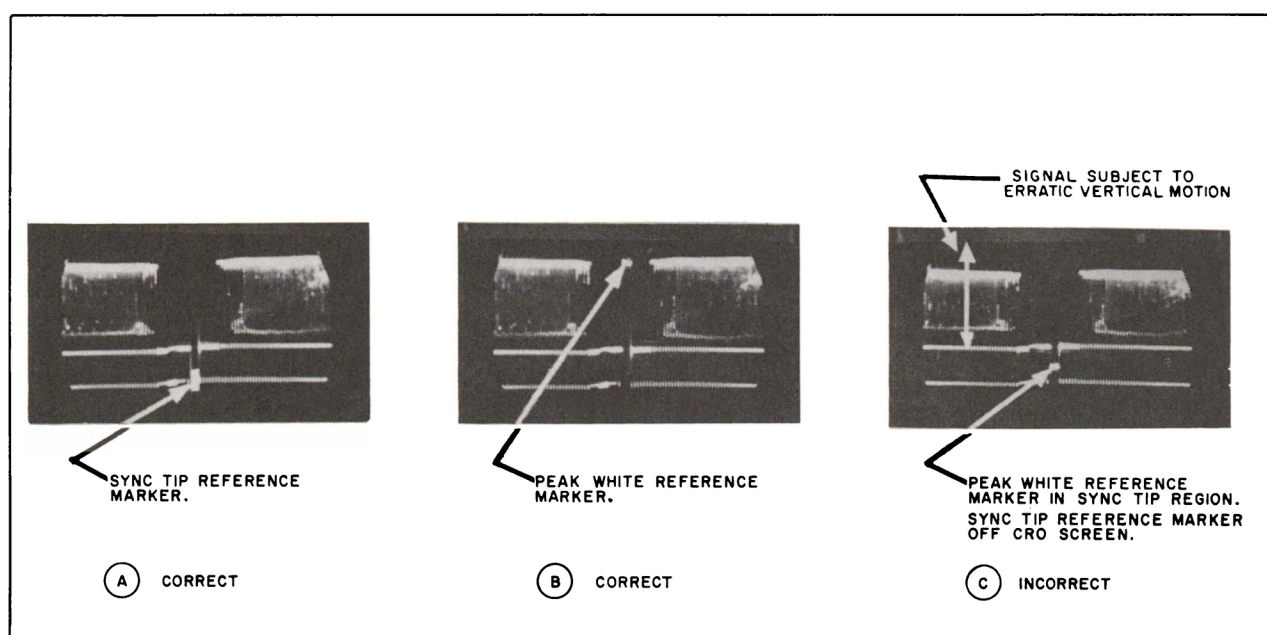


Figure 33—Modulator Frequency Adjustment Waveform

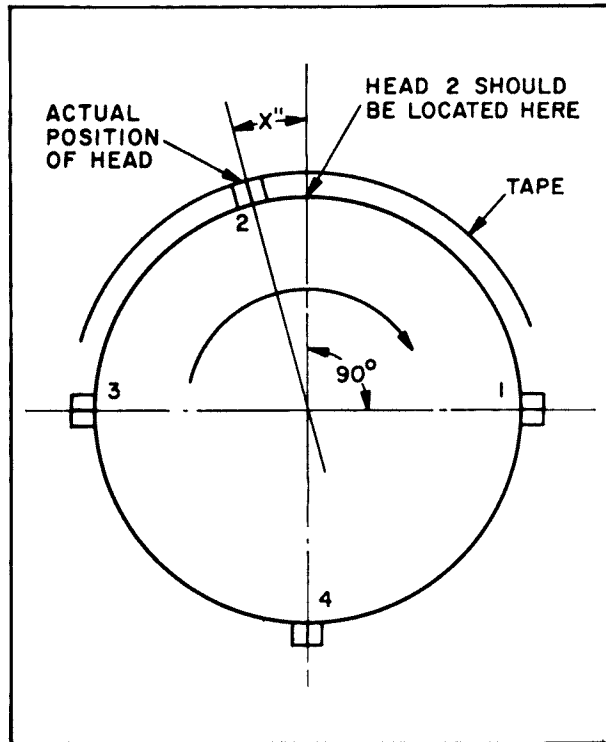


Figure 34—Video Head Placement Showing Head No. 2 Out of Quadrature

aligned will produce a picture with horizontal displacement as shown in figure 35. Because the angular displacement of head No. 2 is in the direction of counter rotation to its proper position, the information will be recorded late in time. However, if the signal feeding the late head is advanced in time by an amount equal to the mechanical displacement, the recorded information will appear in the proper position on the tape. This is accomplished electrically by means of the tapped delay line.

When the information is being recorded the FM signal from the appropriate FM output line driver on the Modulator (module 207B-S) is fed to the input of the delay section (see figure 36). The incoming signal is coupled through C100 to the base of Q100, an emitter follower. The input is terminated in 75 ohms by R100. From the emitter of Q100, the signal is fed through R119, a parasitic suppressor, to the base of Q101, the delay line driver. The output on the collector of Q101 is fed via the delay switch, S2, to the delay line, L100.

The delay network consists of ten sections with each section connected to a tap switch. Each section of the line provides a delay of approximately .015 microseconds, which is equivalent to approximately 5 seconds of arc on the headwheel. Selection of the

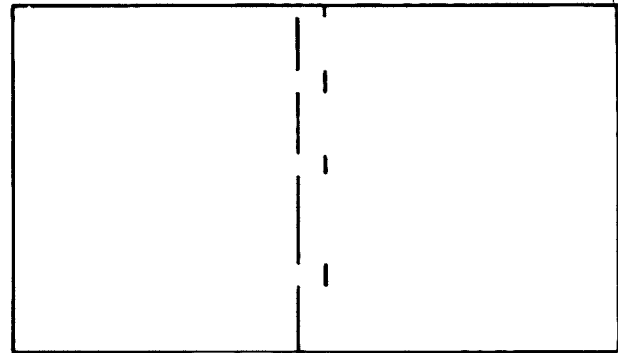


Figure 35—Vertical Line on TV Raster Showing Horizontal Displacement of Head No. 2

desired delay increment is by means of S2 which is controlled from the front panel of the module. The delay selector dial is calibrated so that zero switch position represents the mid-point of the delay line. At this setting, 50% of the delay available is in the circuit. To the right of zero, the dial has the numerals from 1 to 5, over which is a plus sign to indicate that turning the switch in this direction increases the amount of delay. Similarly to the left of zero are numerals from 1 to 5 over which is a minus sign to show a decrease in the amount of delay. Such an arrangement makes it possible to delay or, in effect, advance the signal ultimately driving the heads. Each end of the delay line is terminated in 46.4 ohms; at the input by R105 and at the output by the 38.3 ohms of R108 in combination with the emitter impedance of Q102.

The output of the delay line is coupled through C114 and R108 to the emitter of Q102, a common base amplifier. This stage has a gain of slightly more than 3 and provides virtually all of the signal amplification. Nominal value of the signal initially applied to the base of the input transistor, Q100, is .6 volt peak-to-peak. Thus the output signal on the collector of Q102 is approximately 2 volts peak-to-peak. From the collector of Q102, the signal is dc coupled to the base of Q103. This transistor together with Q104, an-

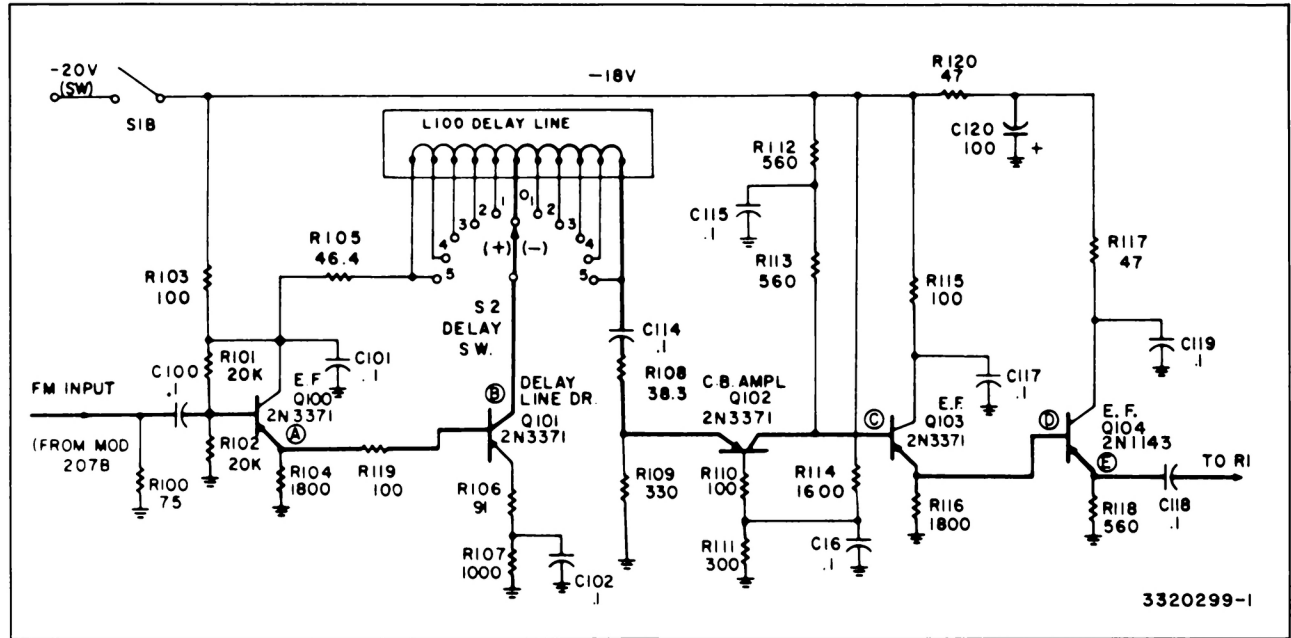
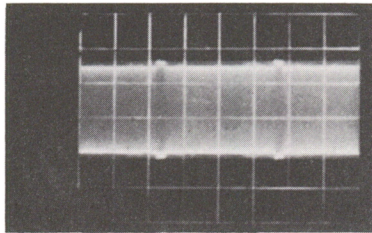
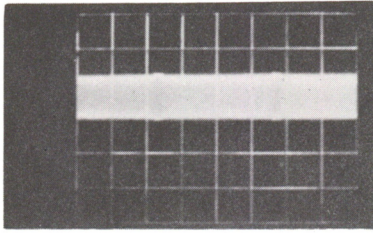


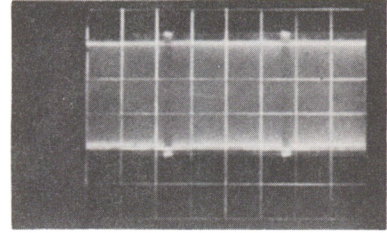
Figure 36—Delay Circuits, Record Amplifier Module



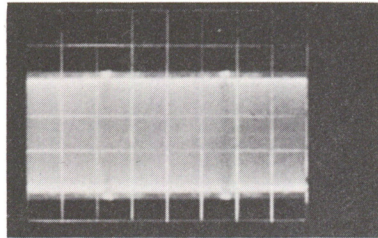
A. Q100 emitter, 5 ms/cm, .2v/cm



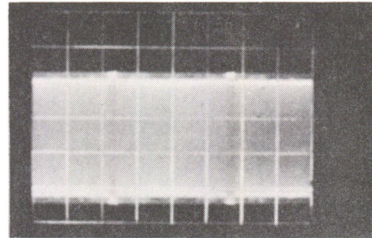
B. Q101 collector, 5 ms/cm, .1v/cm



C. Q103 base, 5 ms/cm, .5v/cm



D. Q104 base, 5 ms/cm, .5v/cm



E. Q104 emitter, 5 ms/cm, .5v/cm

Figure 37—Typical Waveforms; Delay Circuits, Record Amplifier Module

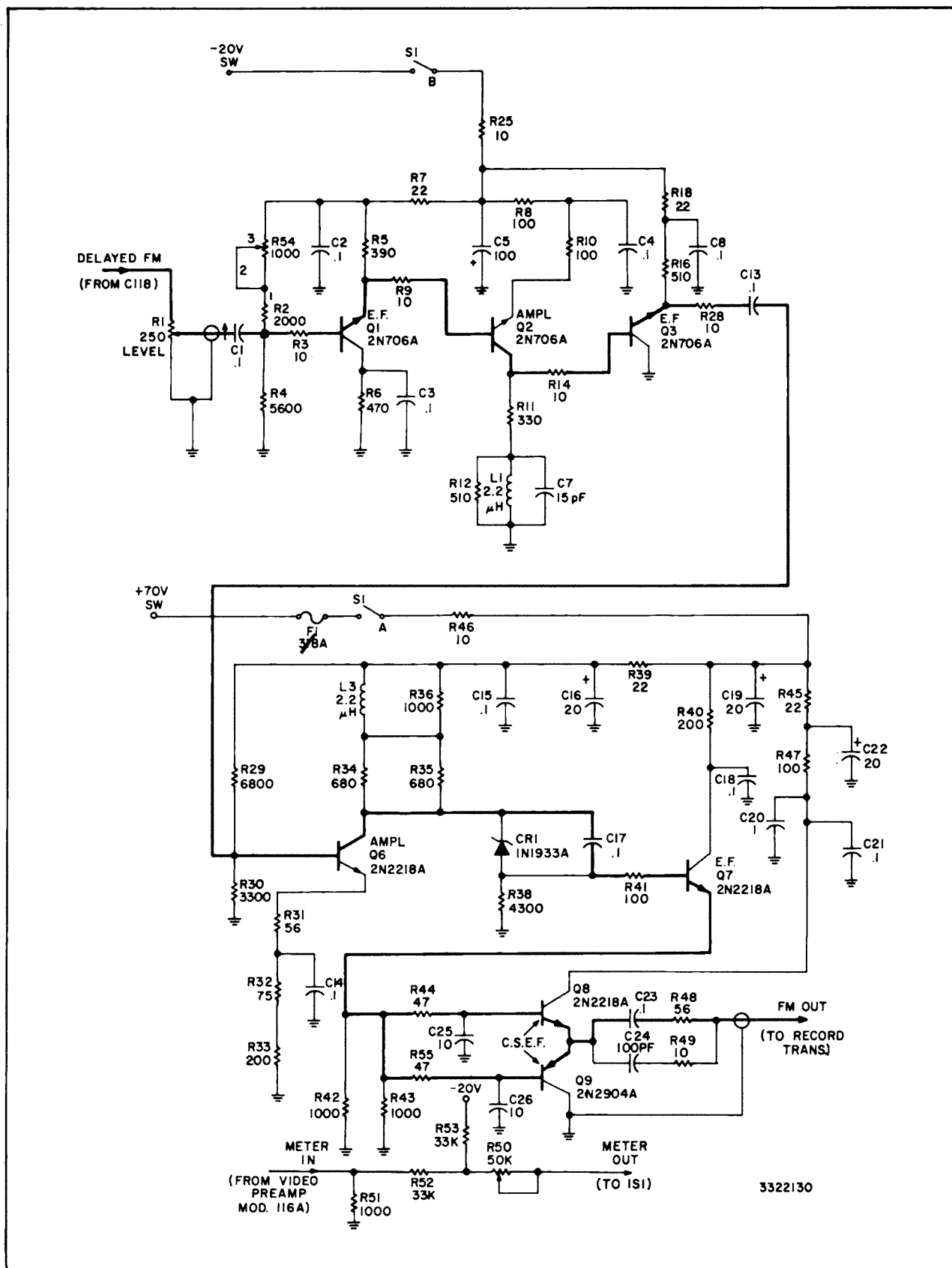


Figure 38—Amplifier Circuits, Record Amplifier Module

other emitter follower, are connected to form a direct coupled cascade amplifier. This configuration isolates Q102 from the succeeding input circuit of the amplifier section. The gain of the cascade amplifier is unity; therefore the signal available on the emitter of Q104 is of the order of 2 volts peak-to-peak. From the emitter of Q104, the signal is fed through C118 to the input stage of the amplifier section.

AMPLIFIER SECTION

The 2-volt output of the delay section is coupled through C118, potentiometer R1, and C1 to the base of Q1, an emitter follower (see figure 38). Potentiometer R1 is a LEVEL control on the front panel. This control permits the amplitude of the record current to be adjusted to the optimum value for driving the heads. From the emitter of Q1, the signal is fed to the base Q2, an amplifier with a gain of about 3. A shunt peaking coil, L1, in series with the collector load provides high frequency compensation for this stage. The output on the collector of Q2 is approximately 5.5 volts and this is fed to the base of Q3, an emitter follower with unity gain. From the emitter of Q3, the signal is coupled through C13 to the base of Q6.

The gain of Q6 is almost 4, thus the signal on the collector is approximately 20 volts peak-to-peak. This stage also employs shunt peaking for high frequency compensation. Coil L3 in series with the collector load serves this purpose. The output on the collector of Q7 is fed through C17 to the base of Q7, an emitter follower. Zener diode CR1 maintains the bias on the base of Q7 at a potential that is 12 volts positive with respect to the dc voltage on the collector Q6. From the emitter of Q7, the signal is fed to the complementary symmetry amplifier, Q8, Q9.

The complementary symmetry stage is operated similar to a class B amplifier, with Q8 conducting on the positive half cycles and Q9 conducting on the negative half cycles. The output from the complementary symmetry amplifier is coupled through C23 and R48 to the primary of the appropriate record transformer on the Video Preamplifier (module 116A). Capacitor C24 and R49, in parallel with the output coupling components form a frequency compensation network to compensate for the response of the record transformer and the head.

The four 10-ohm resistors R3, R9, R14 and R28; the one 100-ohm resistor, R41; and the two R-C networks, R44, C25 and R55, C26, are used in the coupling circuits between stages to eliminate parasitic oscillations.

Potentiometer R50 is an internal control used to calibrate the head current metering circuit on the Video Preamplifier (module 116A) so that the reading on the multimeter, 5M1, will be correct.

The dc operating voltages, +70v switched and -20 switched, are applied to the Record Amplifier when the ON-OFF toggle switch, S1, on the front panel is in the ON position. Between the +70v contact on the input side of S1 and the incoming 70v line, there is a $\frac{3}{8}$ ampere fuse (F1). The ON-OFF switch permits the head currents to be turned off when making tests or adjustments. For example, if adjustments are being made to the Headwheel Servo System and the headwheel is not rotating with the TR-22 in the Record or Setup modes, the ON-OFF switch on all four Record Amplifiers should be switched to the OFF position. Applying record currents with the headwheel stationary could possibly cause damage to the headwheel slip rings.

The +70v and the -20v are supplied from the Regulator (module 329A). These voltages are present only when the TR-22 is in Record or Setup modes of operation; in other modes these voltages are switched off. The Regulator is interlocked with modules 313 Tonewheel Processor, 314A Tonewheel Servo, 315 Headwheel Modulator, 322 Capstan Oscillator, and 331-334 Headwheel/Capstan Power Amplifiers. If any of these modules are removed from the TR-22, the +70v and -20v circuits are opened. (For a detailed description of the module interlock circuitry, see INTERLOCK SYSTEMS in the CONTROL AND POWER SUPPLY SYSTEMS instruction book, IB-31623.)

VIDEO PREAMPLIFIER (Module 116A)

The primary purpose of the Video Preamplifier is to provide a small measure of current amplification to the signal from the heads during playback and to furnish the proper impedance match between the heads and the Playback Amplifiers.

There are four preamplifier circuits, one for each playback channel. The video Preamplifier module also contains a head current metering and indicator circuit for each of the four record channels.

The four preamplifiers and the four current sampling circuits are wired on two boards, with channels 1 and 3 on one board and channels 2 and 4 on the other board. The boards are assembled back-to-back to form the module. The module is enclosed in a metal shield, and it is mounted in a recess directly behind the headwheel panel on the tape transport.

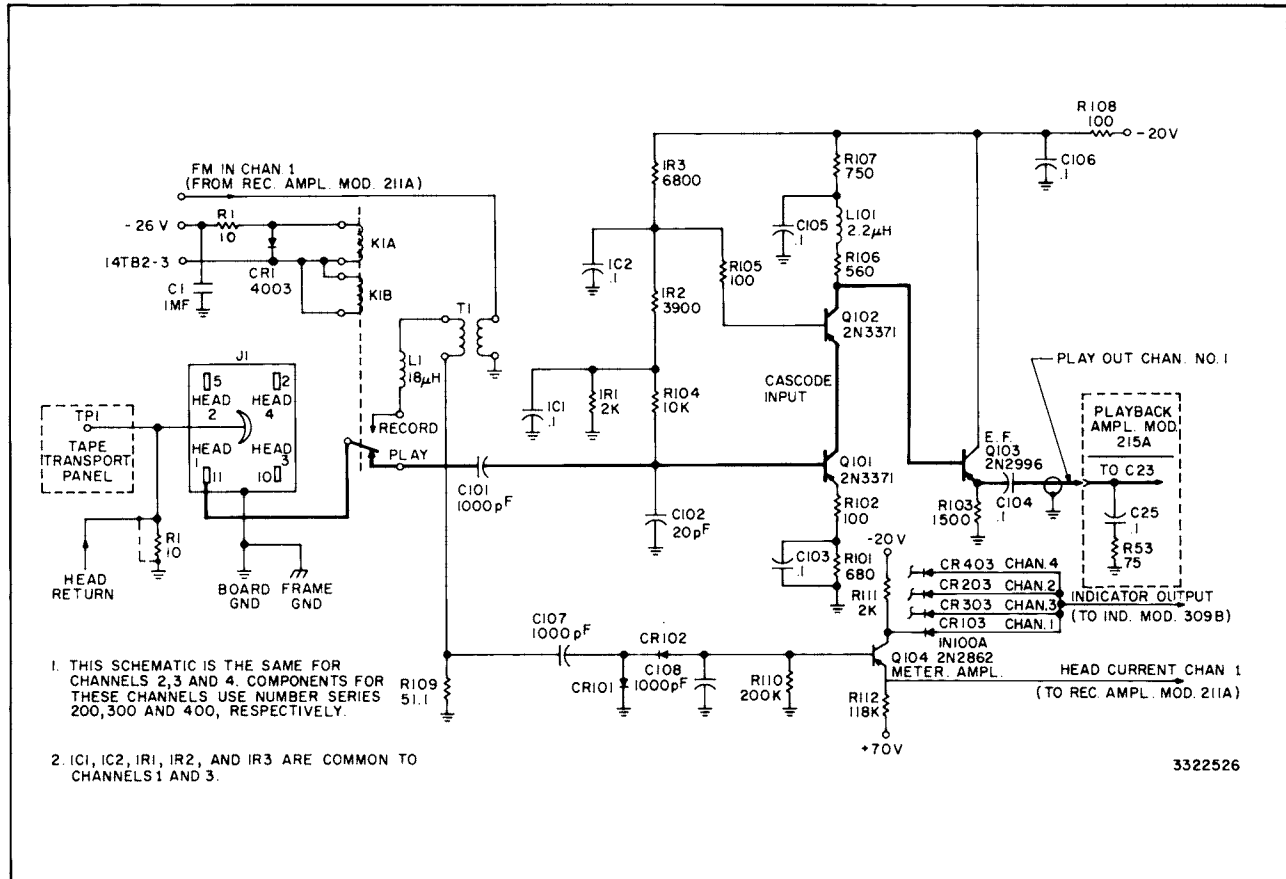


Figure 39—Video Preamplifier Circuit

Each preamplifier circuit consists of a cascade input and an emitter follower output and each metering circuit employs a single transistor. Components in number series 100 (i.e., Q101, R101) refer to channel 1. Components in number series 200 refer to channel 2 and so forth. Where a component has a numerical prefix, such as 1R1, or 1C1, it is common to channels 1 and 3. Similar components in channels 2 and 4 have prefix 2.

PREAMPLIFIER CIRCUIT

Since the circuits for all four channels are electrically identical only one is described here. (Refer to the simplified schematic, figure 39.)

In the playback mode, low level signals from the appropriate head are fed through K1 and C101 to the base of Q101. Transistors Q101 and Q102 are connected as a cascade input amplifier. The advantage of this type of circuit in dealing with low level signals is that most of the noise is eliminated even though the signal is amplified. Virtually all of the amplification is provided by Q102. Most of the noise inherent in the circuit is confined to Q101; and since this tran-

sistor furnishes very little amplification, the amount of noise in the signal subsequently amplified by Q102 is very slight.

Transistor Q102 serves as the load in the collector circuit of Q101, with the output of the latter feeding directly into the emitter of Q102. The impedance presented by Q102 to the flow of signal current in the collector of Q101 is negligible, therefore the voltage available at the emitter of Q102 is very slight. However, the output of the cascade amplifier is taken across the collector load (R106) of Q102.

The impedance of the load is such that the amplitude of the output signal is suitable for ultimately driving the output line.

A shunt peaking coil, L101, in the collector of Q102 provides high frequency compensation.

Bias voltage on the bases of Q101 and Q102 is developed across the voltage divider consisting of 1R1, 1R2, and 1R3 connected across -20 volts. Capacitor C102 is the head resonating capacitor.

The signal on the collector of Q102 is direct coupled to Q103, an emitter follower. The output on

the emitter of Q103 is coupled through C104 to the input of Playback Amplifier module 215A. Emitter follower coupling prevents loading of the cascade amplifier by the input stage of the Playback Amplifier.

METERING AND INDICATOR CURRENT SAMPLING CIRCUIT

The metering and the indicator current circuits of all four channels are similar, therefore only the circuit pertaining to the head current for channel number one will be described (see figure 40).

In the record mode, the amplified FM record current from Record Amplifier module 211A is fed to head number one through transistor T1, of Pre-Amplifier 116A. The FM signal is sampled from the secondary of T1 and fed through a peak-to-peak detector, CR101, CR102, to the base of Q104, the meter amplifier. This stage furnishes two rectified outputs, one for the metering circuit and the other for the indicator circuit.

The metering current is taken off the emitter of Q104 and returned to Record Amplifier module 211A, passing through two resistors on this module, R52 and potentiometer R50. The latter is an internal control that is used to calibrate the metering circuit so that the reading on the multimeter, 5M1, will be correct. From R50 the current goes to the head current selector pushbutton, H1, of meter switch 1S1. When the contacts of the H1 are closed, the current is fed to the multimeter, 5M1, which provides an indication of the record current for channel one.

In the same manner, the record currents for channels 2, 3, and 4 are selected individually by pushbuttons H2, H3, and H4, respectively.

The indicator current is taken off the collector of Q104. However, unlike the meter current output where the record current for each channel is read separately on the meter, the indicator current from the four channels is combined in a single output. Thus the magnitude of the signal current applied to the differential switch, Q1, Q2, in the Indicator (module 309B) represents the sum of the four indicator currents.

Diode CR103, in series with the collector of Q103, is a steering diode. The purpose of CR103 is to isolate the collector of Q104 from the indicator current output of the other three channels. Each of the other channels is isolated in a similar manner.

PLAYBACK AMPLIFIERS (Modules 215A, 216A, 217A, 218A)

A Playback Amplifier is used in each of the four playback channels to amplify the output of the four video preamplifiers and to enable the correct amount of delay to be inserted to compensate for errors in head quadrature. Quadrature errors are due to the magnetic heads not being exactly ninety degrees apart around the periphery of the headwheel, or to tapes that were recorded with improper headwheel quadrature. Equalization is also provided so that the response of the FM playback system can be adjusted to compensate for slight differences in the frequency response of the individual heads.

Like the Record Amplifiers (modules 211A through 214A), the Playback Amplifiers consist of two sections, the amplifier circuits proper (figure 41), and the delay circuits (figure 42). However, in the case of the Playback Amplifier, the delay section follows the amplifier section. Since the operation and configuration of the delay circuits in the Playback Amplifiers are similar to the counterparts in the Record Amplifiers, they will not be covered as part of the Playback Amplifier description. For a discussion of the purpose and operation of the delay circuits, refer to the Delay Section under the Record Amplifiers (modules 211A through 214A) description, elsewhere in this book.

Since all four Playback Amplifier modules are identical, only one will be discussed.

AMPLIFIER SECTION

In the PLAY mode the signal from the appropriate preamplifier channel on the Video Preamplifier (module 116A) is coupled through C23 to the base of amplifier Q10. (See figure 41.) The signal is terminated in 75 ohms at the input by R53. Variable peaking coil L2 in series with the collector load, R48, provides high frequency shunt compensation. The response of Q10 is adjusted at the factory, therefore the setting of L2 should not be disturbed unless a component affecting the response of this stage is replaced. The output on the collector of Q10 is coupled through C21 to the base of amplifier Q9.

Amplifier Q9 contains a variable gain circuit which is controlled by the sensitivity gain circuit which is controlled by the sensitivity switch (SENS SW), S2 in the emitter circuit. The SENS SW switch permits the gain of this stage to be changed by a fixed amount to accommodate the playback current require-

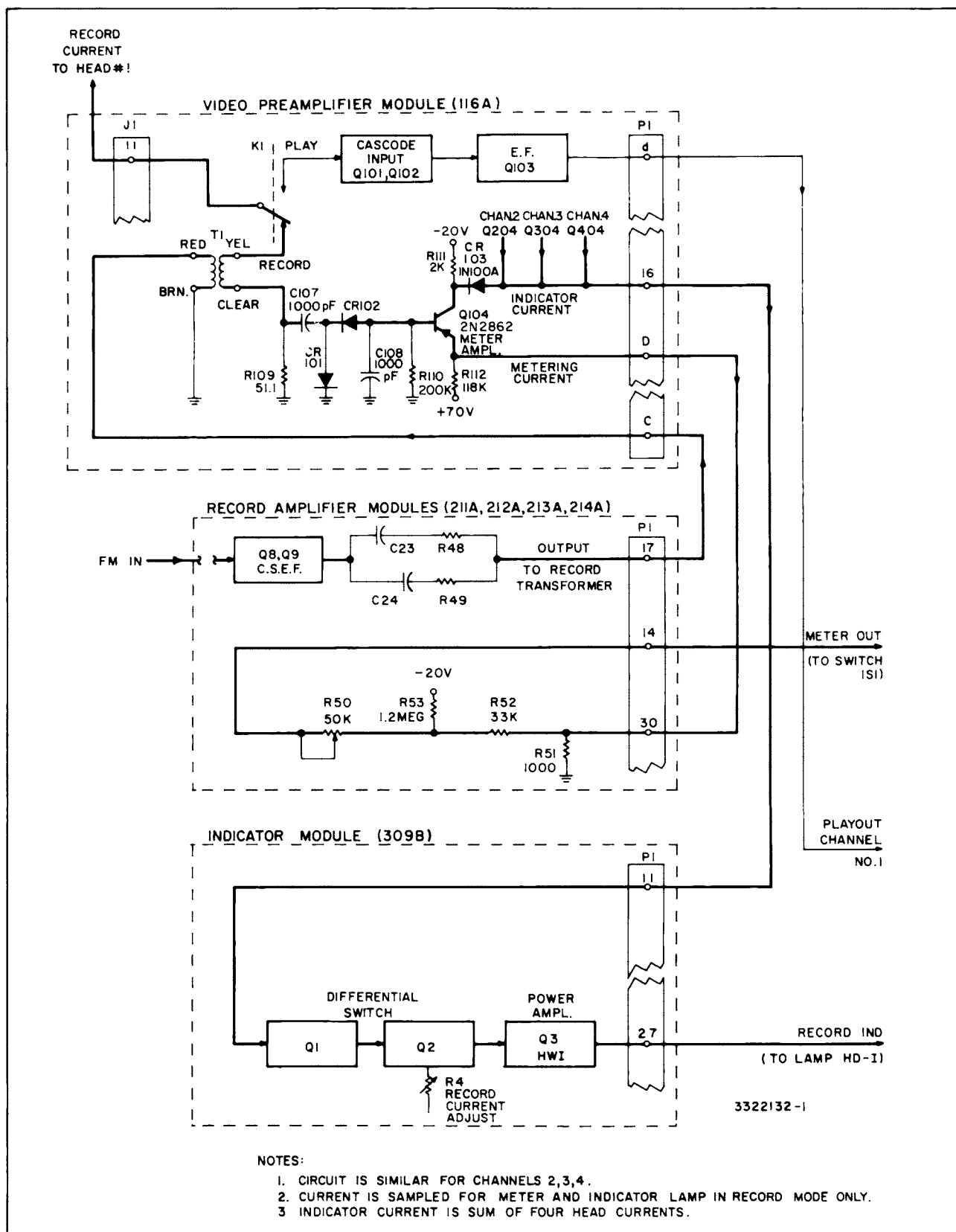


Figure 40—Record Current Metering and Indicator Circuits

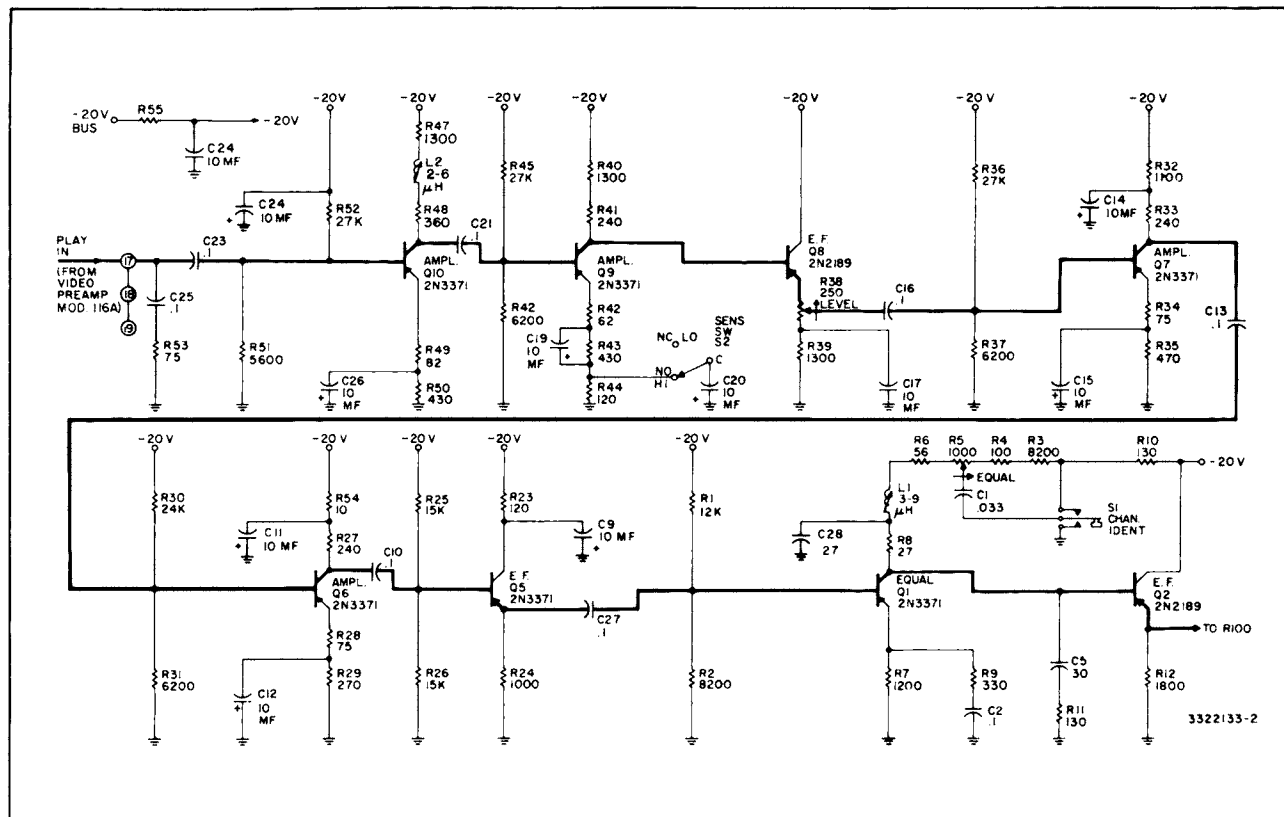


Figure 41—Amplifier Circuits, Playback Amplifier Module

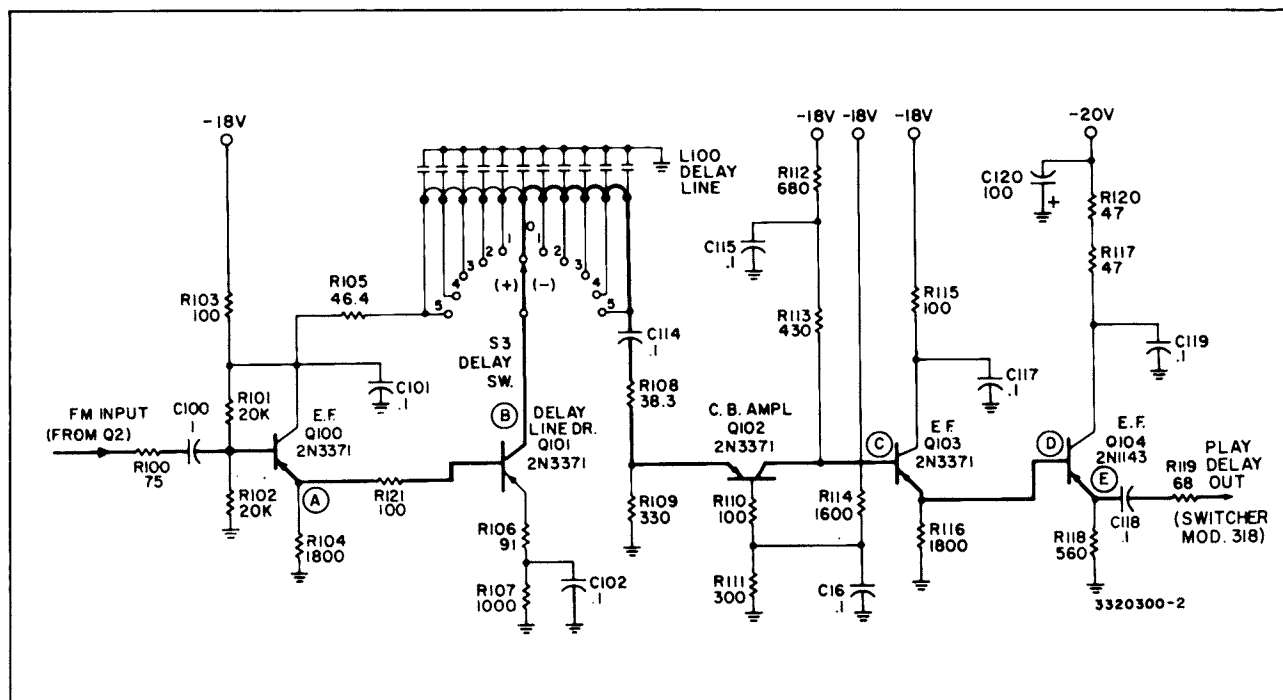


Figure 42—Delay Circuits, Playback Amplifier Module

ments of the headwheel panel in use. With S2 in high (NO) position, as shown in figure 41, C20 is switched into the emitter circuit bypassing R44 so that maximum gain is obtained. When S2 is in the low (NC) position C20 is disconnected from the emitter and the degeneration introduced into the emitter by R44 reduces the gain of this stage 8 db. The SENS SW is an internal control.

The output on the collector of Q9 is direct coupled to the base of Q8, an emitter follower, which isolates Q9 from the succeeding amplifiers. The variable resistor, R38, in the emitter enables the FM level of each Playback Amplifier to be set individually so that the output of all four can be adjusted for equal amplitude. This control is a front panel screwdriver adjustment designated LEVEL. From the emitter of Q8, the signal is coupled through C16 to the base of amplifier Q7.

The output on the collector of Q7 is coupled through C13 to the base of Q6, another amplifier. These two transistors form a cascade amplifier. This configuration increases the amplitude of the signal to the desired level without sacrificing bandwidth. From the collector of Q6 the signal is coupled through C10 to the base of Q5, an emitter follower. Transistor

Q5 isolates Q6 from the loading effects of the next stage, Q1. The output on the emitter of Q5 is coupled through C27 to the base of Q1, the equalizer.

The equalizer, Q1, is a high frequency amplifier employing shunt compensation, which is provided by variable peaking coil L1 in the collector circuit. Unless a component affecting the response of this stage is replaced, the setting of L1 should not be disturbed. The EQUAL potentiometer, R4, in the collector circuit is used to compensate for the difference in the frequency response of the individual heads. Turning R5 counterclockwise increases the response of the high frequency end of the FM band, which represents an increase in the response of the low end of the video band. The opposite occurs when R5 is turned clockwise. The response of the low end of the FM band is increased, representing an increase in the high frequency end of the video band. Optimum response is usually found with the pointer of the EQUAL control between 2 and 3 on the dial. The EQUAL control is on the front panel.

A pushbutton switch, S1, is located in the collector circuit of Q1 so that the individual playback channels can be identified. The switch control, which is on the front panel, is designated CH ID. When the switch

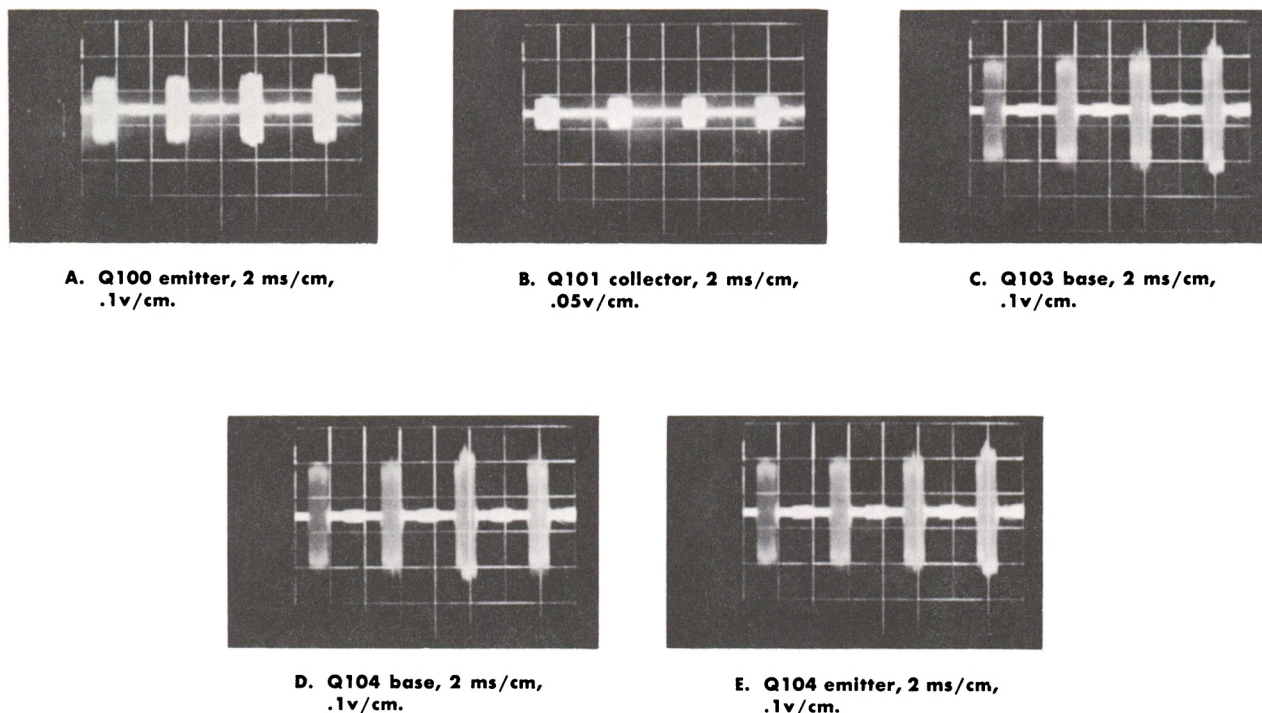


Figure 43—Typical Waveforms; Delay Circuits Playback Amplifier Module

is pressed, the circuit parameters are changed. This will be evident when observed on a monitor, appearing as a change in the frequency response of a particular head. The CH ID switch should not be operated while the TR-22 is on the air, since bands will appear in the picture.

The compensated output from the collector of Q1 is dc coupled to the base of Q2, an emitter follower. From the emitter of Q2, the signal is fed through R100, C100 to the base of Q100, the input stage of the delay section. After passing through the circuits of the delay section, the signal is fed to the FM Switcher (module 318).

ADJUSTMENTS

To check the frequency response and the output level of the Playback Amplifiers, follow the procedure outlined below.

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) with a high gain amplifier and a low capacity probe.

Video sweep generator capable of sweeping 0 to 15 mc.

Calibrated rf attenuator network if sweep generator is not equipped with attenuator.

Module Extender.

Test Connector, RCA Stock No. 205330 or Amphenol No. 26-151.

1. Remove the power from the TR-22 by placing the EQUIPMENT POWER circuit breaker in the OFF position.

2. (a) Remove the Playback Amplifier to be swept (see chart, below) from the TR-22.

(b) Disconnect the coaxial input signal lead from pin P1-17.

(c) Check the position of the HI-LO sensitivity switch, S2. This is an internal control and for the first part of the response check, it should be in LO.

(d) Mount the Playback Amplifier in an extender and insert it in the TR-22.

3. (a) Connect the output of the sweep generator, using RG-59U coaxial cable, to the attenuator. Using the same type of cable, connect the output of the attenuator to the junction of C23, C25.

(b) Connect the low capacity probe from the oscilloscope to the junction of C27, R24.

4. Place the EQUIPMENT POWER circuit breaker in the ON position.

5. Set the sweep rate on the generator for 0 to 12 mc. Adjust the output of the sweep generator in combination with the attenuator to obtain a 50 mv signal at the junction of C23, C25.

6. Observe the oscilloscope and adjust coil L2 to obtain the flattest response.

7. Place the EQUIPMENT POWER circuit breaker in the OFF position.

8. (a) Disconnect the attenuator lead from the junction of C23, C25, and the oscilloscope probe from the junction of C27, R24.

(b) Restore the HI-LO switch, S2, to its original position.

9. (a) Remove the extender from the TR-22.

(b) Remove the Playback Amplifier from the extender and reconnect the input signal lead to pin P1-17.

(c) Replace the Playback Amplifier in the TR-22.

10. Remove the Headwheel Panel from the Tape Transport Panel and plug the test connector into J1 on the Video Preamplifier. Disconnect the Demodulator (module 203B) from the recorder system by sliding it partly out of its slot.

11. Connect the output of the attenuator to the pin on the test connector corresponding to the channel driving the Playback Amplifier (see chart, below).

NOTE

Keep the ground lead formed by the braid on the signal cable as short as possible, and make certain it is connected firmly to the frame of the TR-22 in close proximity to the test plug. Failure to exercise these precautions may cause the waveform display to appear distorted, resulting in an inaccurate representation of the response characteristics.

<i>Channel No.</i>	<i>Test Connector Pin No.</i>	<i>Playback Amplifier Module No.</i>
1	11	215A
2	5	216A
3	10	217A
4	2	218A

12. Terminate the appropriate input pin on the test connector in 75 ohms. Set the sweep rate on the gen-

erator for 0 to 12 mc. Adjust the output of the generator in combination with the attenuator to provide a 5 mv input signal to the Video Preamplifier. (If the generator is capable of an output of 2.5 volts peak-to-peak, 54 db of attenuation will furnish a 5 mv signal.)

13. Place the EQUIPMENT POWER circuit breaker in the ON position.

14. Connect the low capacity probe from the oscilloscope to the test point on the Playback Amplifier associated with the channel being swept.

15. Adjust the EQUAL control, R4, to obtain a flat response. This is usually obtained with pointer of the control knob between 2 and 3 on the dial. Adjust the LEVEL control, R24, to obtain a .5 volt peak-to-peak output. The response curve should be ± 5 db at 10 mc with respect to 5 mc.

16. Turn the EQUAL control, R4, fully ccw. The response should be the same as that shown in figure 44, with the peak occurring at 7.5 mc. This illustration is a composite photograph showing the appearance of the envelope with the EQUAL control turned to each extreme and then adjusted for a flat response. If the peak does not occur at 7.5 mc, remove the Playback Amplifier and adjust coil L1. Turning coil L1 ccw will shift the peak towards the high end of the band; turning it cw will shift the peak to the low end.

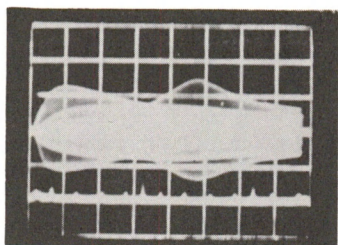


Figure 44—Composite Waveforms Showing Response Characteristics

NOTE

Equal control turned to each extreme then set between 2 and 3 on dial. 1 mc markers from 0 to 12 mc.

17. Repeat the foregoing procedure for the remaining Playback Amplifiers.

FM SWITCHER (Module 318B)

The FM Switcher (refer to figure 45) combines the four separate FM channel outputs from the four Playback Amplifiers (modules 215A through 218A) into one continuous FM signal, which is then fed to the FM Equalizer (module 132).

In the non-critical first switching stages, the four inputs are combined to form two outputs. Here the signals are fed in pairs, i.e., channels 1 and 3 and channels 2 and 4, from opposite sides of the head-wheel into two diode gates. The gates are opened at the appropriate time by keying pulses. These pulses are generated in the two tonewheel rate (240/250 cps) multivibrators, Q13, Q12 and Q16, Q15, the latter being driven with a delayed trigger.

The timing reference for the first or undelayed TW Rate multivibrator, Q13, Q12, is established by a pulse (A, figure 46) derived from the Tone Wheel Processor (module 313). This pulse occurs near the middle of head no. 1 due to the mechanical arrangement of the pulse-generating notch on the tone wheel in relation to the four heads.

Two pulse outputs are taken from the first TW Rate multivibrator, Q13, Q12. The first output (B, figure 46) is used to key diode gate no. 2 which combines the FM input of channels 2 and 4 into a signal channel (C, figure 46). The second pulse output is passed through a delay amplifier, Q14, which delays the pulse approximately 1000 microseconds (D, figure 46). The delayed pulse is used to drive the second or Delayed TW Rate multivibrator, Q16, Q15. The output of this multivibrator (E, figure 46) keys diode gate no. 1 where the FM inputs of channels 1 and 3 are combined into a single output (F, figure 46). The output of each gate is fed to a separate emitter follower, each of which is followed by a diode quad. From gate 1 the output is fed to Q17 which drives quad Z2. Similarly, the output of gate 2 goes to Q9 and the latter, in turn, drives Z1. The quads, Z1 and Z2, are driven push-pull in phase opposition by a 2 x TW Rate (480/500 cps) pulses, to combine the two FM inputs into a single FM output. The gating input to the quads is generated in Q2, Q1, the $\div 2$ multivibrator or binary divider. The output from Q2, Q1 (K, figure 46) is passed through a three-stage feedback amplifier, Q4, Q5, and Q6, and then applied to the quads. Correct phasing of the pulse is obtained by triggering one side of the $\div 2$ multivibrator, Q2, Q1, with the tone wheel pulse, insuring that head no. 1 is keyed in when the tone wheel pulse occurs.

Switching between the quads takes place at the time the first sync pulse interval occurs during the period when two heads overlap in reading information from the tape. To confine the switching to the overlap region, a delayed 4 x Tone Wheel (960/1000 cps) pulse is developed in the Tone Wheel Processor (module 313). The delay of this pulse is controlled by the 4 x TW delay potentiometer on the Tone Wheel Proc-

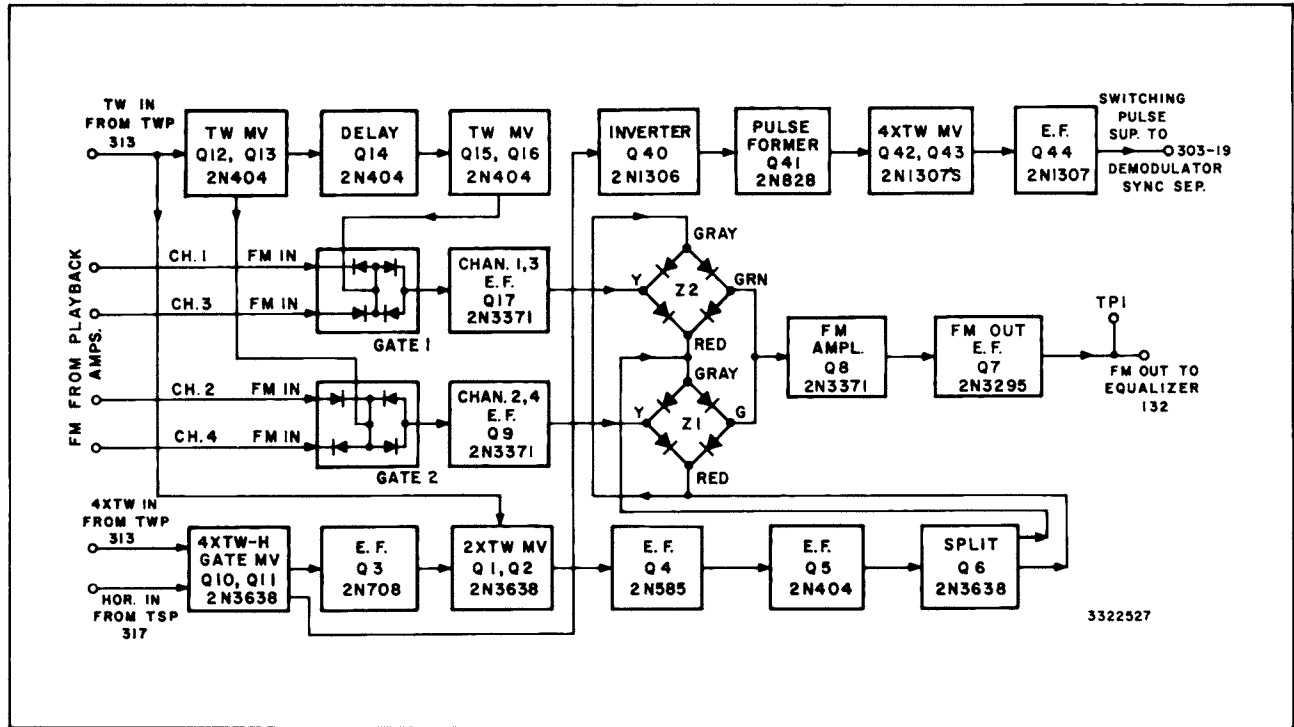


Figure 45—Block Diagram, FM Switcher Module

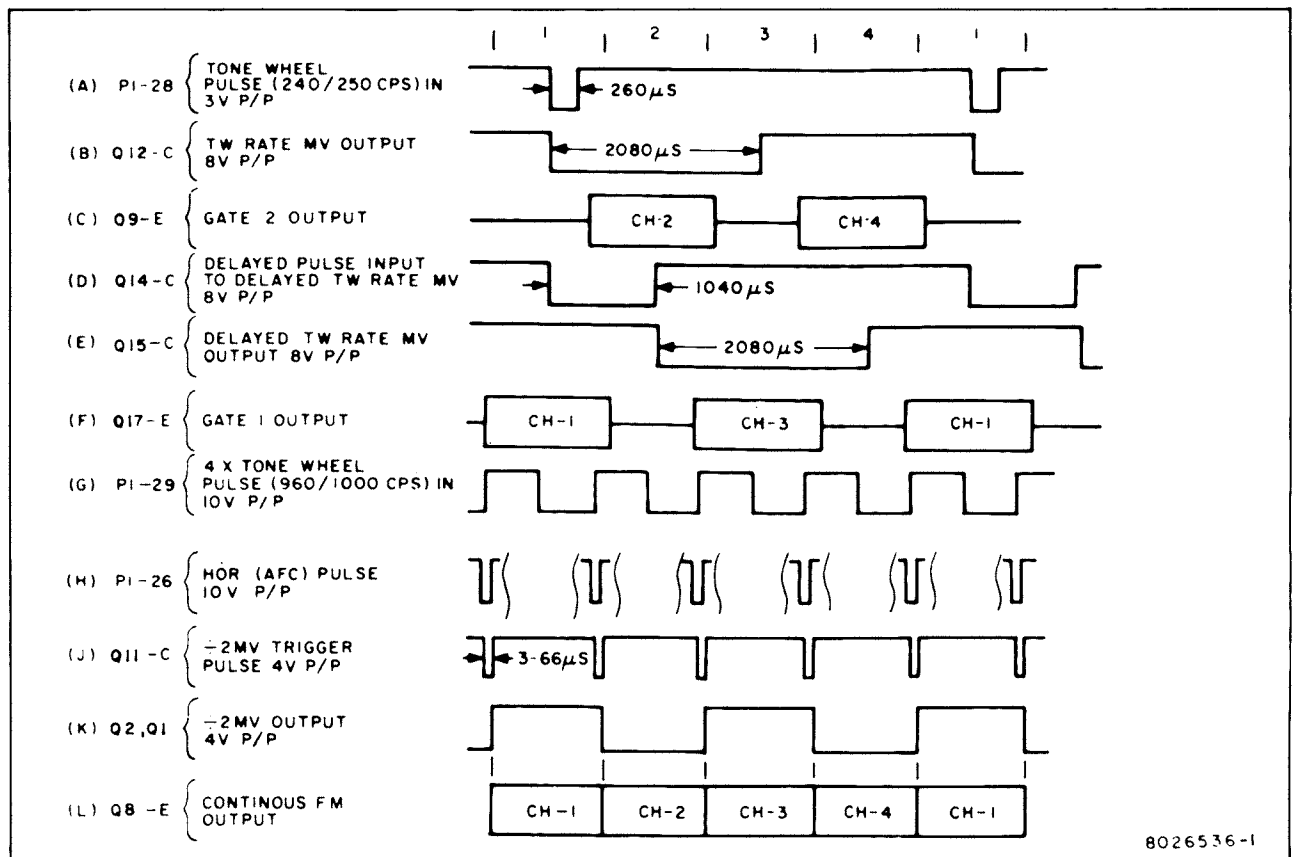


Figure 46—Idealized Waveforms; FM Switchers

essor and the potentiometer is adjusted so that the pulse edge occurs during the overlap period.

The 4 x TW pulse (G, figure 46) is fed to the bi-stable gate multivibrator, Q11, Q10, causing it to change state. The gate (Q11, Q10) is then flipped to the opposite state by the first AFC Horizontal Pulse (H, figure 46) arriving after the 4 x TW pulse. The AFC Horizontal Pulse is formed in the Tape Sync Processor (module 317). Once the gate has been flipped by this horizontal pulse, the continuing train of horizontal pulses will have no further effect on the gate until another 4 x TW pulse arrives and causes the gate to again change state.

The output pulse from the gate (J, figure 46) is coupled through an emitter follower, Q3, to the $\div 2$ multivibrator, Q2, Q1. It is the positive-going trailing edge of this pulse, which is determined by the first horizontal pulse following the 4 x TW pulse, that triggers the $\div 2$ multivibrator.

The output of the $\div 2$ multivibrator, after passing through a three-stage amplifier, Q4, Q5, Q6, drives the two quads to combine their separate FM input signals into a single FM output signal. The single continuous FM output signal from the quads (L, figure 46) is fed to amplifier Q8, which is dc stabilized

by a feedback loop. Q8 drives the base of emitter-follower Q7. Q7 feeds the signal to the FM Equalizer module 132.

CIRCUIT GENERATING DIODE GATE KEYING PULSES

Figure 47 shows the circuits that form the keying pulses that drive the two diode gates. The tone wheel rate multivibrator, Q12, Q13, is a monostable multivibrator, with Q13 off and Q12 on in the stable state. A pulse from the Tone Wheel Processor (module 313) is coupled through steering diode CR20 to Q13, turning it on. The on period of Q13 is determined by the length of time C29 takes to charge through R67, which is approximately 2000 microseconds. From the collector of Q12, the output pulse, slightly integrated by C18 and R42, is fed to diode gate no. 2, where channels 2 and 4 are combined. The output pulse from the collector of Q13, the other half of the multivibrator, is fed to Q14, the delay stage, cutting it off. (The delay stage is a standard boxcar circuit.) The delay interval, which is approximately 1000 microseconds or one head wide, is determined by C28 discharging through R63. The positive-going edge of the pulse appearing on the collector of Q14 is used to trigger the delayed tone-wheel rate multivibrator, Q16, Q15. This

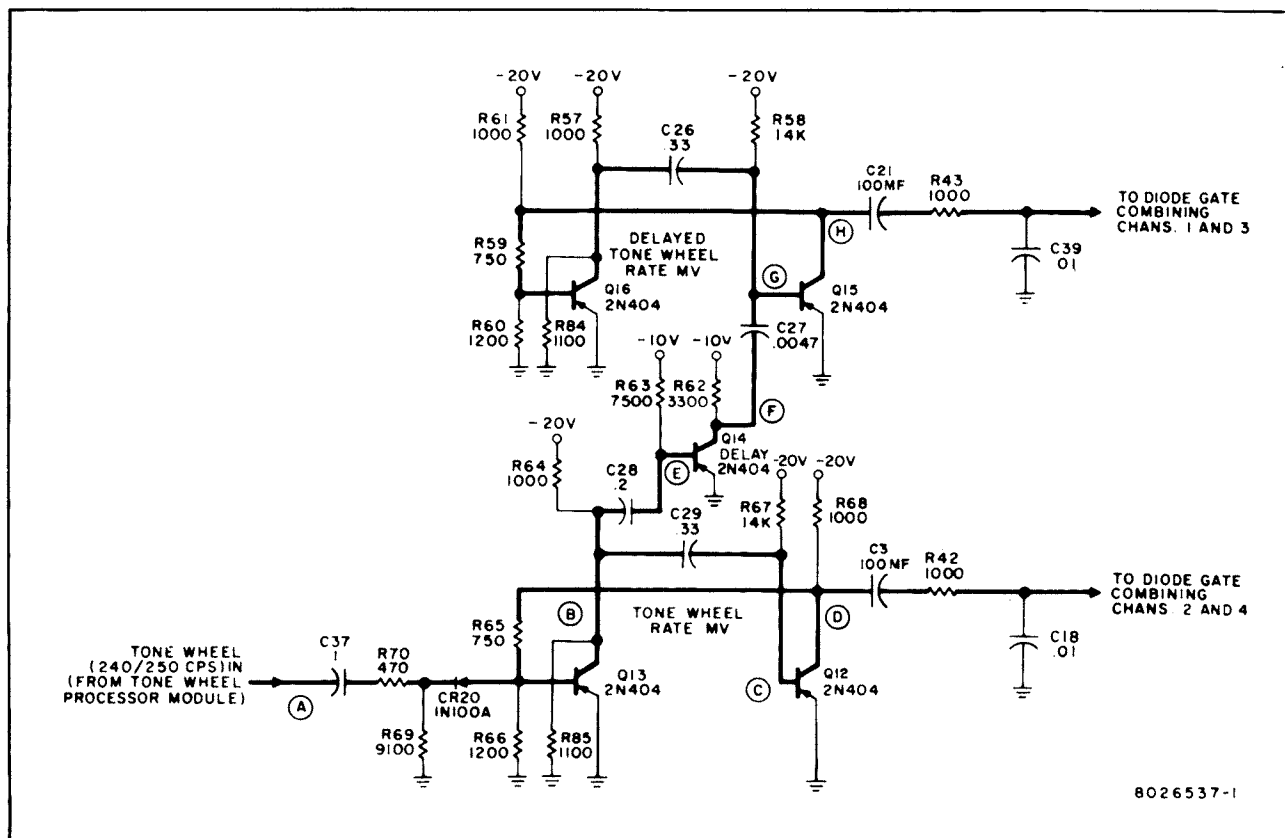
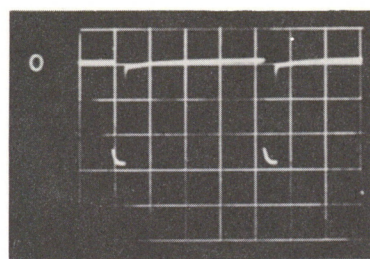
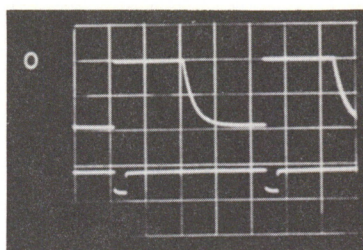


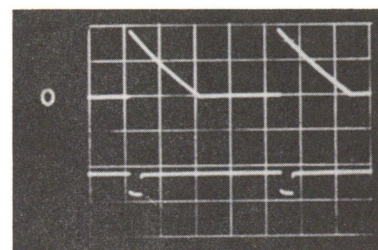
Figure 47—Tone Wheel Rate Multivibrators and Delay Circuits



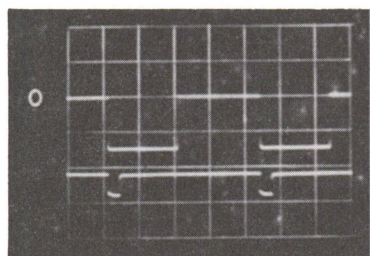
**A. P1-28, tone wheel pulse,
1 ms/cm, 1v/cm.**



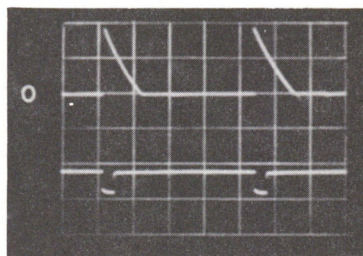
**B. Top: Q13 collector, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



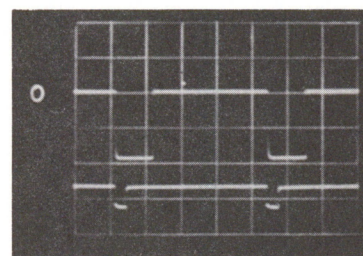
**C. Top: Q12 base, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



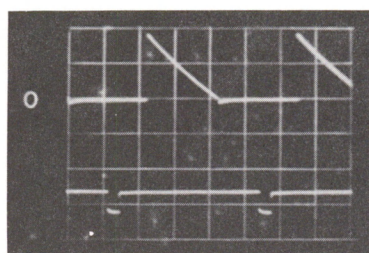
**D. Top: Q12 collector, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



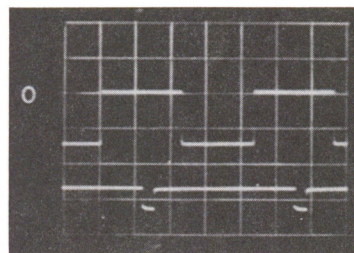
**E. Top: Q14 base, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



**F. Top: Q14 collector, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



**G. Top: Q15 base, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**



**H. Top: Q15 collector, 1 ms/cm,
5v/cm.
Bottom: Tone wheel reference.**

Figure 48—Typical Waveforms; Tone Wheel Rate Multivibrators and Delay Circuits

is a monostable multivibrator, identical to Q12, Q13. The input trigger is fed to the base of Q15, turning off this normally on transistor. The output pulse for keying diode gate no. 1, where channels 1 and 3 are combined, is taken off the collector of Q15 and coupled through an integrator consisting of C39 and R43 to the gate.

DIODE GATES

The two diode gates are shown in figure 49. The output pulses from the tone-wheel rate multivibrator, Q12, Q13, are applied to gate no. 2 at the junction of R5 and R6. During the negative half of the cycle, CR2, CR4 conduct, and CR1, CR3 are cut off, thus allowing FM input from channel 2 to pass. On

the positive half of the cycle, diodes CR1, CR3 conduct while CR2, CR4 are cut off, and the FM input from channel 4 is passed. As a result of each pair of diodes switching on and off, one combined signal appears at the output. The output of the gate is coupled through C4 to an emitter follower, Q9. The output from the emitter of Q9 is coupled through R88 and C5 to one side of quad Z1.

Diode gate no. 1, which combines the input of channels 1 and 3, is identical to gate no. 2, except that the keying pulses originate in the delayed tone wheel rate multivibrator, Q15, Q16. These pulses are delayed approximately 1000 microseconds or one head period so that they will occur during the time interval of heads 2 and 4. Similarly, the output of gate no. 1 is fed to an emitter follower, Q17, the output of which is coupled through R89 and C23 to quad Z2.

TIMING OF QUAD KEYING PULSES

The timing of the pulses used to key the quads is critical. Switching must take place during the first horizontal sync interval that occurs in the overlap region where two video heads are in contact with the tape. Switching at this time prevents any transients that might occur from being seen, and enables the redundant information read by two heads overlapping to be eliminated. Q10, Q11, the bistable gate (960/1000 cps) multivibrator (see figure 51) acts as a gate

to ascertain the time this coincidence takes place. One input to Q11 is the 4 x TW (960/1000 cps) pulse, which originates in the Tone Wheel Processor (module 313). This pulse is timed by adjusting the 4 x TW DELAY control on the Tone Wheel Processor to coincide with the overlap period. If this control is not properly adjusted, gaps or overlaps will occur in the switching. The effect of this will be to cause noise to appear on the picture monitor every sixteen lines.

The pulse is differentiated by C30 and R73 and the positive spike is coupled through CR21 to turn off Q11 and turn on Q10. The multivibrator remains in this state until Q10 is triggered off by the trailing edge of a horizontal sync pulse, which is generated in the afc horizontal multivibrator in the Tape Sync Processor (module 317). The afc circuit advances the pulse so that switching coincides with the horizontal sync interval of the video signal. It is necessary to advance the pulse to compensate for the delays encountered in the FM demodulation process used in recovering the video component and then separating sync from the video. The degree of pulse advance is variable and is set by adjusting the TAPE HOR FREQ SET control on the Tape Sync Processor, so that switching takes place immediately following the edge of sync.

The horizontal sync pulse input to Q10 is differentiated by C36 and R82 and coupled through CR22 to

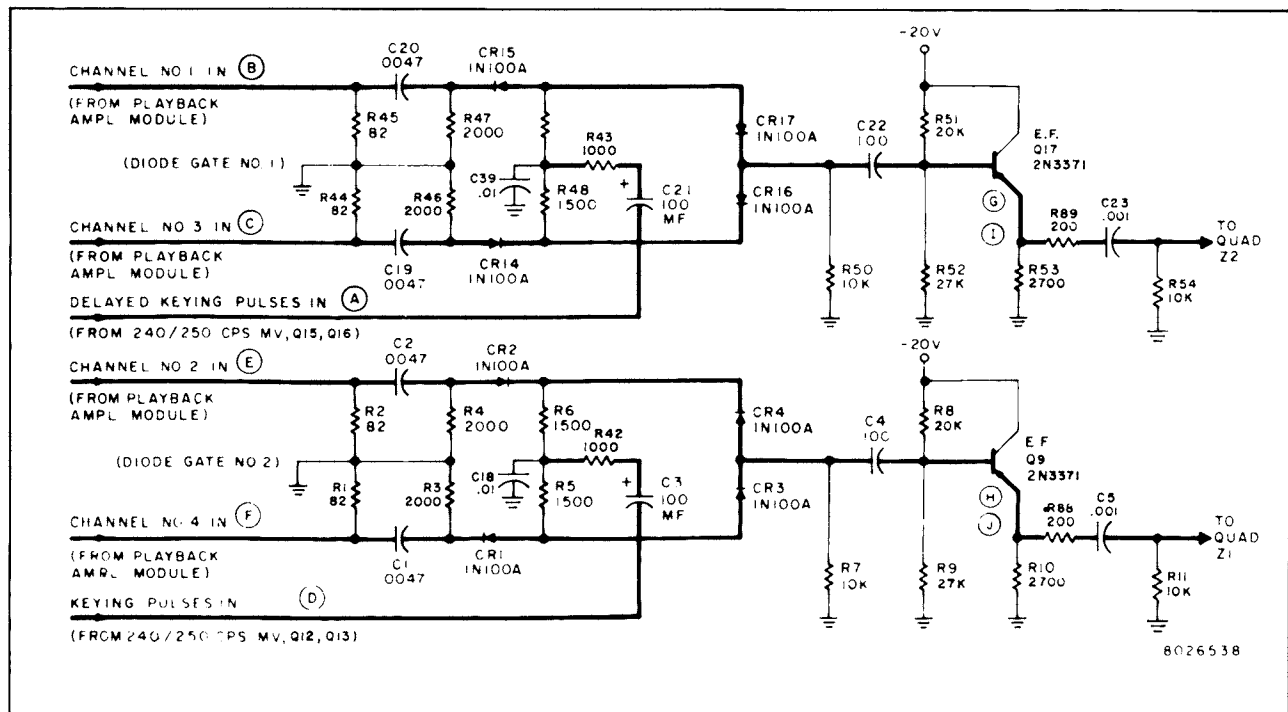
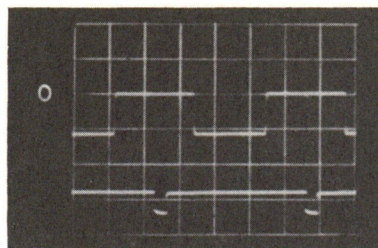
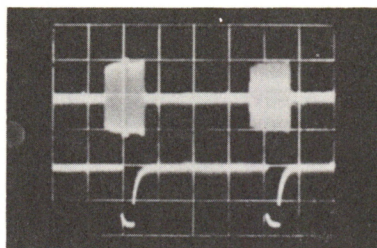


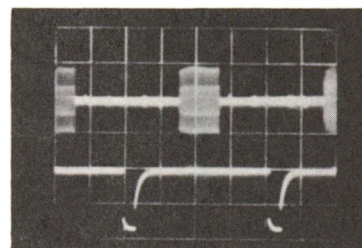
Figure 49—First Gating Stage, 4X2 Channel Switching and Output Circuits



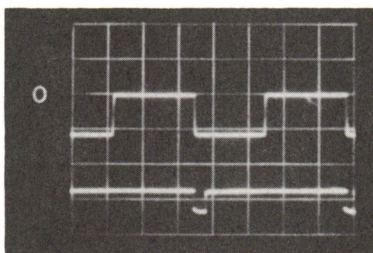
A. Top: Junc. R43, C39, delayed keying pulses, 1 ms/cm, 5v/cm. Bottom: P1-28, Tone wheel reference.



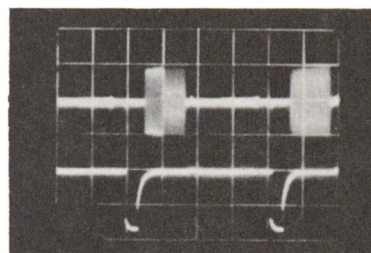
B. Top: P1-17, head #1 FM, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



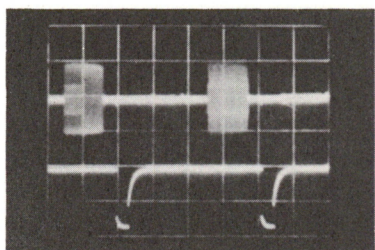
C. Top: P1-18, Head #3 FM, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



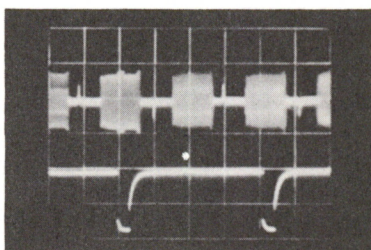
D. Top: Junc. R42, C18, keying pulses, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.



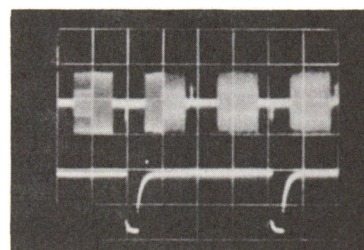
E. Top: P1-19, head #2 FM, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



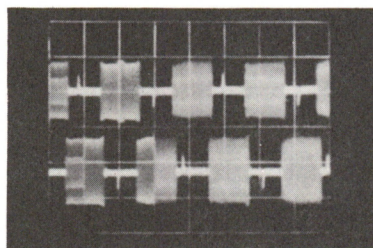
F. Top: P1-20, Head #4 FM, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



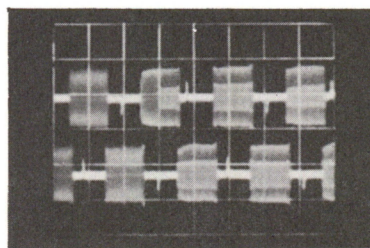
G. Top: Q17 emitter, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



H. Top: Q9 emitter, 1 ms/cm, .2v/cm. Bottom: Tone wheel reference.



I. Top: Q17 emitter, 1 ms/cm, .2v/cm. Bottom: Q9 emitter, 1 ms/cm, .2v/cm.



J. Top: Q9 emitter, 1 ms/cm, .2v/cm. Bottom: Q17 emitter, 1 ms/cm, .2v/cm.

Figure 50—Typical Waveforms; First Gating Stage, 4X2 Channel Switching and Output Circuits

the base of Q10. The initial positive spike turns off Q10 and turns on Q11. The subsequent pulses have no effect on Q10 and the multivibrator remains in this state until another $4 \times TW$ pulse arrives to trigger Q11 and then the cycle is repeated. The output pulse, at a $4 \times TW$ rate, is taken off the collector of Q11. This pulse is of variable width, depending on when a horizontal pulse arrives after the $4 \times TW$ pulse. The output pulse is differentiated by R72 and C31 and applied to emitter follower Q3.

The positive spike from the emitter of Q3 is fed through steering diodes to both sides of the binary divider, Q2, Q1 (see figure 51) which supplies the keying pulses to the quads. Each positive trigger causes the multivibrator to change state, resulting in a $\div 2$ action taking place. Diodes CR9 and CR13 serve as gates that conduct alternately so that the input trigger is applied first to one side cutting it off and then to the other side. To prevent phase ambiguity and to maintain the correct phase relationship so that the gate for channel 1 causes quad Z2 to conduct, the differentiated positive spike of the tone wheel pulse (240/250 cps) is fed to one side (Q1) of the multivibrator to insure it is turned off during head no. 1 interval. Phasing is established at the beginning of the cycle so the multivibrator remains correctly phased thereafter. The output of the $\div 2$ multivibrator is a $2 \times TW$ rate pulse (480/500 cps) which is taken off the collector of Q2 and applied through Z3 to the input of the amplifier stages (see figure 53). Z3, a pair of back-to-back diodes, clips the pulse before it enters the amplifier.

QUAD KEYING, 2×1 SWITCHING AND FM OUTPUT

The amplifier stage consists of Q4, Q5, and Q6 which forms a feedback amplifier to provide drive for the two quads, Z1 and Z2. Two pulse outputs are taken from Q6, one from the emitter, the other from the collector. Each pulse output is fed to both quads (see figure 55), driving them in phase opposition so that when one quad is conducting the other is non-conducting. R135 is adjusted for equal amplitudes at Q6 emitter and collector. This back-and-forth switching action between the quads results in the two separate FM inputs being combined into a single continuous output. The output is fed to Q8, a dc stabilized amplifier which drives emitter follower Q7. Q7 couples the signal to a low-pass filter network. This filter network composed of L1, L2, L3, C66, C67, C68, C69, C70, C71 is used to reduce low frequency switch-

ing transients below 200 kc. The output of the filter is fed to the FM Equalizer module 132.

When the TR-22 is in the Record or Setup modes of operation, the FM output of the quads is turned off. The circuit that controls the on-off functioning of the quads is composed of CR7, C40, R86, and R87 (see figure 55). In the Record or Setup modes, +70 volts is switched on in the Regulator (module 329) and this develops a positive bias across R87. This positive potential is sufficient to offset the reverse bias applied to CR7 by the negative potential developed across R86 from the -20 volts. With the reverse bias overcome, CR7 conducts and any output from the quads will pass to ac ground through the path provided by C40.

When the TR-22 is in the Play mode, the +70 volts is switched off and CR7 will be cut off due to the reverse bias applied to it from the -20 volts across R86. Thus, in this mode, the signal appearing at the output of the quads will follow the path going to Q8, the FM amplifier.

A switching pulse suppressor circuit shown in figure 57 is used to produce a $3.2 \mu\text{sec}$ clamp pulse which operates at the $4 \times TW$ rate to suppress the switching pulses that occur every sixteen lines. This signal is timed to occur on the tip of sync and is fed to the sync separator in the demodulator module.

The $4 \times TW$ rate square wave signal derived from multivibrator Q10, Q11 is connected to an inverter amplifier Q40. This in turn drives a pulse narrowing circuit composed of C61, R124 differentiator which is coupled to the base of Q41. Q41 (boxcar) narrows the pulse to $0.5 \mu\text{sec}$ at its collector, and is timed with the leading edge of tape sync. The positive going pulse at the base of Q42 triggers the monostable ($4 \times TW$) rate multivibrator which produces a 3.2 micro-second pulse which is fed to Q44. Q44 is an emitter follower used to isolate the multivibrator from the load. Q44 provides a positive going clamp pulse with its leading edge timed to coincide with leading edge of sync which appears at Q23 base in the sync separator of module 303A. This has the effect of "pushing out" the switching pulses that occur at the 16-line rate in the demodulator output.

The need for this switching pulse suppression arises in the use of monochrome automatic timing correction (MATC) to prevent switching pulses causing improper timing information. (See waveform and timing diagram figures 58 and 59.)

The filter circuit in figure 55 composed of L1, L2,

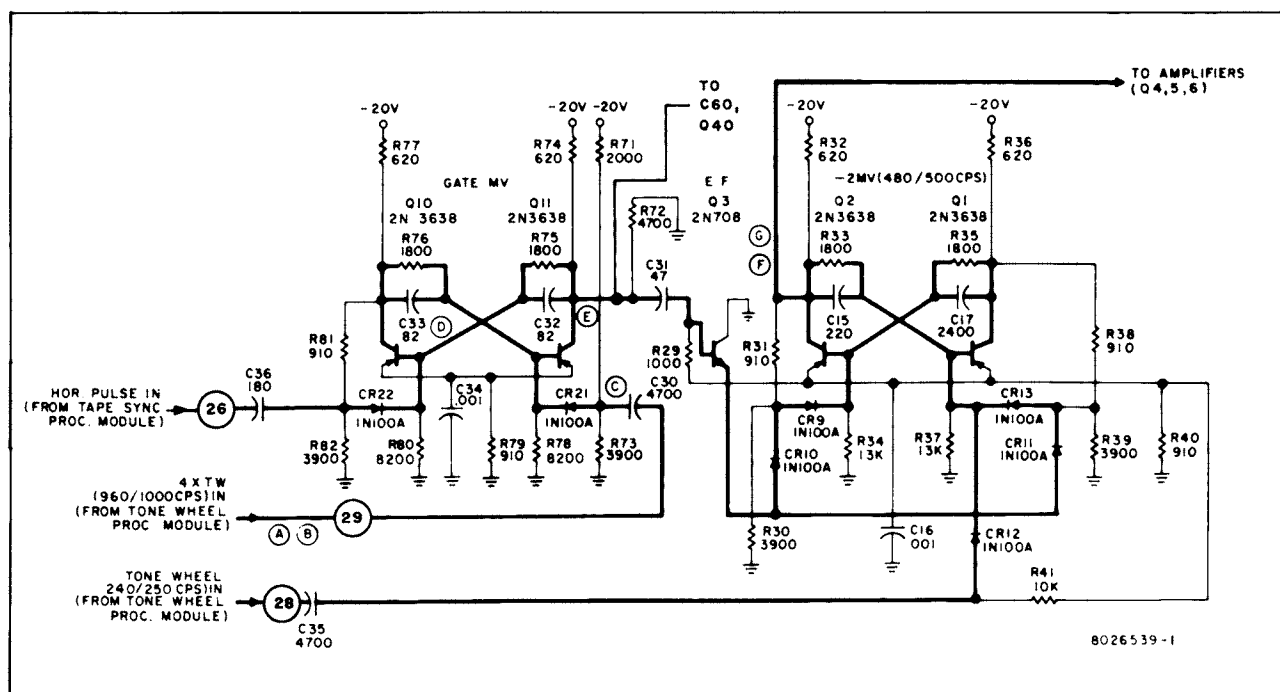


Figure 51—Gate Multivibrator and $\div 2$ Multivibrator

L3, C66 thru C71, is a high pass filter to clean up switching transients in the output of the switcher.

FM EQUALIZER (Module 132)

The FM Equalizer supplements the action of the equalizers in each Playback Amplifier (modules 215A, 216A, 217A, 218A), by compensating for the loss of low frequency components of the FM signal in the head to tape transfer during the Record and the Playback modes of operation.

As shown in the simplified schematic diagram, figure 60, the FM Equalizer consists of an emitter follower input, Q7, a shunt peak equalizer, Q1, a single driver, Q2, which is followed by two line driver series amplifier stages, Q3, Q4, and Q5, Q6.

The input is applied to the base of Q7. The output from the emitter of Q7 is fed to the emitter of Q1. The high frequency compensation coil, L1, in the collector circuit of Q1 is adjusted to produce a peak at 8 mc. The frequency response characteristic can be varied by rotating the FM equalizing control (FM EQ), potentiometer R2, back and forth, as shown in figure 61. When the FM EQ control, R2, is in the ccw position, the response at the high end of the FM band is increased, which represents a boost in the low end of the video band. When the FM EQ control is turned fully cw, the circuit produces a relatively flat response over the range of the FM band.

The signal from the collector of Q1 is coupled through C2 to the base of Q2. From the emitter of Q2, the signal is dc coupled through R9 to the base of Q3. The output from the collector of Q3 is coupled through C4 to the base of Q4. Two outputs are taken from the emitter-collector junction of the first line-driver stage, Q3, Q4. One is used to feed the Tape FM Signal to the Limiter section of (module 203B), while the other output is dc coupled through R14 to the base of Q5, which in conjunction with Q6 forms the final driver. The output of the emitter-collector junction of this stage feeds the monitor.

The SYNC GAIN potentiometer, R27, is used to vary the sync level in the video output. Adjusting R27 changes the bias on the sync gain control transistor, Q10, which is located on the Video Output (module 233A). The location in 132 is only for operator convenience, there is no electrical tie-in with 132 otherwise.

ADJUSTMENTS

As a matter of convenience, two methods of checking the frequency response of the FM Equalizer are given below. The first method permits the FM Equalizer module to remain in the TR-22 by taking the response measurements at the appropriate terminals on the FM Equalizer connector block at the rear of the TR-22. With the second method, the response

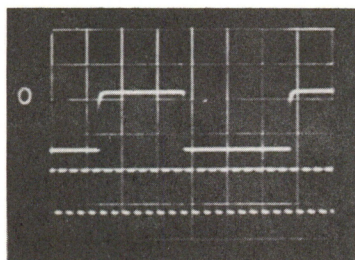
measurements can be made from the front of the TR-22 by mounting the FM Equalizer module in an extender. It is possible, however, that the wiring in the extender may cause additional capacitance to be introduced into the module circuitry which may slightly affect the adjustment covered in the second method.

Recommended Test Equipment

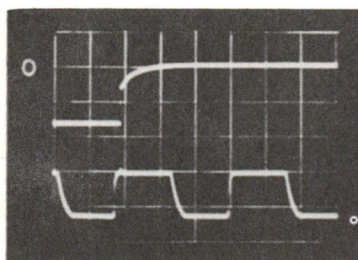
Tektronix Type 535A oscilloscope (or equivalent) with low capacity probe.

Video sweep generator capable of sweeping 0 to 15 mc.

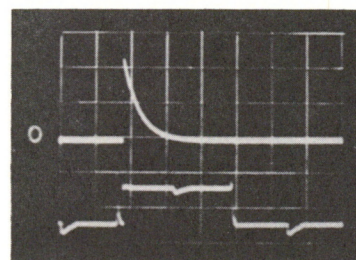
Calibrated rf attenuator network if sweep generator



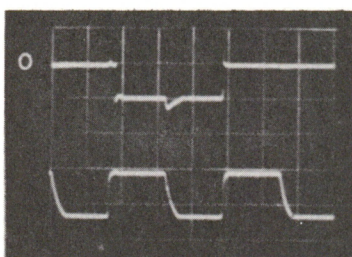
A. Top: P1-29, 4 x TW, .2 ms/cm, 5v/cm. Bottom: P1-26 horizontal pulse, .2 ms/cm, 10v/cm.



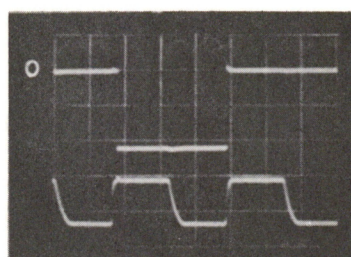
B. Top: P1-29, 4 x TW, 20 μs/cm, 5v/cm. Bottom: P1-26, hor. pulse, 20 μs/cm, 10v/cm.



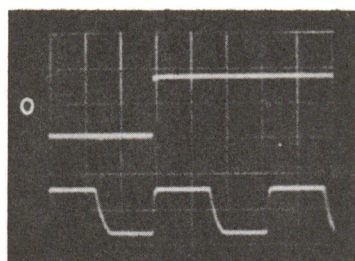
C. Top: Junction C30, R71, R73, 20 μs/cm, 2v/cm. Bottom: Junction C36, R81, R82, 20 μs/cm, 2v/cm.



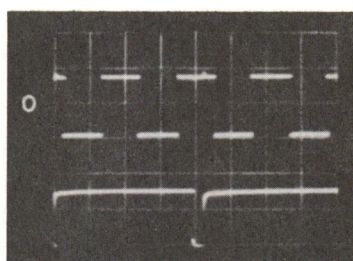
D. Top: Q10 base, 20 μs/cm, 1v/cm. Bottom: Hor. pulse reference.



E. Top: Q11 collector, 20 μs/cm, 2v/cm. Bottom: Hor. pulse reference.



F. Top: Q2 collector, 20 μs/cm, 2v/cm. Bottom: Hor. pulse reference.



G. Top: Q2 collector, 1 ms/cm, 2v/cm. Bottom: P1-28, tone wheel pulse reference.

Figure 52—Typical Waveforms; Gate Multivibrator and ÷2 Multivibrator Circuits

is not equipped with attenuator.

One 75-ohm terminating resistor.

First Method

1. Remove the power from the TR-22 by placing the EQUIPMENT POWER circuit breaker in the OFF position.

2. Remove pins 17 and 32 from their respective rectangular terminals in connector 132 on the rear of the TR-22. Use two pairs of long-nose pliers for this

purpose, one to hold the terminal in place in the connector block and the other to remove the pin from the terminal. Pull the pin out carefully while simultaneously applying sufficient pressure to the terminal to support it against the force of the withdrawing pin.

3. Connect the output of the sweep generator to the attenuator. Connect the output of the attenuator, using RG-59U coaxial cable, to terminal 17. Connect the ground braid on the input end of the coaxial cable to pin 1 on the connector.

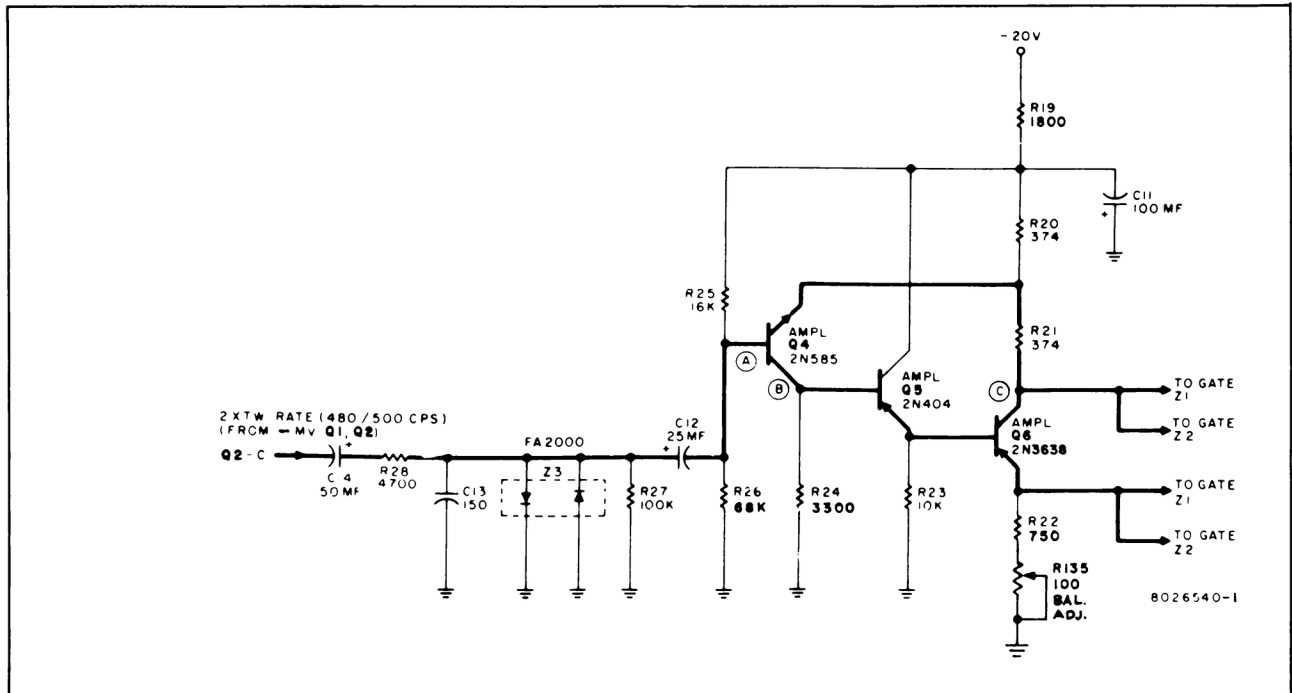
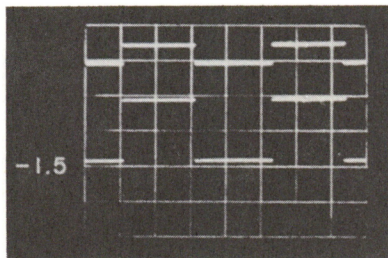
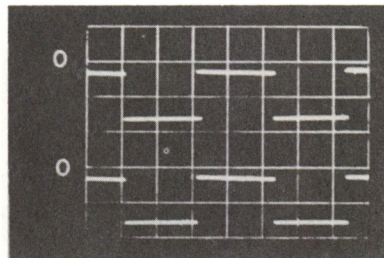


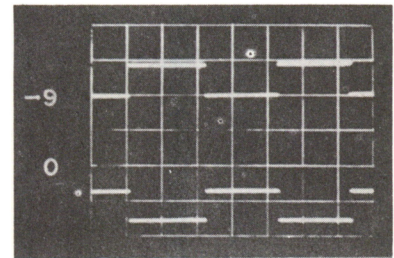
Figure 53—Amplifier Circuits



A. Top: Q4 base, .5 ms/cm.
Bottom: Q2 collector reference.



B. Top: Q4 collector, .5 ms/cm,
2v/cm. Bottom: Q5 emitter,
.5 ms/cm, 2v/cm



C. Top: Q6 collector, .5 ms/cm,
2v/cm. Bottom: Q6 emitter,
.5 ms/cm, 2v/cm

Figure 54—Typical Waveforms; Amplifier Circuits

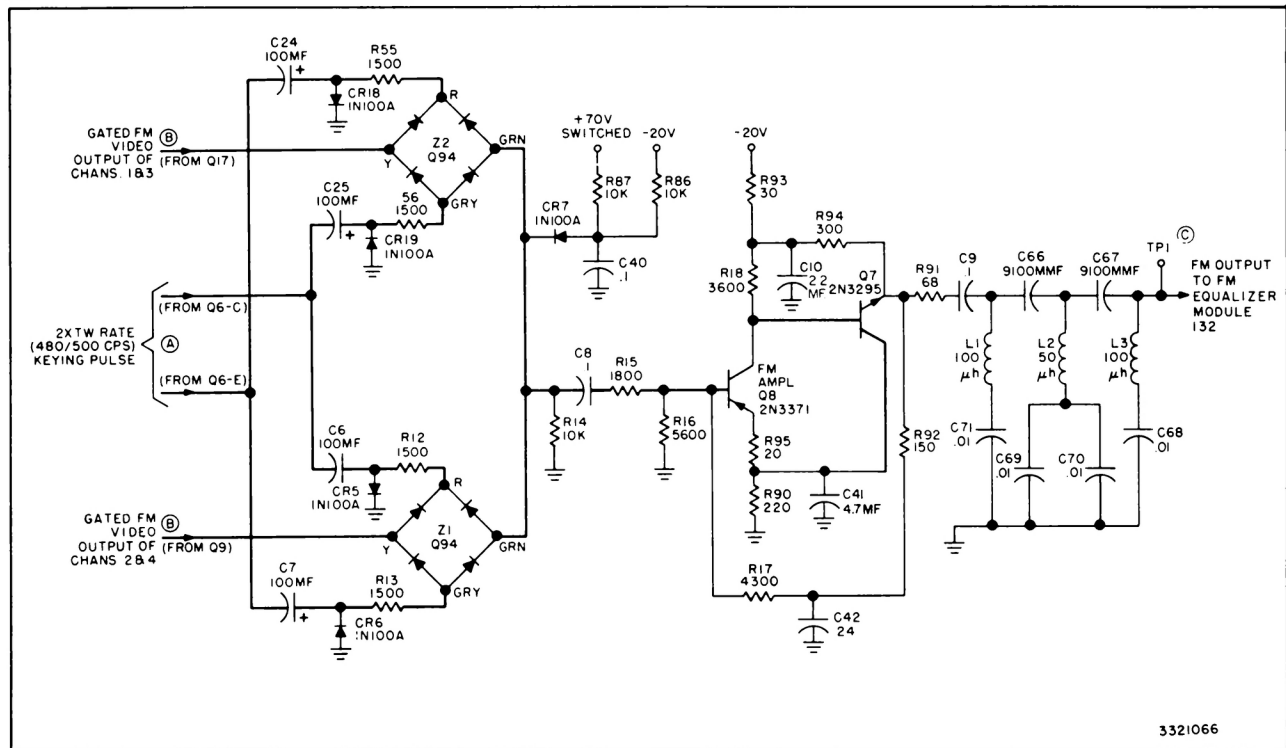


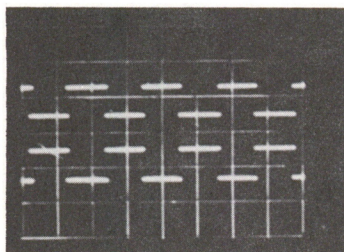
Figure 55—Second Gating Stage, 2X1 Switching and FM Output Circuits

4. Set the sweep rate of the generator for 0 to 10 mc, and adjust the output to obtain a .2 volt peak-to-peak signal at terminal 17, as measured on the oscilloscope.

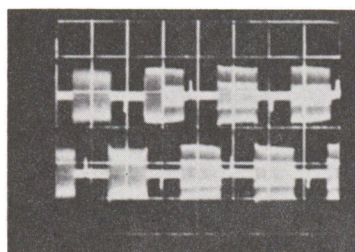
5. Terminate the output of the FM Equalizer by connecting the 75-ohm resistor across terminals 32 and 16. Connect a low capacity probe from the oscilloscope input to terminal 32; fasten the ground lead to terminal 16 keeping it as short as possible.

6. Place the EQUIPMENT POWER circuit breaker in the ON position.

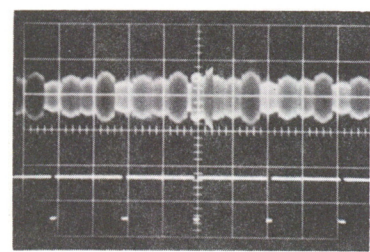
7. Turn the FM EQ control, R2, fully ccw. The response should be the same as that shown in figure 61, with the peak occurring at 8 mc. (This illustration is a composite showing the response waveforms when R2 is turned to either extreme.) If the peak appears below or above 8 mc, coil L1 will have to be adjusted until the response peaks at 8 mc. The latter adjustment will have to be on a trial and error basis, since coil L1 is an internal control. The module will have to be removed, coil L1 adjusted, the module then replaced and the waveform observed on the oscilloscope to determine the effectiveness of the ad-



A. Top: Q6 collector, 1 ms/cm, 2v/cm. Bottom: Q6 emitter, 1 ms/cm, 2v/cm.



B. Top: Q9 emitter, 1 ms/cm, .2v/cm. Bottom: Q17 emitter, 1 ms/cm, .2v/cm.



C. Top: TP1 2 ms/cm, .2v/cm. Bottom: TP2 on Module 132, 2 ms/cm, 5v/cm.

Figure 56—Typical Waveforms; Second Gating Stage, 2X1 Switching and FM Output Circuits

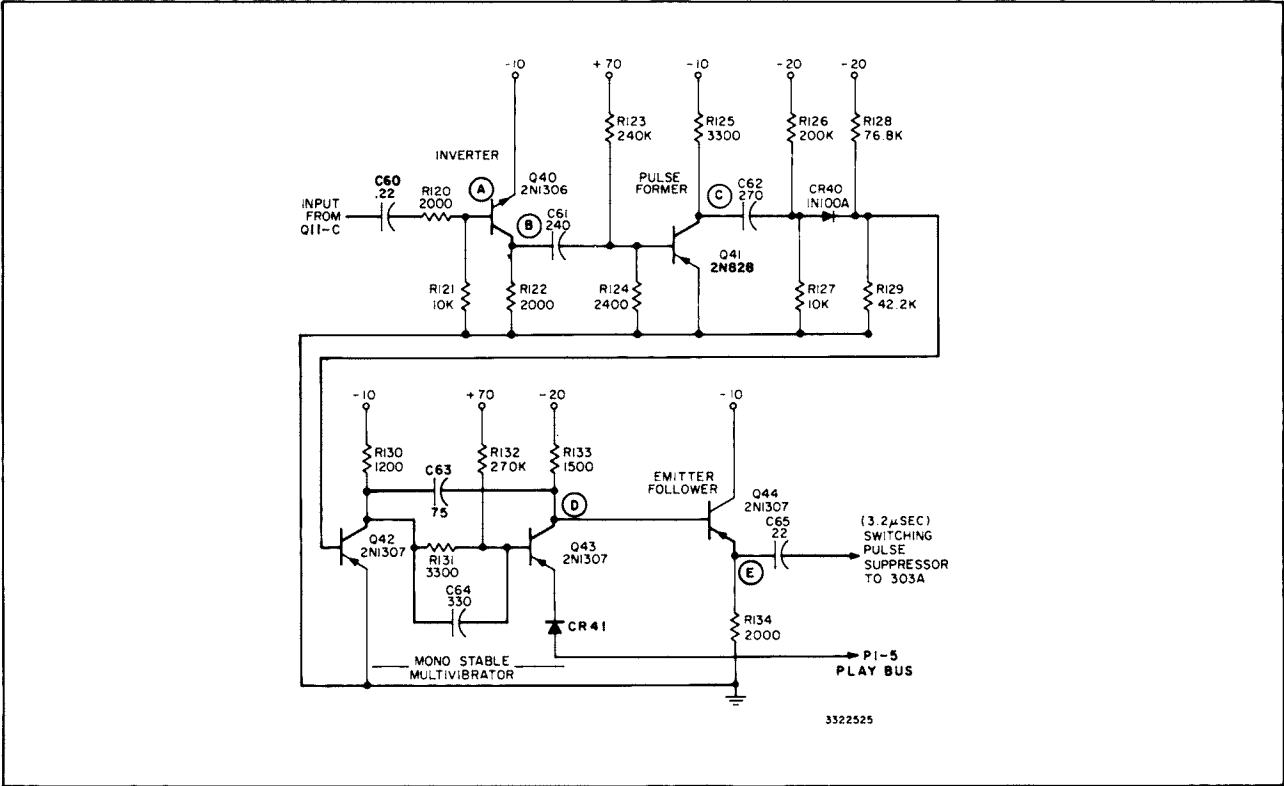


Figure 57—Sync Tip Switching Pulse Suppressor Circuits

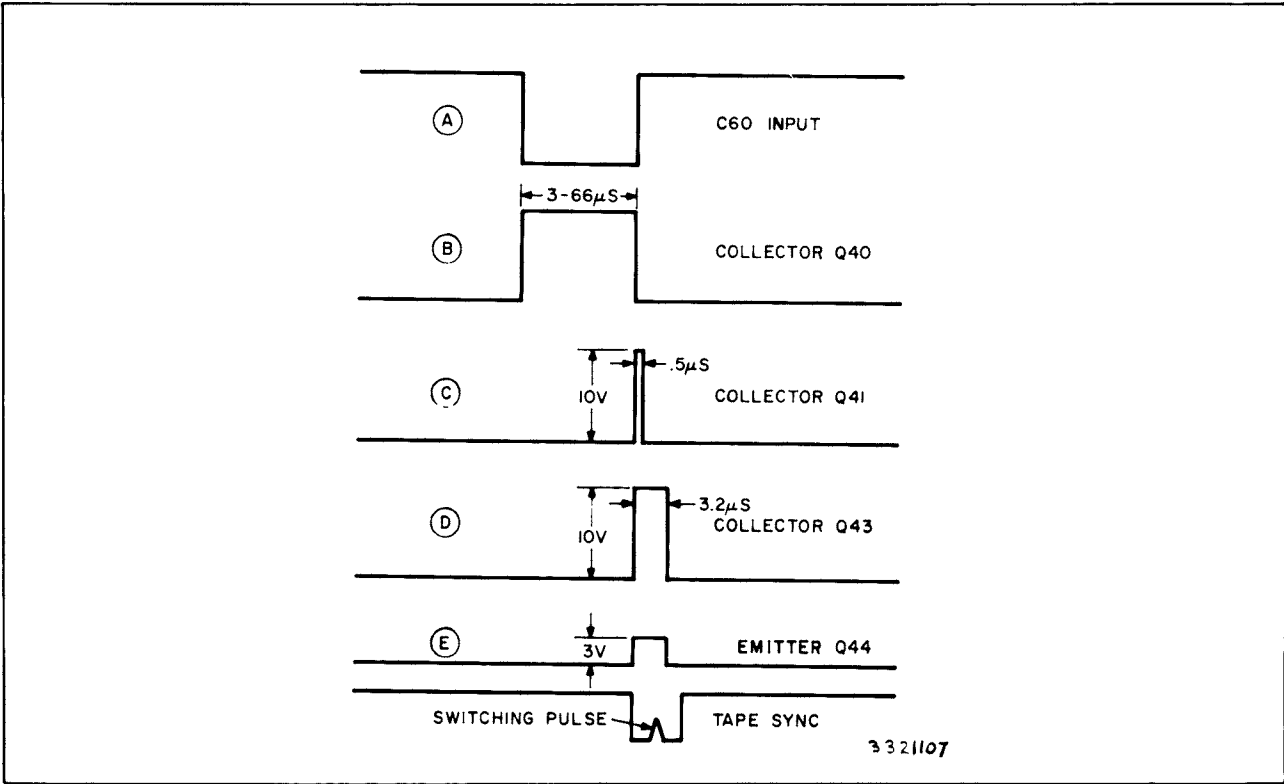


Figure 58—Timing Diagrams; Sync Tip Switching Pulse Suppressor

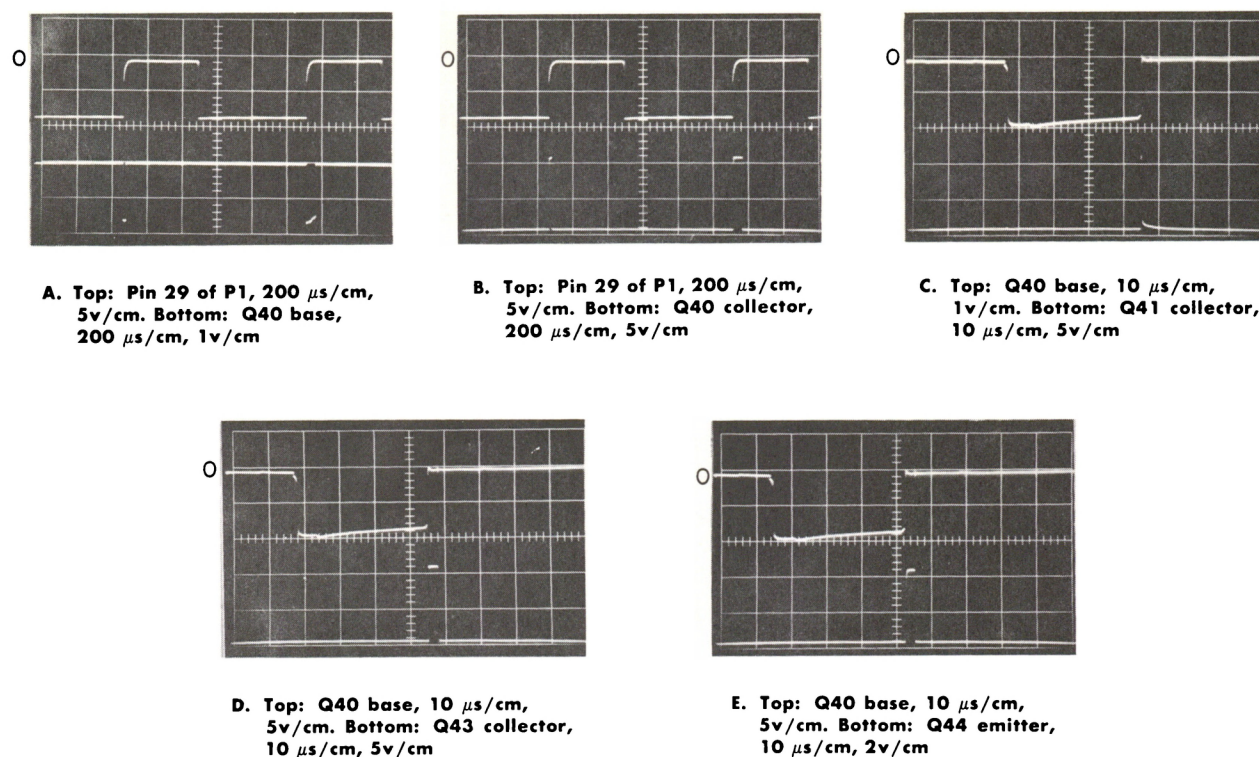


Figure 59—Typical Waveforms; Sync Tip Switching Pulse Suppressor

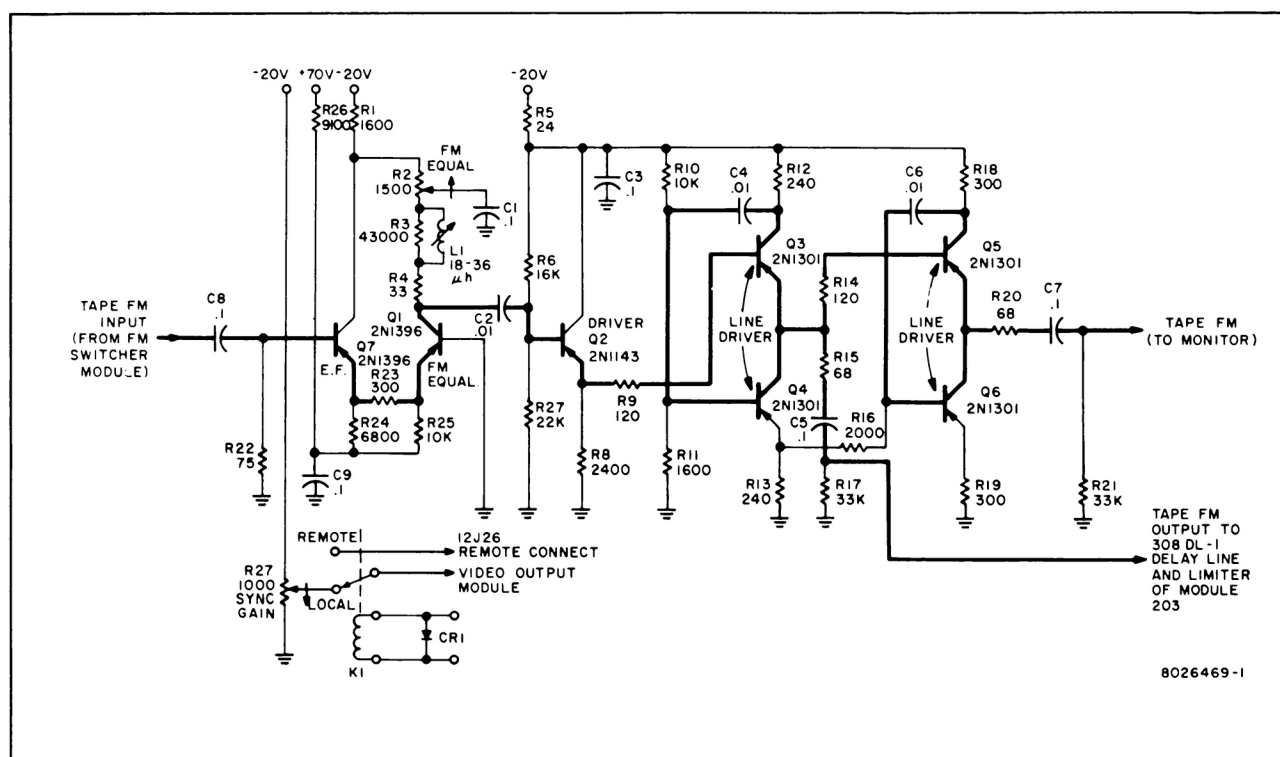


Figure 60—FM Equalizer Circuit

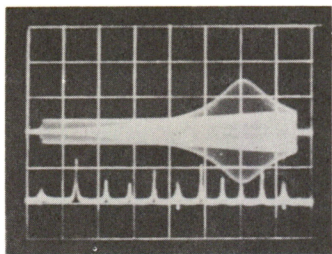


Figure 61 — Composite Waveform Showing Response Characteristics

justment. Turning L1 ccw will shift the peak towards the high end of the band; turning L1 cw will shift the peak towards the low end of the band. Repeat adjustment if necessary.

8. Turn the FM EQ control, R2, fully cw. A response similar to that shown in figure 61 should be obtained.

9. Replace pin 32 in its terminal and remove pin 31. Use the same technique described in step 2 for removing the pin. Terminate the FM Equalizer output by connecting the 75-ohm resistor across terminals 31 and 15. Connect a low capacity probe from the oscilloscope input to terminal 31; fasten the ground lead to terminal 15, keeping it as short as possible.

10. Check the response and output level at this point, with R2 first fully cw and then fully ccw. The level of the output signal at terminal 31 may be on the order of 10% lower than the output at terminal 32.

11. Replace pins 17 and 31.

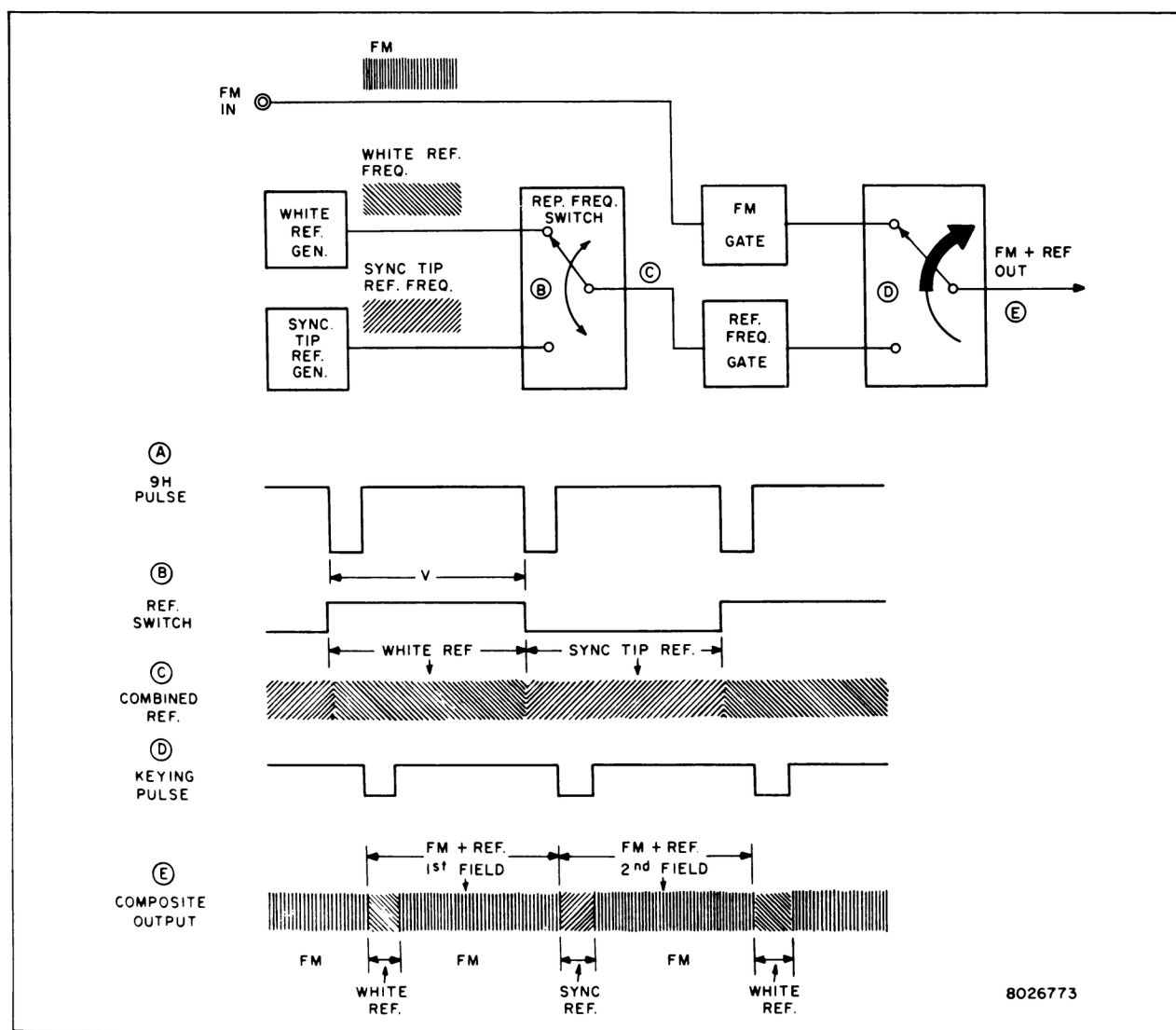


Figure 62—Simplified Functional Diagrams, FM Reference Switching

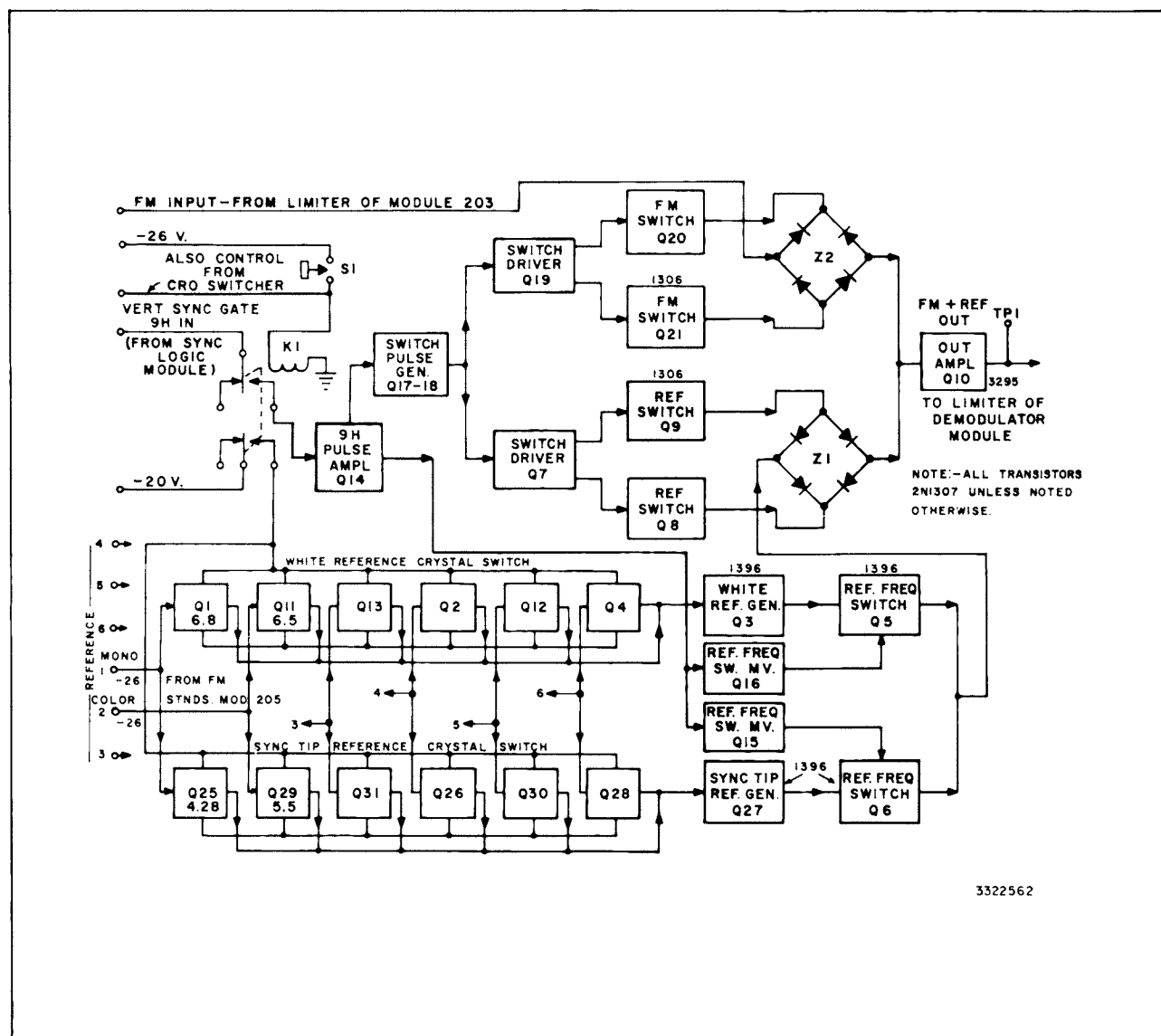


Figure 63—Block Diagram, FM Reference Module

Second Method

1. Place the module in an extender, and disconnect the coaxial cable on the input side of C8 within the module. Connect the output of the sweep generator to the attenuator; then connect the output of the attenuator using RG/59U coaxial cable to the input side of C8 and ground.

2. Set the sweep rate of the generator for 0 to 10 mc, and adjust the output to obtain a .2 volt peak-to-peak signal at C8, as measured on the oscilloscope.

3. Terminate the FM Equalizer output by connecting the 75-ohm resistor from the junction of C5 and R17 to ground; then connect a low capacity probe from the oscilloscope to the junction of C5 and R17.

4. Disconnect the Demodulator (module 203B) from the recorder by sliding it partly out of its slot. This is necessary in order to prevent double termination.

5. Turn the FM EQ control, R2, fully cw then fully ccw. The response should be the same as that shown in figure 61, with the peak occurring at 8 mc. (This illustration is a composite showing the response waveforms when R2 is turned to either extreme.) If the peak appears below or above 8 mc, adjust coil L1 until the response is peaked at 8 mc.

6. Disconnect the terminating resistor from the junction of C5 and R17, and replace the Demodulator module in the recorder.

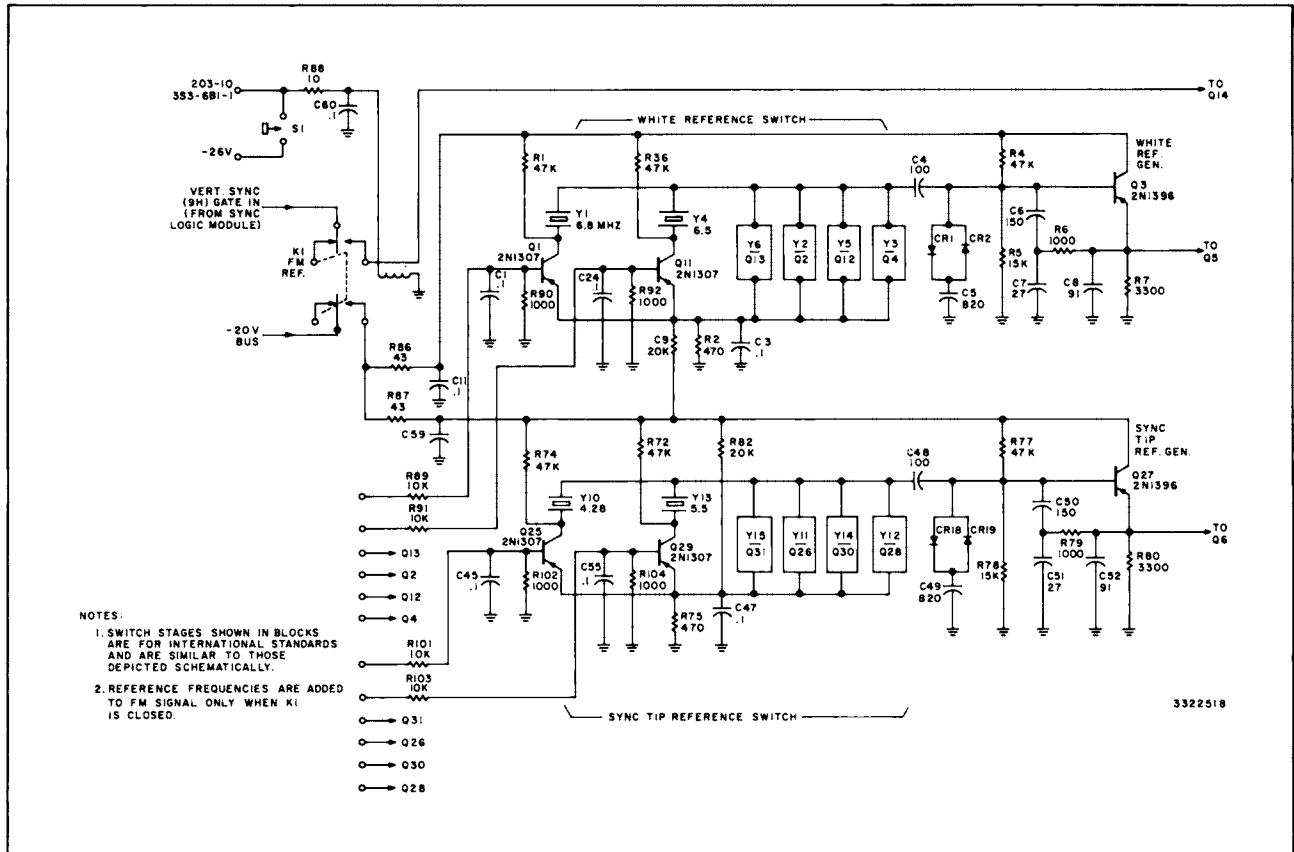


Figure 64—White and Sync Tip Reference Crystal Switches and Generator Circuits

7. Disconnect the coaxial cable from the junction of C7 and R21, and terminate this junction in 75 ohms.

8. Connect the probe to the junction of C7 and R21. The response at this point with R2 fully ccw then fully cw should be the same as that obtained in step 5; however, the output level may be on the order of 10% lower than the output at the junction of C5 and R17.

9. Restore the coaxial lead connections at C8 and at the junction of C7 and R21.

FM REFERENCE (Module 302A)

The FM Reference module provides two crystal controlled reference frequencies that represent the sync tip and the peak white deviation limits of the FM signal. The reference frequencies are short bursts that can be inserted alternately at a field rate following the vertical sync interval. When demodulated along with the FM representing video, the reference bursts result in calibration pulses at levels corresponding to standard sync tip and peak white carrier frequencies. There are six pairs of reference frequencies. The appropriate set is selected by means of the STDS switch on the front panel of the FM Standards (mod-

ule 205A). The reference bursts are added to the FM signal when the FM REF switch on the front panel is pressed or the FM REF switch on the CRO switcher (3S3). Otherwise, the circuits of the FM Reference module remains in a quiescent state.

The FM Reference module is shown in its simplest form in figure 62. Basically, the principle of operation can be likened to the action of two single-pole double-throw switches that have been arranged so that separate input signals can be successively combined to form one continuous output. The white and the sync tip reference frequencies are indicated by the opposing crosshatched signals adjacent to their respective generators. The FM input signal is shown as a series of vertical lines. Generators that produce keying or gating pulses, along with the pulse control circuits, have been omitted. However, keying waveforms (B and D, figure 62) are shown in their relation to the vertical sync gate (9H) pulse (A, figure 62) to demonstrate the switching sequence of the different signals. These waveforms, and the others in figure 62, are related to the simplified diagram by corresponding letters.

The reference frequency switch, operating at a ver-

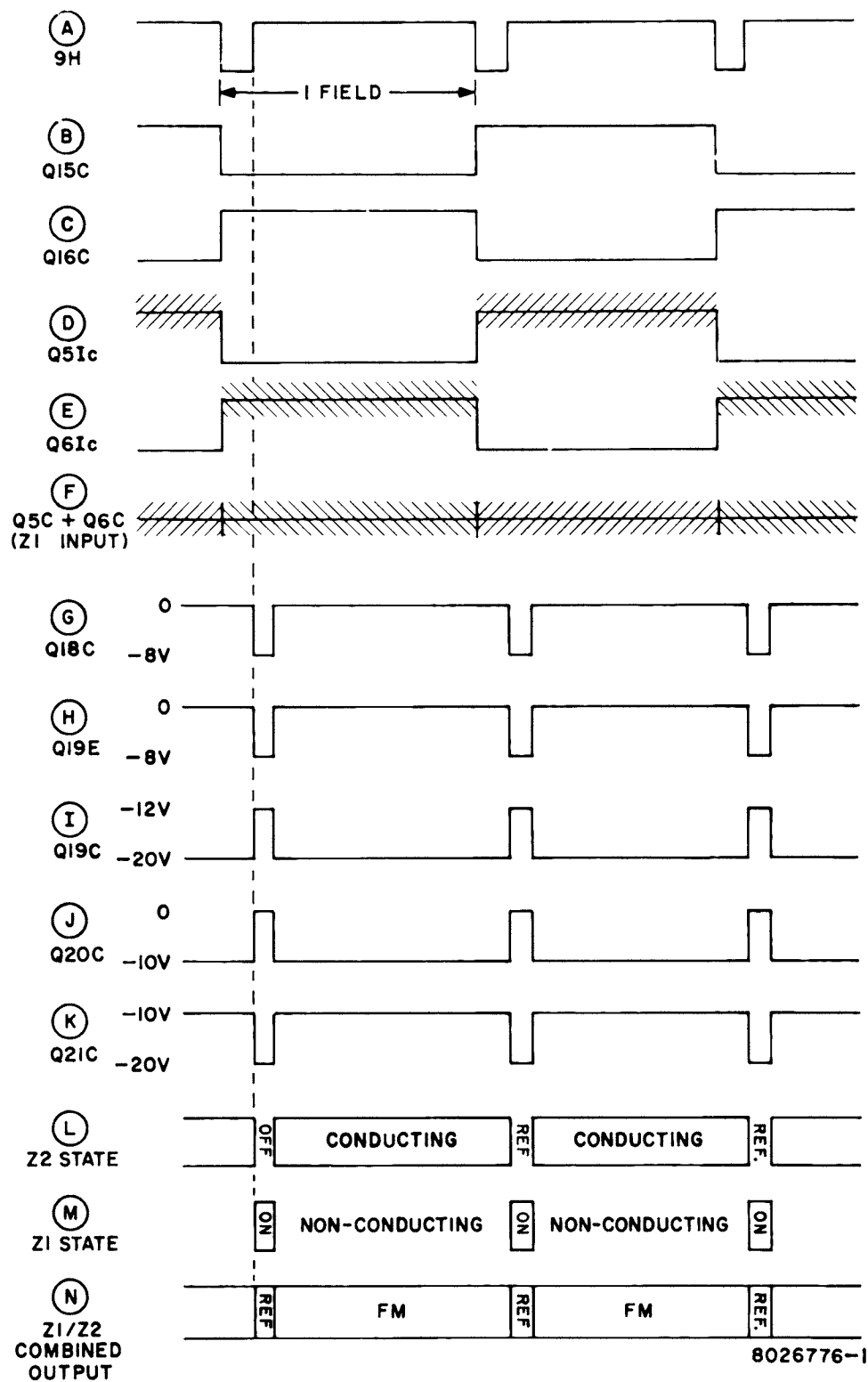


Figure 65—Waveform Timing Chart

tical rate from waveform B, switches back and forth uniformly between the sync tip reference and the white reference generators during the negative-going leading edge of the 9H pulse (A, figure 62). Thus equal increments of each reference frequency are passed and at the output of the switch there appears a continuous signal (C, figure 62) which is fed to the reference frequency gate.

The second switch, FM/reference, switches between the FM and the combined reference frequencies. Switching between these two signals occurs at a vertical rate during the positive-going trailing edge of the 9H pulse, in accordance with waveform D, figure 62. The reference frequency interval is much shorter than the duration of one field, therefore the FM gate is on much longer than the reference frequency gate. Thus the combined output signal appears as E, figure 62.

The reference frequencies are produced by two identical crystal oscillators, the white reference generator, Q3, and the sync tip reference generator, Q27. (See block diagram, figure 63.) Each crystal is controlled by a transistor switch and only the white and sync tip reference crystals corresponding to the standard selected for operation are activated. The remaining crystals are inactive. For example, assuming the selector switch on the FM Standards, (module 205A) to be in the MONO STD position, Q1 and Q25 are saturated and their associated crystals, Y1 and Y10, 6.8 mc and 4.28 mc, respectively, are thereby grounded.

The output of the white and the sync tip reference generators is fed to the reference switches, Q5 and Q6, which are alternately keyed on and off by the reference frequency switch multivibrator, Q15, Q16. The multivibrator keying signal and the combined output of the reference switches are depicted by waveforms B and C, respectively, in figure 62. The multivibrator is triggered by the leading edge of the 9H pulse which is generated in the Sync Logic (module 230B). The trailing edge of the 9H pulse triggers Q17, Q18, a monostable multivibrator that generates a 200-microsecond switch pulse (D, figure 62). This pulse determines the width of the reference burst that is inserted in the FM envelope.

The output of the switch pulse multivibrator is fed to two phase splitters, Q19 and Q7. Each of the latter drives a pair of switches, with the output of Q19 going to FM switches Q21 and Q20, while the output of Q7 goes to reference switches Q9 and Q8.

The FM switches supply the keying pulses to Z2,

the diode gate to which the FM input signal is applied. Similarly, the reference switches supplying keying pulses to Z1, the diode gate to which the white and sync tip reference frequencies are fed.

The FM REF switch (S1) and relay K1 must be closed to insert the reference frequency bursts in the FM signal, (also the FM REF switch on the CRO switcher may be used). When the FM REF switch is open, dc bias applied to the FM diode gate, Z2, keeps it on continuously so that the FM input signal passes through it to the output amplifier, Q10. When the FM REF switch is closed, the polarity of the fixed bias and the polarity of the keying signals applied to both diode gates, Z1 and Z2 are such that when one is on the other is off. Switching occurs between Z1 and Z2 after the vertical sync interval so that the reference bursts are alternately inserted during a 200-microsecond interval in the FM signal after each field.

After detection the reference frequency bursts are visible as small pulses which, regardless of the deviation previously established, represent the sync tip and white regions of the signal. Whether the FM input signal originated in the Modulator (module 207B-S) or from tape playback, the bursts can be used as a reference either to measure the existing deviation or, if need be, to assist in adjusting it to conform to the sync tip and peak white limits indicated by the reference bursts. The control used in setting deviation is designated such and is a screwdriver adjustment on the front panel of the FM Standards (module 205A).

The primary setting of the sync tip frequency is made by adjusting internal controls on the FM Standards (module 205A). The screwdriver control on the front of the Modulator module is a vernier for making fine-tuning adjustments, if needed.

The white reference oscillator and crystal switching circuits are almost identical to those of the sync tip reference, therefore only the latter will be described. (Refer to the simplified schematic diagram, figure 64.)

The sync tip reference generator, Q27, is used in a modified Colpitts oscillator that employs one of the quartz crystals, Y10 to Y13, as a frequency determining element. Each crystal is controlled by one of the switching transistors, Q25, Q26, Q28, Q29, Q30 and Q31. The crystal that is activated by its associated switching transistor is effectively connected, from an ac standpoint, from the base of Q27 to the collector. Capacitive voltage divider C50, C51 feeds back a portion of the voltage appearing across the crystal to the

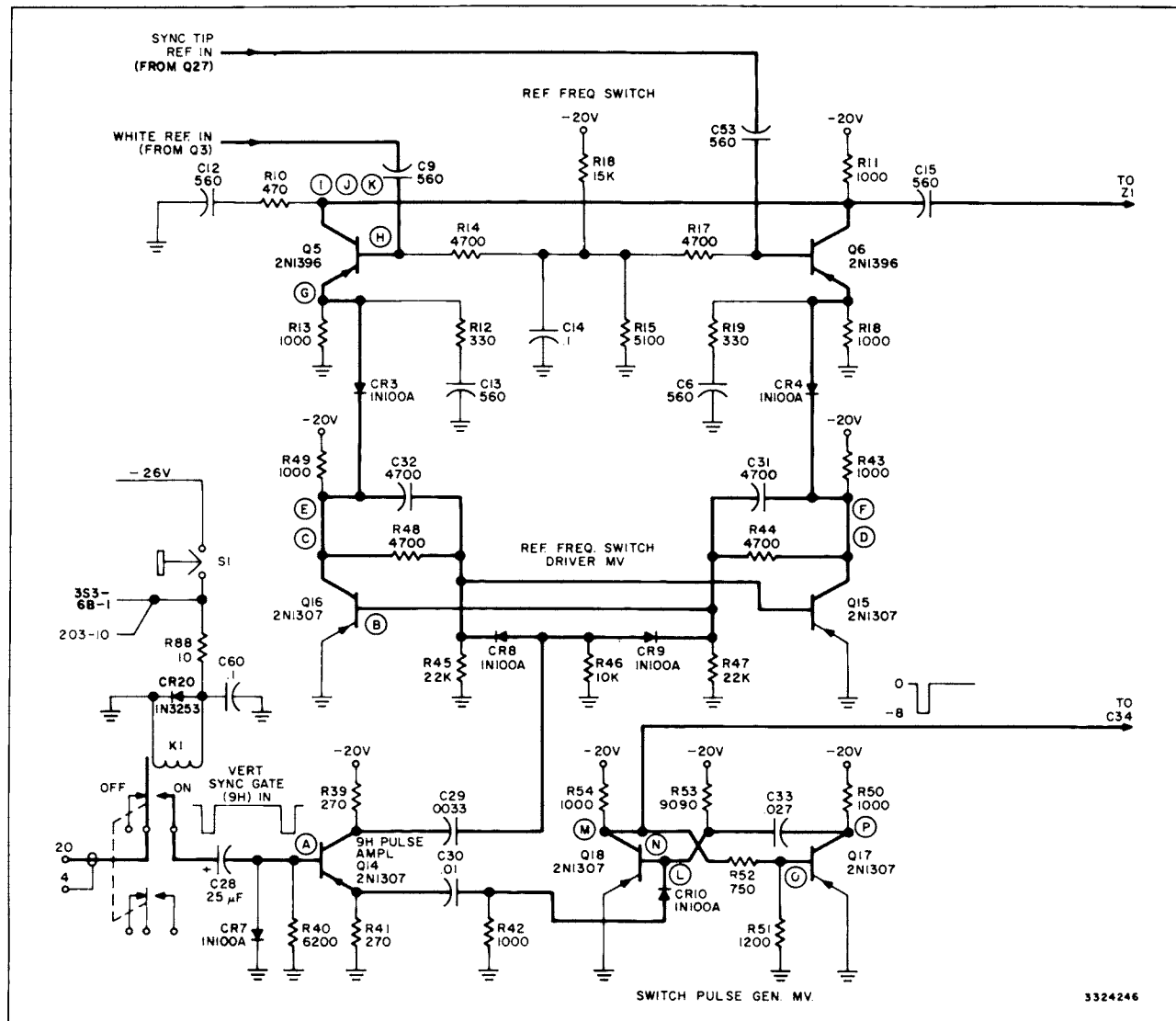


Figure 66—9H Pulse Amplifier, Reference Frequency Switch Driver, Reference Frequency Switch, Switch Pulse Generator and Sync Tip Reference Amplifier Circuits

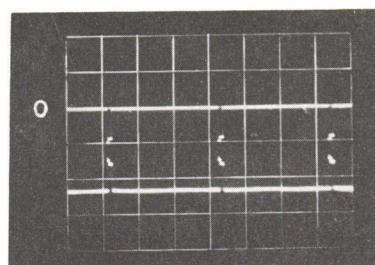
emitter of Q27 to sustain oscillation. The R-C network of R79 and C52 modifies the feedback voltage and phase to insure proper operating conditions. Oscillator stability is further controlled by the diode clipper, CR18, CR19, and C49, which tends to limit the excursion of the signal on the base, so that the amplitude remains constant regardless of crystal activity. Coupling capacitor C48 furnishes dc isolation between the base of Q27 and the crystals. Bias on the base of Q27 is established across R78, R77, both of which in conjunction with the emitter resistor, R80, determine the dc current in Q27. The rf output to the following stages is taken from the low impedance emitter point.

Each of the crystals, Y10 to Y13, is connected from

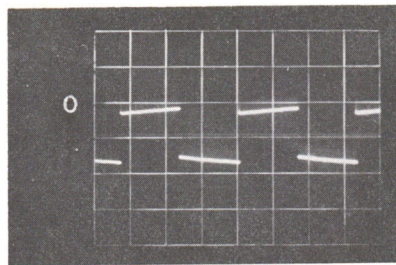
the base of Q27 to individual control transistors, Q25, Q26, Q28, Q29 and Q30. The STDS switch on the FM Standards (module 205A) selects a crystal for reference purposes by feeding a negative current to the base of the control transistor which is in series with the desired crystal. The control transistor saturates, connecting the crystal from the base of Q27 to ground through bypass capacitor C47.

Flexibility of crystal utilization is enhanced by patch board terminals, permitting any crystal to be controlled by a position of the STDS switch, as described in the Reference Crystal Selection Connections section.

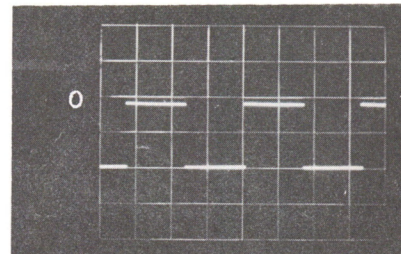
The keying and gating pulses are shown in the



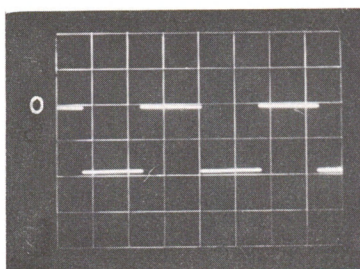
A. Top: Q14 base, 9H, 5 ms/cm, 5v/cm. Bottom: Q14 collector, 5 ms/cm, 5v/cm



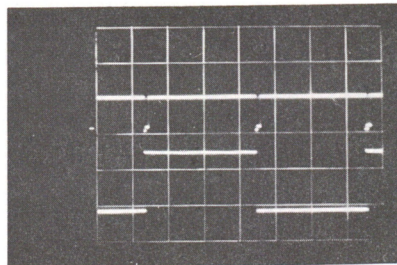
B. Q16 base, 10 ms/cm, .2v/cm



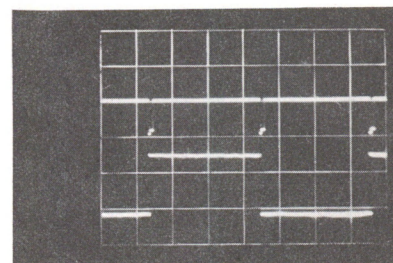
C. Q16 collector, 10 ms/cm, 5v/cm



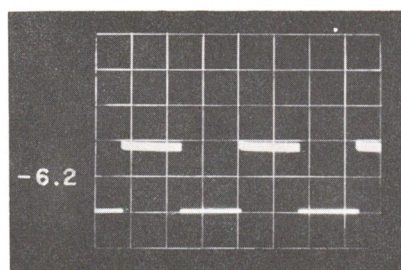
D. Q15 collector, 10 ms/cm, 5v/cm



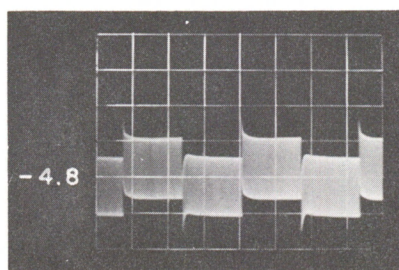
E. Top: Q14 base, 9H reference. Bottom: Q16 collector, 5 ms/cm, 5v/cm



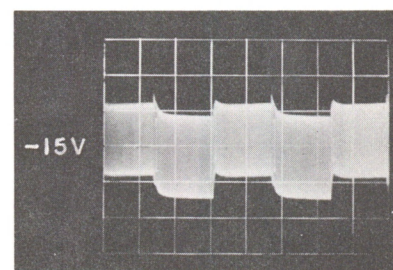
F. Top: Q14 base, 9H reference. Bottom: Q15 collector, 5 ms/cm, 5v/cm



G. Q5 emitter, 10 ms/cm, 2v/cm

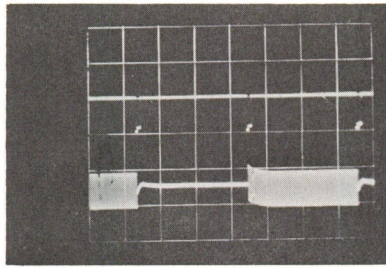


H. Q5 base, 10 ms/cm, .2v/cm

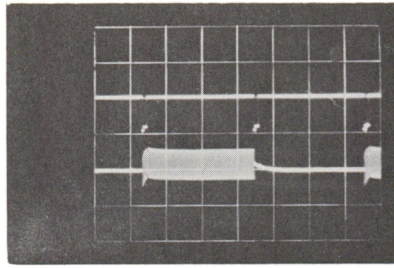


I. Q5 collector, 10 ms/cm, .2v/cm

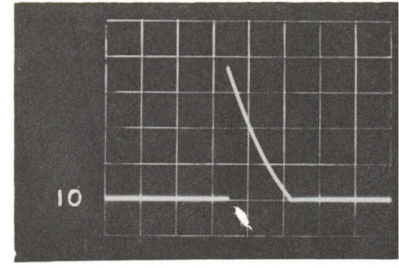
Figure 67—Typical Waveforms; 9H Pulse Amplifier, Reference Frequency Switch Driver, Reference Frequency Switch, Switch Pulse Generator and Sync Tip Reference Amplifier Circuits



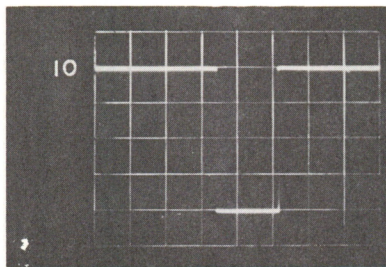
**J. Top: Q14 base, 9H reference.
Bottom: Q5 collector, 4.3 crystal removed, 5 ms/cm, .5v/cm**



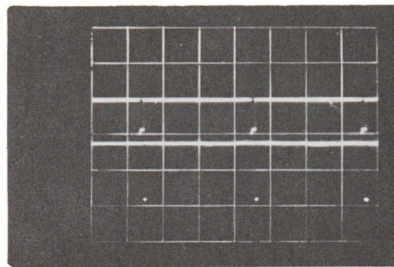
**K. Top: Q14 base, 9H reference.
Bottom: Q5 collector, 6.8 crystal removed, 5 ms/cm, .5v/cm**



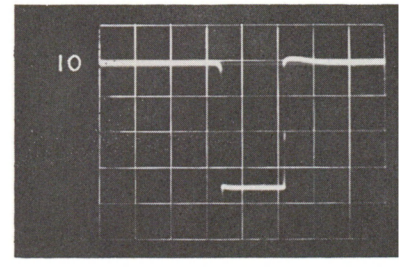
L. Q17 base, 100 μ s/cm, 5v/cm



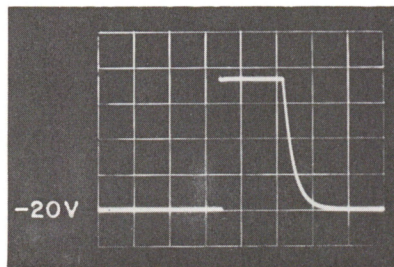
M. Q17 collector, 100 μ s/cm, 2v/cm



**N. Top: Q14 base, 9H reference.
Bottom: Q17 collector, 5 ms/cm, 5v/cm**



O. Q18 base, 100 μ s/cm, .1v/cm



P. Q18 collector, 100 μ s/cm, 5v/cm

Figure 67—Typical Waveforms; 9H Pulse Amplifier, Reference Frequency Switch Driver, Reference Frequency Switch, Switch Pulse Generator and Sync Tip Reference Amplifier Circuits (Continued)

waveform timing chart, figure 65, which includes a graphical representation of the complementary on-off state existing between Z1 and Z2. Their development will be covered as the description continues. Next to be discussed is the manner in which reference switching is accomplished. Refer to the simplified schematic, figure 66.

When K1, the FM reference relay controlled by the front panel pushbutton control is closed, the 9H (vertical sync gate) negative pulse (A, figure 65) from the Sync Logic (module 230B) is fed through coupling capacitor C28 to CR7 and the base of Q14, the 9H pulse amplifier. Diode CR7 clamps the positive excursions of the 9H pulse to ground, causing the

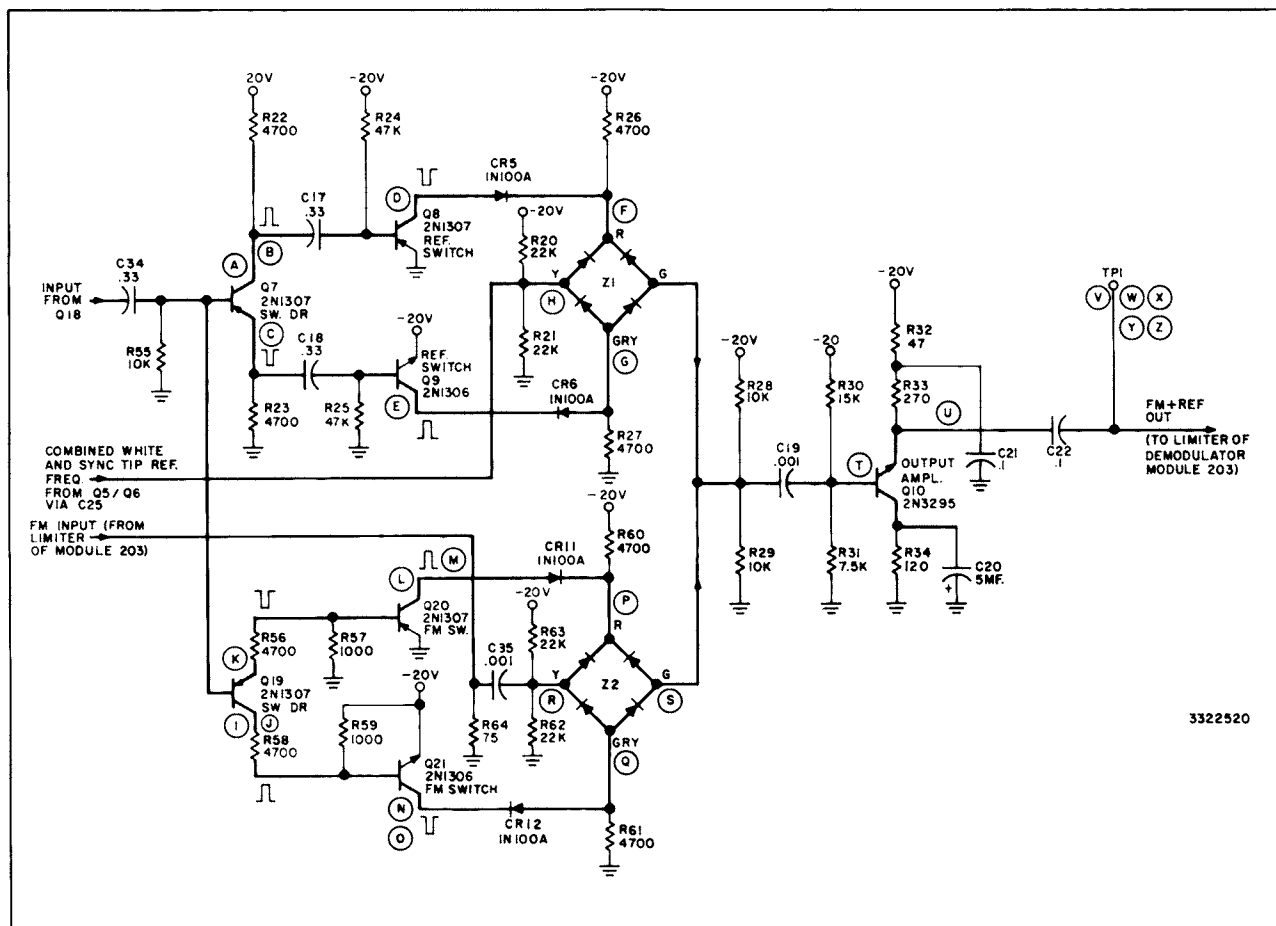


Figure 68—Switch Drivers, FM and Reference Switches, Diode Gates and Output Amplifier Circuits

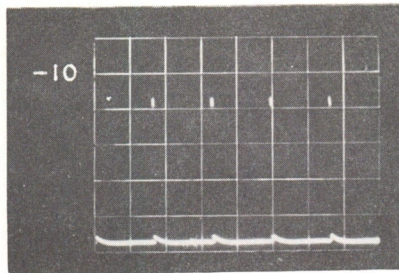
pulses to extend entirely in a negative direction. Transistor Q14 operates as a split load phase inverter, and each pulse appearing on CR7 causes Q14 to conduct heavily, producing a positive pulse across the collector load, R39, and a negative pulse across the emitter load, R41.

The positive-going leading edge of the collector pulse is used to trigger bistable multivibrator Q15, Q16, the reference switch driver. Only the positive transition is conducted by the isolation diodes, CR8 and CR9, tending to cut off Q15 and Q16, whichever had been previously conducting. The multivibrator thus switches state at a field rate, with Q15 conducting during one field and Q16 conducting on the next, as long as the FM REF button is pressed.

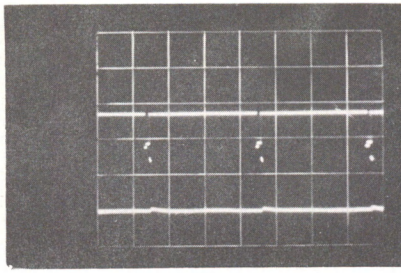
Voltage swings (B and C, figure 65) at the collectors of Q15 and Q16 are direct coupled to the emitters of Q6 and Q5, respectively, through diodes CR3 and CR4. Fixed bias developed by R15 and R16 across -20 volts and coupled through R14 maintains the base of Q5 at approximately -5 volts. When Q15 is

cut off CR3 conducts because of the relatively high negative potential at its cathode. This causes the emitter of Q6 to assume a -10 volt potential since it is connected through CR3 to the center of voltage divider R18, R43. With the base of Q5 biased to -5 volts and the emitter at -10 volts, the transistor is cut off, preventing amplification of the sync tip reference frequency at its base. This condition exists for an entire field during which time Q15 is cut off and Q16 is saturated. At the end of the field, the multivibrator is triggered to a new state and Q15 becomes saturated and Q16 is cut off. When this occurs, the cathode of CR3 becomes grounded, but the anode is connected to the negative potential at the emitter of Q6. Thus, CR3 is cut off, and Q6 is permitted to function as a conventional amplifier.

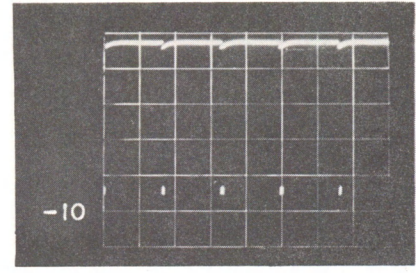
The collector current of Q6 is thus keyed on and off at a field rate by Q15, so that the sync tip reference frequency appears on the collector of Q6 on every other field, as shown in D, figure 65. During the field interval when Q6 is cut off by Q15, Q16 causes Q5 to conduct and amplify the white reference



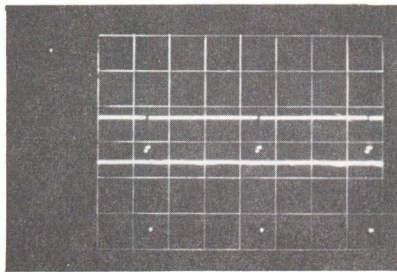
A. Q7 collector, 10 ms/cm, 2v/cm



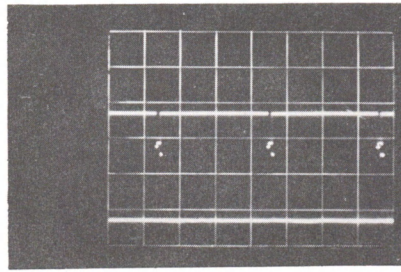
**B. Top: Q14 base, 9H reference.
Bottom: Q7 collector, 5 ms/cm, 5v/cm**



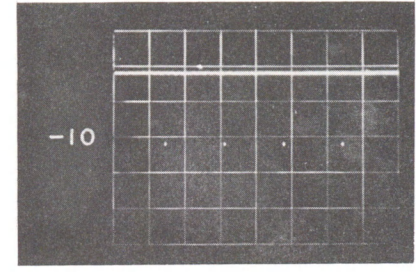
C. Q7 emitter, 10 ms/cm, 2v/cm



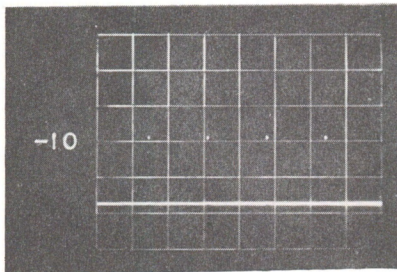
**D. Top: Q14 base, 9H reference.
Bottom: Q2 collector, 5 ms/cm, 5v/cm**



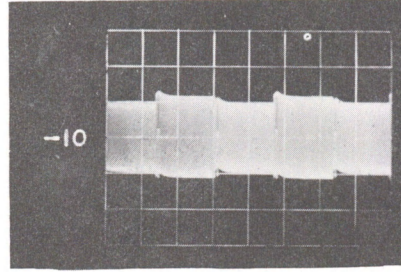
**E. Top: Q14 base, 9H reference.
Bottom: Q9 collector, 5 ms/cm, 5v/cm**



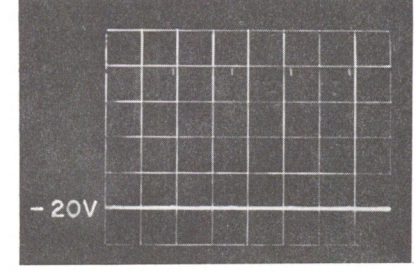
F. Z1 red, 10 ms/cm, 5v/cm



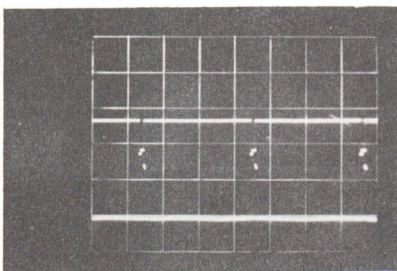
G. Z1 gray, 10 ms/cm, 5v/cm



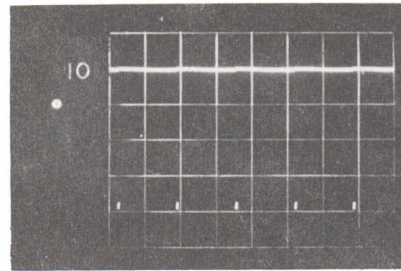
H. Z1 yellow, 10 ms/cm, .2v/cm



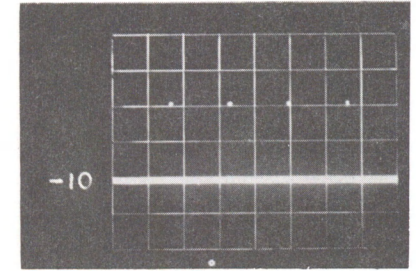
I. Q19 collector, 10 ms/cm, 2v/cm



**J. Top: Q14 base, 9H reference.
Bottom: Q19 collector, 5 ms/cm, 5v/cm**

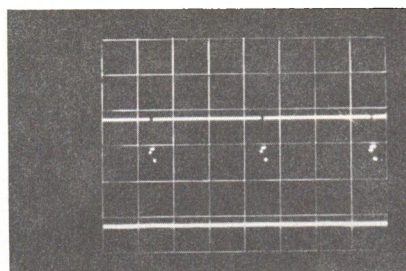


K. Q19 emitter, 10 ms/cm, 2v/cm

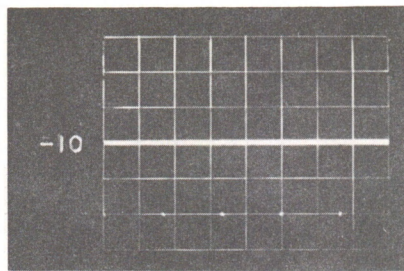


L. Q20 collector. 10 ms/cm, 5v/cm

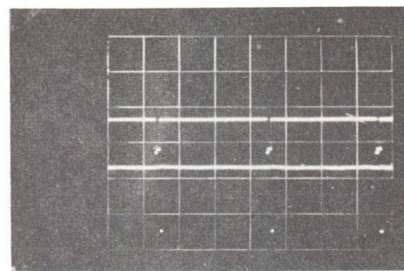
Figure 69—Typical Waveforms; Switch Drivers, FM and Reference Switches, Diode Gate and Output Amplifier Circuits



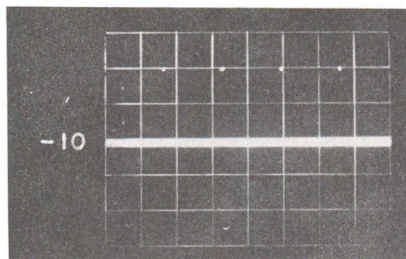
M. Top: Q14 base, 9H reference.
Bottom: Q20 collector, 5 ms/cm, 5v/cm



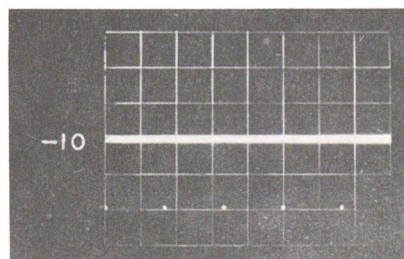
N. Q21 collector, 10 ms/cm, 5v/cm



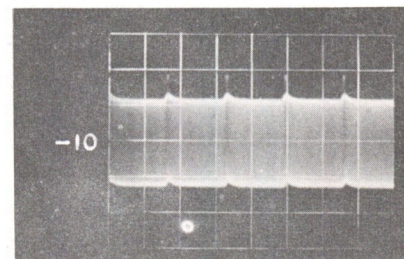
O. Top: Q14 base, 9H reference.
Bottom: Q21 collector, 5 ms/cm, 5v/cm



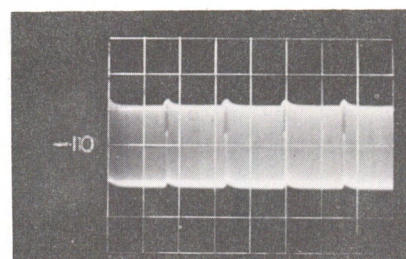
P. Z2 red, 10 ms/cm, 5v/cm



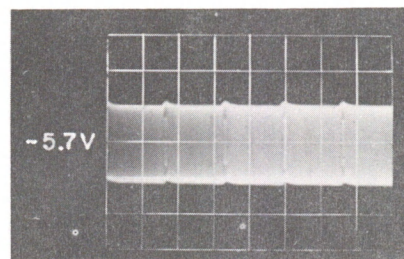
Q. Z2 gray, 10 ms/cm, 5v/cm



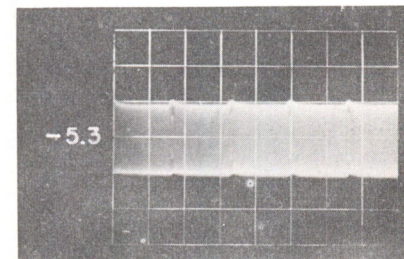
R. Z2 yellow, 10 ms/cm, .2v/cm



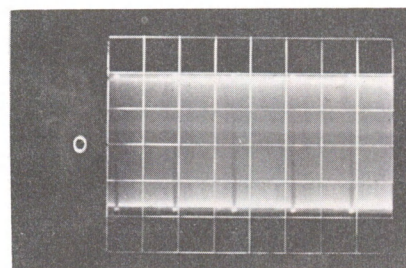
S. Z2 green, 10 ms/cm, .2v/cm



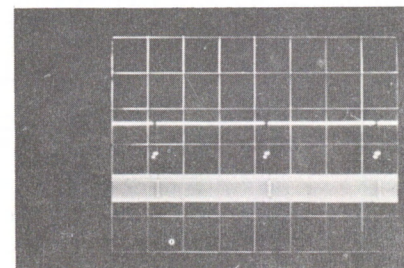
T. Q10 base, 10 ms/cm, .2v/cm



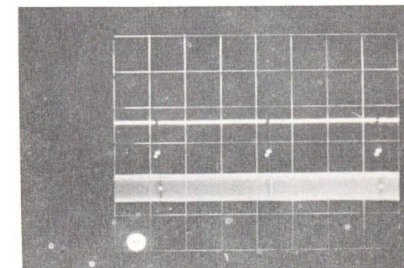
U. Q10 emitter, 10 ms/cm, .2v/cm



V. TP1, 10 ms/cm, .1v/cm

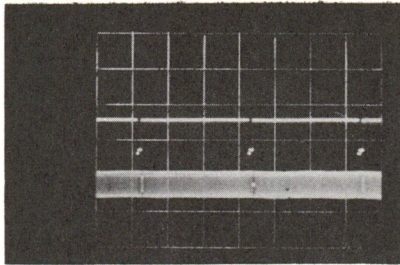


W. Top: Q14 base, 9H reference.
Bottom: TP1, 5 ms/cm, .5v/cm

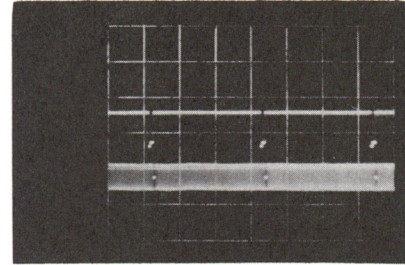


X. Top: Q14 base, 9H reference.
Bottom: TP1, 4.3 mc crystal removed, 5 ms/cm, .5v/cm

Figure 69—Typical Waveforms; Switch Drivers, FM and Reference Switches, Diode Gate and Output Amplifier Circuits (Continued)



**Y. Top: Q14 base, 9H reference.
Bottom: TP1, 6.8 mc crystal
removed, 5 ms/cm, .5v/cm**



**Z. Top: Q14 base, 9H reference.
Bottom: TP1, 4.3 mc and 6.8
mc crystals removed, 5 ms/cm,
.5v/cm**

**Figure 69—Typical Waveforms; Switch Drivers, FM and Reference Switches,
Diode Gate and Output Amplifier Circuits (Continued)**

frequency as in E, figure 65. The output of Q6 and Q5, combined in the common load resistor, R11 (F, figure 65), is thus a signal changing in frequency from sync tip reference to white reference on alternate fields.

Short bursts of the composite reference signal are keyed into the FM signal from the modulator on the tape playback by the switching pulse generator, Q18, Q17, a monostable multivibrator (figure 66). The generator exists in a quiescent state with Q18 saturated and Q17 cut off, until triggered by the pulse at the emitter of Q14. During the interval between triggers, negative current supplied to the base of Q18 through R53 keeps this transistor saturated; Q17 is kept cut off because the base bias resistors, R52 and R51, are at ground potential. When a 9H pulse appears on the emitter of Q14 the positive-going trailing edge is coupled through isolation diode CR10 to the base of Q18, driving it towards cutoff. Regenerative feedback between Q18 and Q17 increases the speed of the transition taking place as the multivibrator changes state until Q18 is cut off and Q17 saturated. The multivibrator remains in this state, with Q18 cut off and Q17 saturated, for approximately 200 microseconds. This period is determined by the time constant of the charging network formed by R53 and C33. At the end of 200 microseconds, C33, charging through R53 towards -20 volts, has acquired sufficient negative potential to once again cause Q18 to conduct. The remainder of the time, the collector of Q18 is near ground potential as illustrated by G, figure 65.

This pulse ultimately determines the duration and location of the reference frequency bursts. Its amplitude depends on the voltage division effected by R54 and R52 across -20 volts when Q18 is cut off; the peak negative excursion is therefore approximately 8 volts. From the collector of Q18 the negative keying pulse is coupled through C34 to the bases of Q19 and Q7, the switch drivers, both of which are phase splitters.

The next part of this discussion covers the operation of the diode gates, Z1 and Z2, and the driving and the switching circuits associated with them (see figure 90).

To begin, consider first the state of phase splitter Q19 and the two FM switches, Q21 and Q20, it drives, during the intervals, between keying pulses. At this time the slight positive signal potential cuts off Q19 so neither FM switch can conduct. Transistor Q20 is turned off because the base bias resistor, R57, is returned to ground and R56 is floating. Q21 is cut off because the base bias resistor, R59, returns the base directly to the emitter and no current flows in R58. Since Q21 and Q20 are cut off, the diodes in series with the collector of each, CR11 and CR12, respectively, are non-conducting. Thus, the diode quad, Z2, is completely isolated and the conduction of the diodes in the quad depends only on bias furnished by the associated resistors. These conditions are illustrated in A, figure 70.

The bias at the Y terminal of Z2 is -10 volts as developed by R63 and R62 across -20 volts. The G

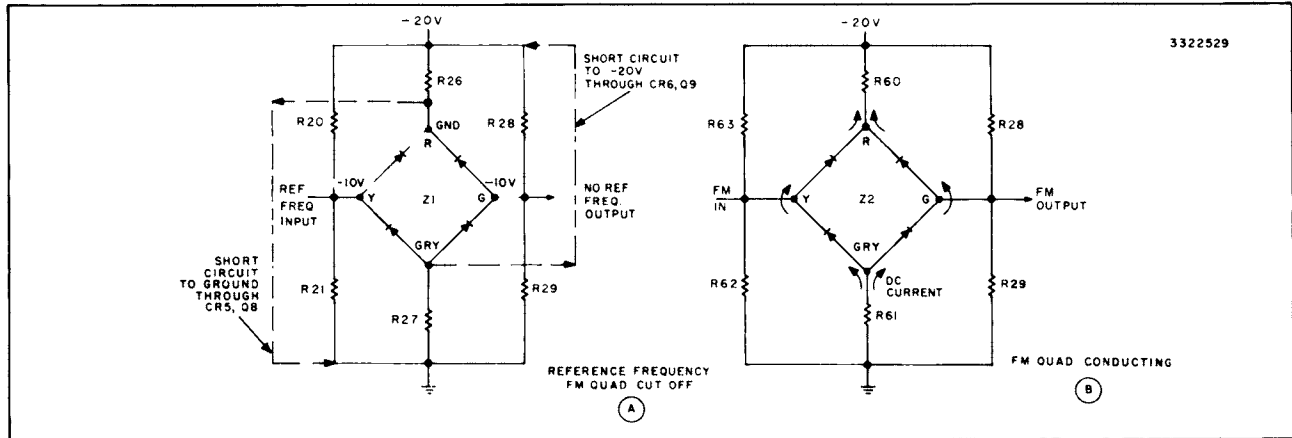


Figure 70—Condition of Z1 and Z2 During Absence of Keying Pulse

terminal is also returned to -10 volts as determined by R28 and R29. The upper pair of diodes will conduct because their cathodes are returned to -20 volts through R60. Finally, the lower pair of diodes will conduct by virtue of their return to ground through R61. Because all the diodes in Z1 are heavily conducting, the Y terminal is effectively connected to the G terminal, and FM fed in at Y passes freely through the quad to the output emitter follower, Q10. As

shown in B, figure 70, the FM reference quad, Z1, is turned off for the period Z2 is on.

When a negative keying signal arrives at the base of Q19 this transistor is driven into saturation. The output signals of Q19, negative on the emitter, positive on the collector, (H and I, figure 65) are transferred to the bases of Q20 and Q21, respectively, driving both into saturation. With both Q20 and Q21 saturated (J and K, figure 65), CR11 and CR12 are

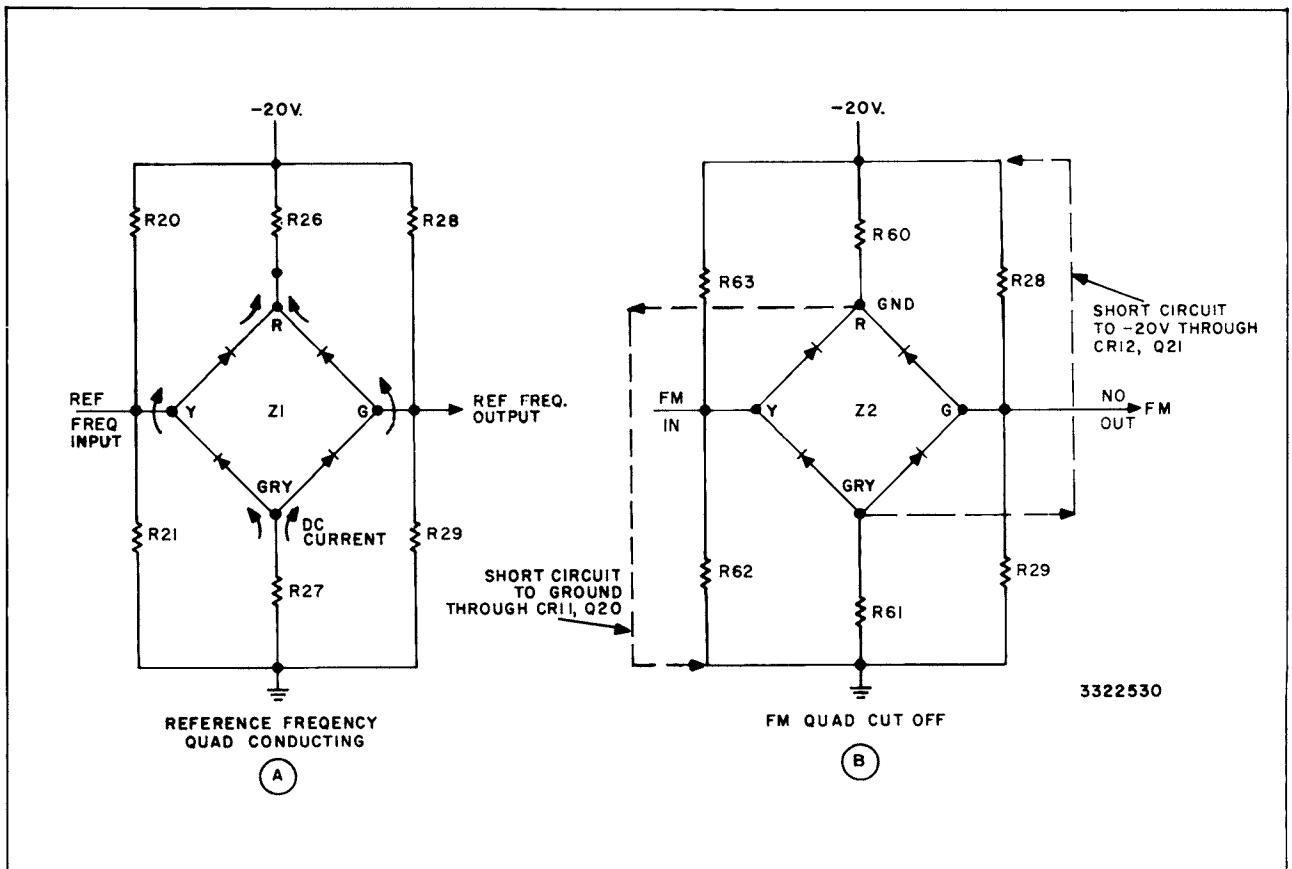


Figure 71—Condition of Z1 and Z2 During Presence of Keying Pulse

returned to ground and -20 volts, respectively. As shown in A, figure 71, the cathodes of the two quad diodes connected to terminal R now go to ground through CR11 and Q20, while the anodes of the two quad diodes connected to the GRY terminals are returned via CR12 and Q20 to -20 volts. Thus all four diodes in Z2 are cut off and passage through the quad of the FM signal at terminal Y is blocked. In addition, low impedances to ground presented by CR11, CR12, Q21, and Q20 further reduces transmission of the FM signal through the quad due to the shunting effect of these components. The complementary switching action between Z2 and Z1 that results in the combined output signal is demonstrated by L, M, and N, figure 65.

The foregoing analysis of Z2 can be also applied to the operation of the reference frequency quad, Z1, to show that Z1 is switched on and off in a complementary fashion to Z2. That is, during the keying pulse period when Z2 is switched off, Z1 is turned on (B, figure 71). Conversely, during the interval between keying pulses, or when the FM REF pushbutton is not pressed, Z2 conducts, passing the FM signal through to the output amplifier, Q10, while Z1 remains cut off.

When the FM REF pushbutton is pressed, Z2 and Z1 switch on and off alternately and the output of each is combined into one continuous signal. This signal consists of program FM into which has been inserted at a field rate short bursts of standard sync tip frequency and standard peak white frequency. Which reference frequency is present is, of course, dependent on the state of the reference switch, Q6, Q5, composite output.

The output amplifier, Q10, is an emitter follower, which is biased by R30, R31, and R34. The voltage drop across Q10 is limited by the collector load, R33 which is bypassed by C21. The output from the emitter is coupled through C22 and fed to the demodulator (module 203B), where it is terminated at 75 ohms.

REFERENCE CRYSTAL SELECTION CONNECTIONS

Domestic Standards

As shown in figure 72, there is one patch jumper in the FM Reference module for each position on the STDS switch in the Domestic FM Standards (module 205A). On the terminal boards in the FM Reference module there are six groups of terminals, one group

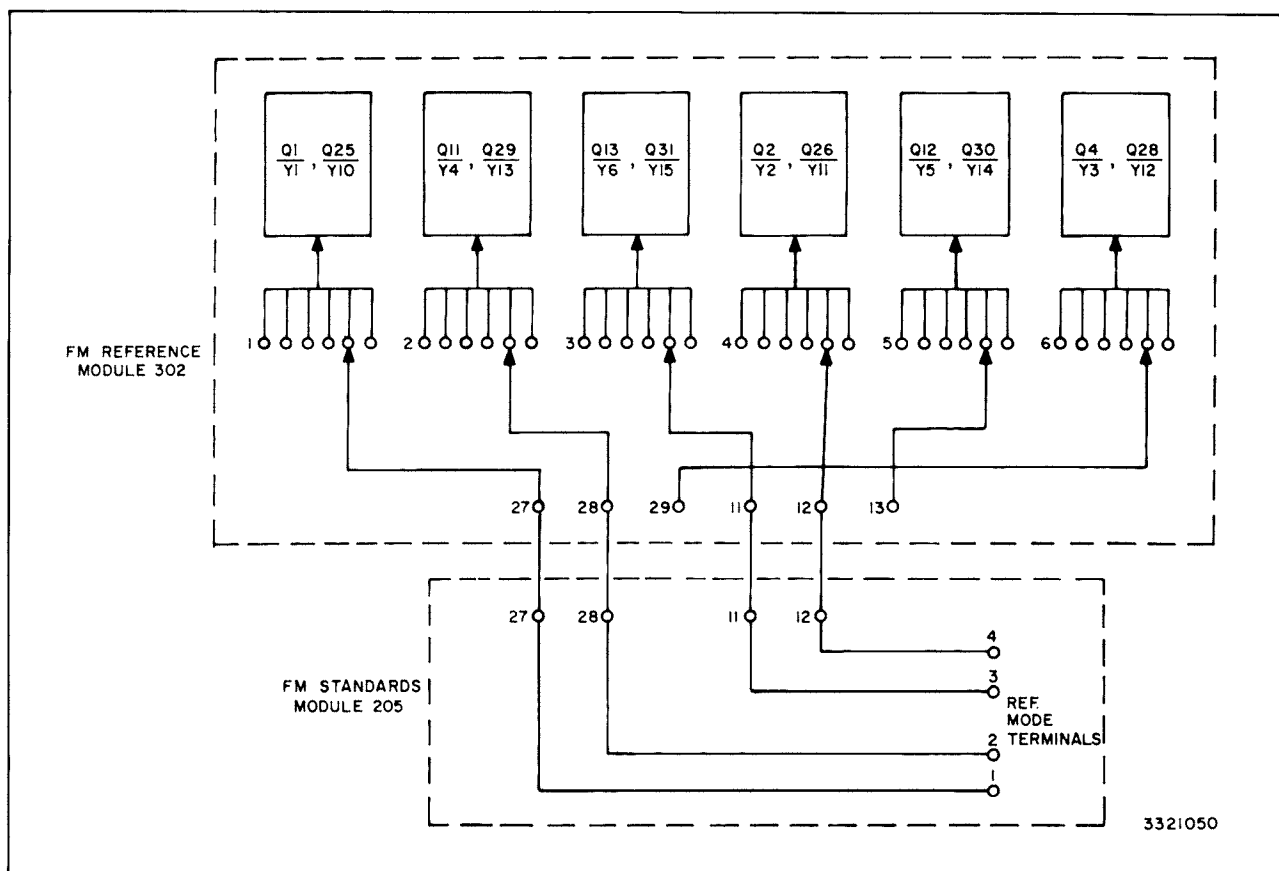


Figure 72—Reference Crystal Connections for Use With FM Standards Module

for each pair of reference crystal control transistors. Each group consists of six terminals connected in parallel.

A particular position on the STDS switch can be made to activate any pair of crystals desired. This is done by soldering the jumpers from the switch contact terminals to two terminals in the group associated with the desired pair of crystals. It is also possible to use more than one position on the STDS switch to control the same pair of crystals. In this case all the jumpers from the switch contacts to be used are wired to an equal number of terminals in the group corresponding to the pair of crystals to be activated.

The normal arrangement as wired uses the first three positions on the STDS switch to select the monochrome standards crystals, Y1, Y10 or Y15 or Y3, and the last two positions to select the color standards crystals, Y4, Y13.

As evidenced from the preceding information, other combinations also can be devised, as needed, to meet the requirements of a particular installation, such as different international standards.

A 20-volt signal is developed in the FM Standards module and fed through one of the patch jumpers to activate the correct pair of reference crystals. This control signal is based on the video line standard selected.

The method used to derive the control signal is covered in the FM Standards module description, elsewhere in this book.

DEMODULATOR (Module 203B)

GENERAL (Refer to Figure 73)

The Demodulator module performs two basic functions along with others of less importance which will be mentioned in order of processing of the signals. The left side of the module contains mostly circuitry involved with amplification and limiting of the FM signal. The right side module board is concerned mainly with the actual Demodulation process, i.e., conversion of FM signals back to Video.

In the STOP mode the FM signal from the modulator may be passed on to the Limiter and Demodulator for an actual check on the performance of that part of the system. The Demodulator output may be actually viewed on the picture monitor. This is done by selection of the MOD-DEMODO position of the switch so labeled on the PLAY panel. Relays and switches activate the required circuitry to perform the

function. The picture monitor switcher will then show the modulation and demodulation of the signal if the DEMOD OUT button is depressed. If the VID OUT button is depressed the signal will also go on through the processing amplifier for a check of its performance, also in the STOP mode.

Another function of the module is to provide amplified and limited FM signal, with facility to drive the record amplifiers of another tape machine in the dubbing process. This can be done without going into an intermediate demodulation-modulation process. This is known as the RF copy technique and is sometimes used where many machines are driven as "slaves" in dubbing a large number of copies simultaneously. The R.F. copy circuits will be discussed later.

The Limiter amplifies the input from either of two sources, the Record FM signal from the Modulator (module 207B-S) or the Tape FM signal from the FM equalizer circuit in the FM Equalizer (module 132).

As shown in the upper part of the block diagram, figure 73, the Limiter consists of an input selection relay (K1) with relay driver, an interlocking relay (K2), four push-pull limiter stages, a phase combiner and two output stages comprising a demodulator driver and an R-F Copy output.

The four limiter stages are similar. Each stage is a differential amplifier, with each half of the amplifier coupled by an emitter follower to the succeeding stage. The gain is approximately 15 db per stage, with overall limiting of at least 55 db for 1 volt input. To insure symmetrical clipping, a balance control is employed in the first three limiter stages. The push-pull output from the final limiter is fed to a phase combiner. The output of the phase combiner is a single phase signal that goes to an isolation emitter follower which feeds two more emitter follower stages. One drives the Demodulator and the other feeds the R-F Copy line driver stage which goes through switch S1, if used, to the machine output connector 12J14.

CIRCUIT

Input Signal Selection

The function of K1 (figure 74) is to select either the record FM signal or the tape FM signal from the playback circuits. When in the RECORD or SETUP mode of operation, K1 selects record FM; in the PLAY mode, K1 selects tape FM. If the machine is in STANDBY, WIND, or STOP modes, K1 will select either record FM or the zero signal output of the

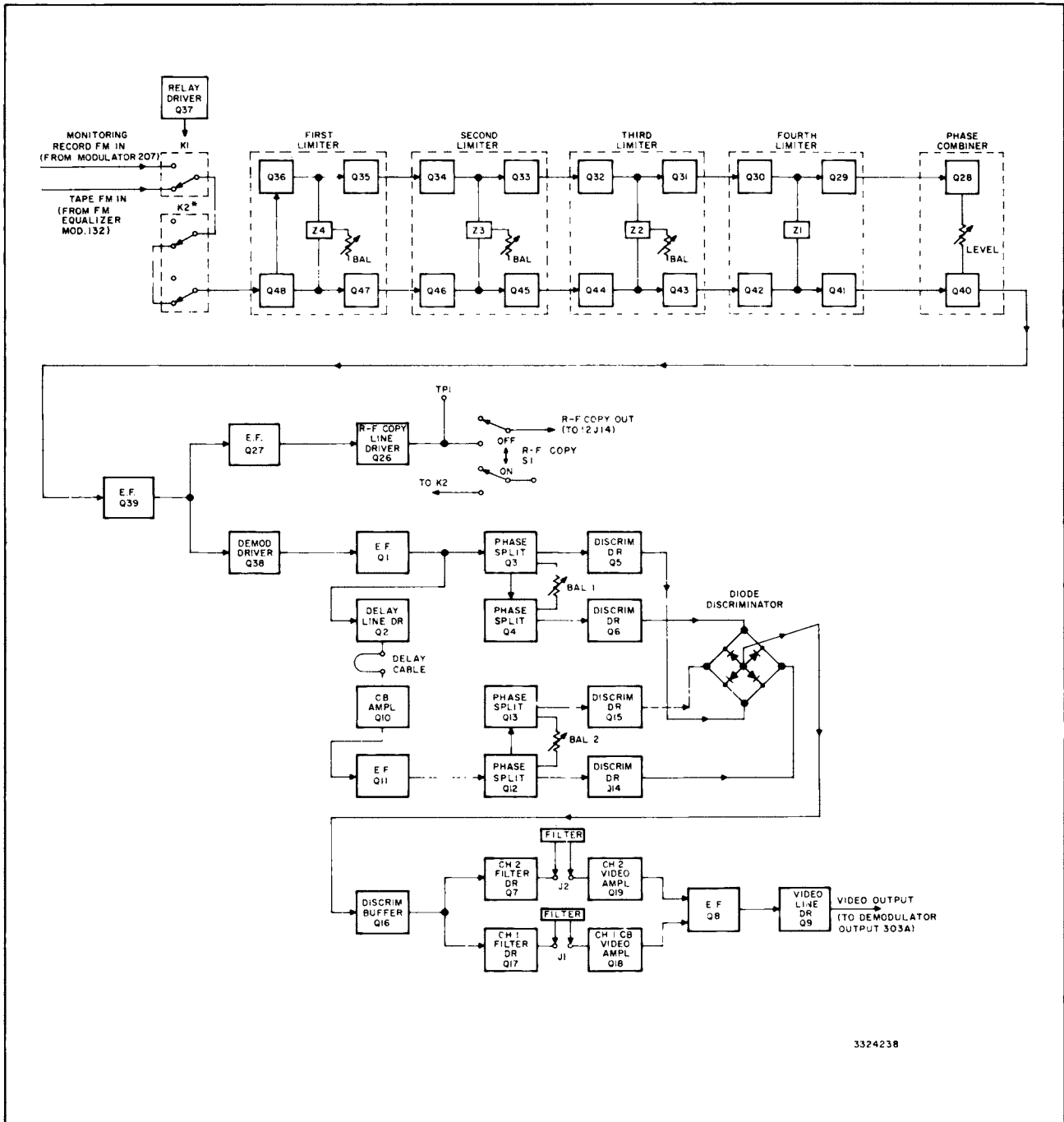


Figure 73—Block Diagram, Demodulator Module

video heads. The choice between these two signals is determined by the position of the MOD-PLAY switch, which is a control on the PLAY control panel. For a detailed discussion on the operation of this switch, see sections entitled *-20 Volts Switch* under *Modulator (module 207B-S)* description.

Relay K2 serves as a protective interlock in providing a path for the input when the FM Reference (module 302A) is removed, and for preventing the

FM reference signal from being added when a tape is being played for R.F. copy purposes.

With the input selection relay, K1, and relay K2, de-energized, as shown in figure 74, K1 would accept the Tape FM signal from the FM Equalizer module that appears on pin 18 of the module connector. The signal would go through K1 to K2. The signal would follow the path through the jumpered contacts on K2 to the base of Q48, the input of the first limiter.

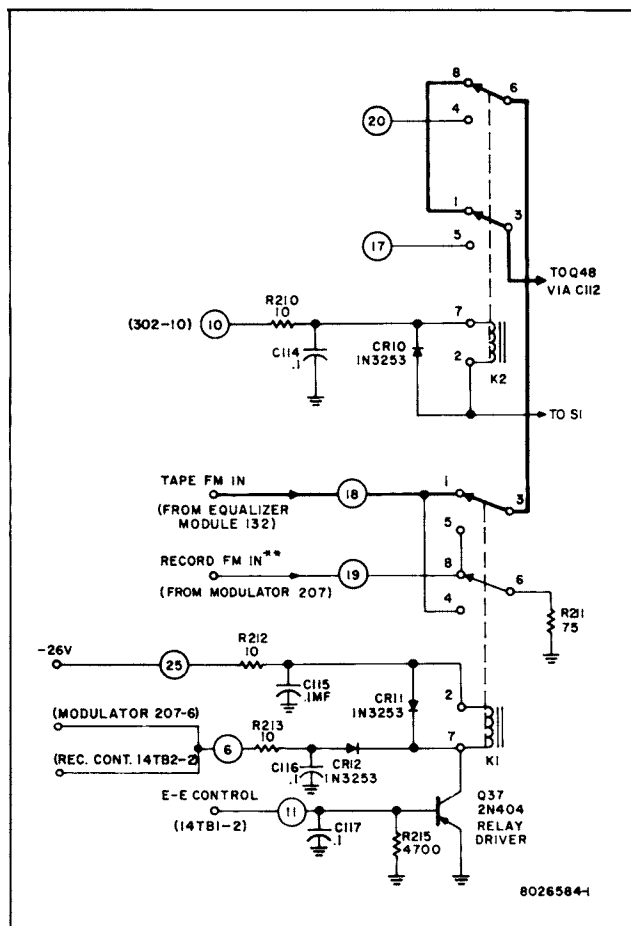


Figure 74—Input Signal Selection Circuit

When K1 is energized, the Record FM signal from the Modulator module is applied to K1 through pin 19 on the module connector. From K1 the signal goes through the still-closed loop provided by K2 to the base of Q48 via C112.

Regardless of the state of K1, the coaxial input lines are properly terminated at all times by R211 (figure 74) and by R203 (figure 75). The former terminates the unused signal input line to K1 and the latter provides input termination of the signal being applied to the base of Q48, the input of the first limiter.

The input selection relay, K1 is controlled by the relay driver, Q37, or the RECORD/SETUP bus. In the STANDBY, WIND or STOP modes with the MOD-PLAY switch in the MOD position, negative voltage from the E-to-E bus saturates Q37, driving the collector to ground. This energizes K1 and it switches to the Record FM input. In the RECORD or SETUP modes, the RECORD/SETUP bus is grounded and this supplies the ground return to the coil of K1 through CR12. Again K1 is energized and switches to the Record FM input signal.

Limiters, Phase Combiner, and Output

Since the four limiter stages are similar, with the exception of the balance control circuits in the first three limiter stages, only the first limiter will be covered in the following discussion (see figure 75).

Transistors Q36 and Q48 form the two halves of a push-pull stage generally known as a differential or emitter coupled amplifier. As mentioned earlier, the incoming signal, Tape FM or Record FM, is coupled through C112 to the base of Q48. The input signal is distributed across both halves of the amplifier by coupling the signal on the emitter of Q48 through C107 and R194 to the emitter of Q36.

The push-pull signals on the collector of Q36 and Q48 are clipped close to their ac axes by the pair of back-to-back diodes in Z4 (see figure 77). Each diode conducts alternately on the half cycles when the amplified input signal causes the collector-to-collector potential to exceed the forward conduction voltage of the diodes, which is approximately 1 volt. When the diodes conduct, the signal swing on each collector is limited and the positive and negative peaks are clipped at approximately 0.5 volt. The clipped output from each half of the first limiter is coupled to the succeeding stage through emitter followers, with Q36 driving Q35 and Q48 driving Q47. In the remaining three limiter stages, the signal is further amplified and clipped. In the next three limiters, clipping again takes place at the 0.5 volt level.

The BALANCE control, potentiometer R208, is a front panel screwdriver adjustment. This control is used to set the bias between both halves of the clipper Z4, in order to establish symmetrical clipping of the amplifier output signal. When the input signal is symmetrical, the setting of the BALANCE control is such that the dc bias at the junction of R192 and Z4, is equal to the dc bias at the junction of R193 and Z4. Should the input signal be asymmetrical (A, figure 78), the BALANCE control can be adjusted to vary the bias on the clipper Z4, so as to shift the relation between the ac axes of the signal with respect to the clipping level to achieve a symmetrical output, as shown in B, figure 78. Symmetrical output is necessary for proper operation of the Demodulator. Balance controls R206, and R205, are internal module controls and function as above but during normal operation do not require adjustment.

The push-pull output of the fourth limiter is coupled to the bases of the phase combiner transistors Q28 and Q40 (see figure 79). Although at any instant the signal on the base of Q28 is opposite in phase to

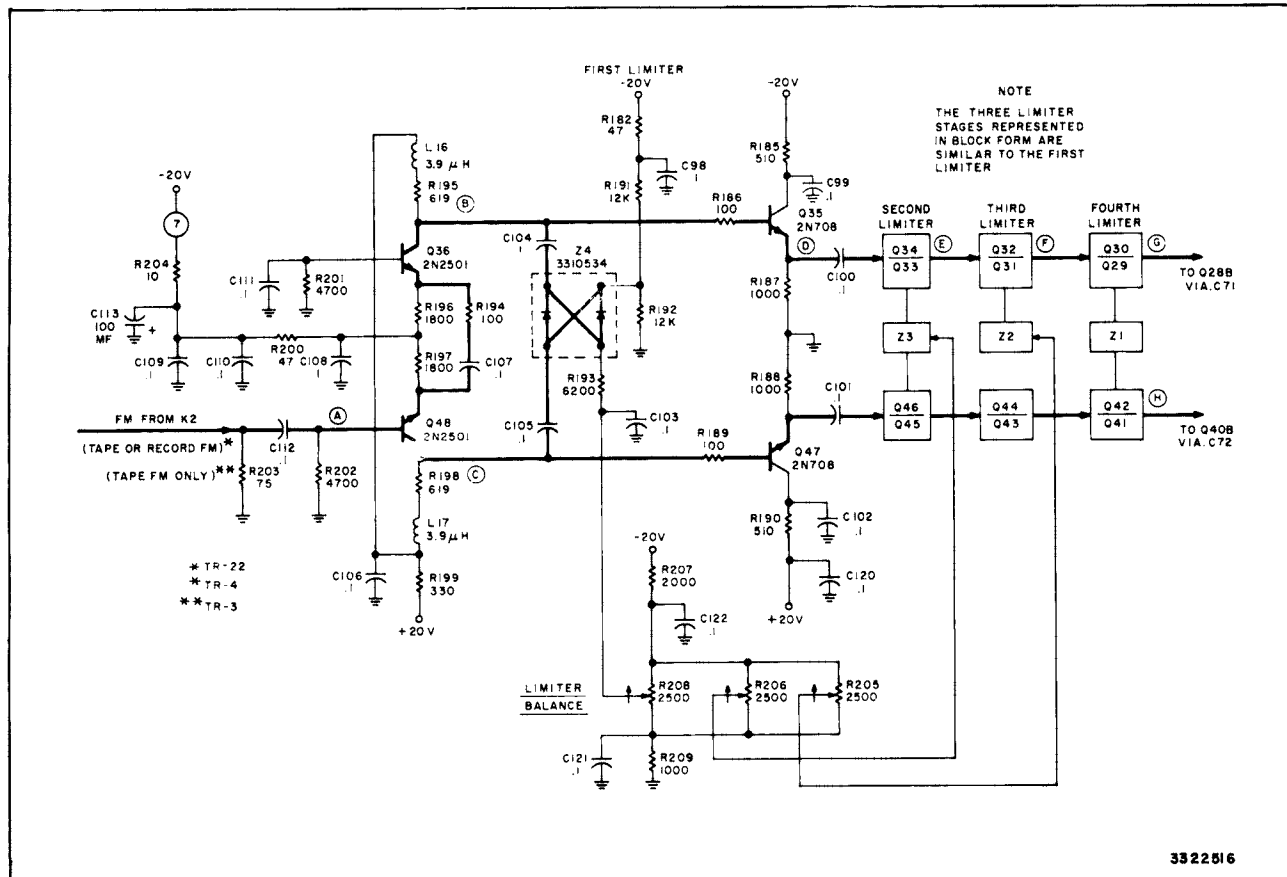


Figure 75—Amplifier and Clipper Circuits

that on Q40, phase reversal between the input and output to each half of the phase combiner takes place only in Q40. The output of Q28 is effectively added in phase with the output of Q40 at the collector of Q40, to produce a combined single phase output. The gain of the system is adjusted by level control R122. This is normally adjusted only during the limiter adjustment procedure.

The output of Q40 is fed to an emitter follower Q39, which in turn drives two other emitter followers, Q38 and Q27. Q38 drives the input transistor, Q1 of the demodulator section. Q27 drives the R.F. Copy Line Driver, Q26. The output of Q26 goes through S1, R.F. Copy Switch, and on to the R.F. Copy output jack, 12J14 if the machine is used in the R.F. Copy mode.

The output impedance of Q26 and the 68-ohm series resistance of R107 provide a source impedance of 75 ohms for the RF Copy output, which is available at 12J14. The RF Copy output level is nominally 1 volt when driving a 75-ohm load. The demodulator drive signal is fed at a 2-volt level to the Demodulator section where video information is subsequently recovered from the FM signal.

DEMODULATION

General

The Demodulator detects the video information contained in the FM output of the Limiter. As shown in the lower part of the block diagram, figure 73, the FM signal from the limiter is coupled through an emitter follower and then split into two branches, one delayed, the other undelayed. The signal in both branches is fed to similar pairs of phase splitters. Except for the phase shift encountered by the delayed signal, both signals are identical when applied to their respective phase splitters. The output signal from each of the four phase splitters is coupled through an individual discriminator to form the gating input to the diode discriminator.

The configuration of the discriminator is such that each diode will conduct, in turn, during the time a delayed and an undelayed signal are both positive. Since two positive signals, one delayed, the other undelayed, are required for a diode to conduct, the output of the discriminator will be a series of constant-width positive pulses at twice the frequency of the input signals. However, the interval between the out-

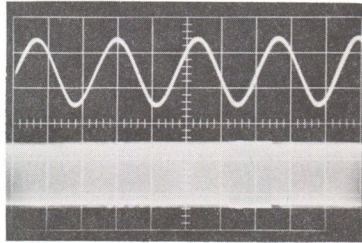
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put pulses is inversely proportional to the frequency of the gating signals. Thus, as the frequency of the gating signals increases, the interval between the output pulses becomes smaller, causing the average energy content to become increasingly positive. Conversely, as the frequency of the gating signals decreases, the interval between the pulses becomes greater and their average contents becomes less positive. The pulse output of the discriminator is fed through a buffer stage to either of two emitter followers, which serve as drivers for two separate filters.

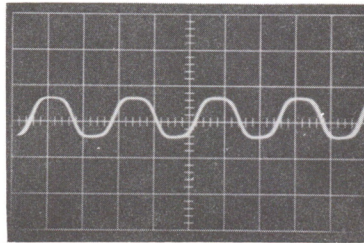
Only one filter channel is used at a time. The channel in use is determined by the standards on which

the TR-22 is being operated. The filter in channel one meets the frequency requirements for domestic standards. The filter in channel two is used for operation on international standards, and is designed to pass frequencies of a slightly higher order than those encountered on domestic standards. Filtering removes unwanted residual high frequency components, supplying a signal at the output that is a varying dc average of the pulse input. Since the dc variations in the filtered signal are proportional to the frequency of the input pulses, the output signal is a replica of the original video modulating signal.

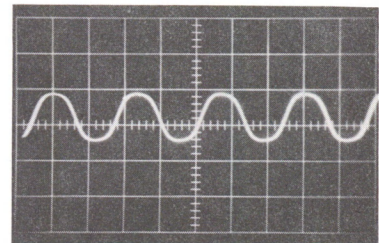
The output of the appropriate filter is fed to its re-



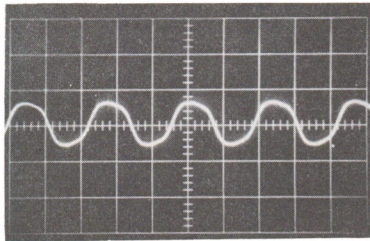
A. Top: Q48 base, $.1 \mu\text{s}/\text{cm}$, $.2\text{v}/\text{cm}$. Bottom: Q48 base, $1 \text{ms}/\text{cm}$, $.2\text{v}/\text{cm}$



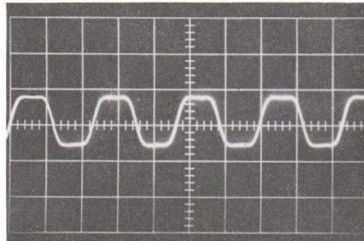
B. Q36 collector, $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



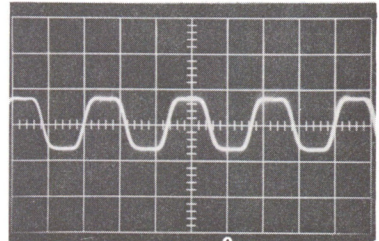
C. Q48 collector, $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



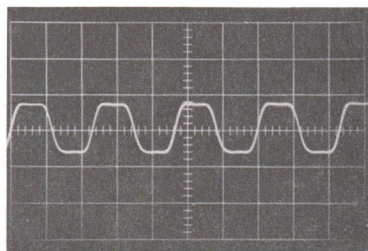
D. Q35 emitter (Q47 emitter inverted), $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



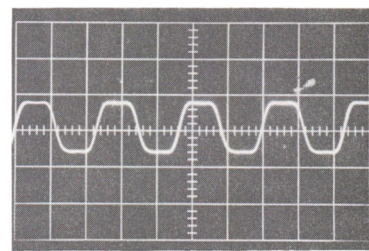
E. Q33 emitter (Q45 emitter inverted), $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



F. Q31 emitter (Q43 emitter inverted), $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



G. Q29 emitter, $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



H. Q41 emitter, $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$

Figure 76—Typical Waveforms; Amplifier and Clipper Circuits

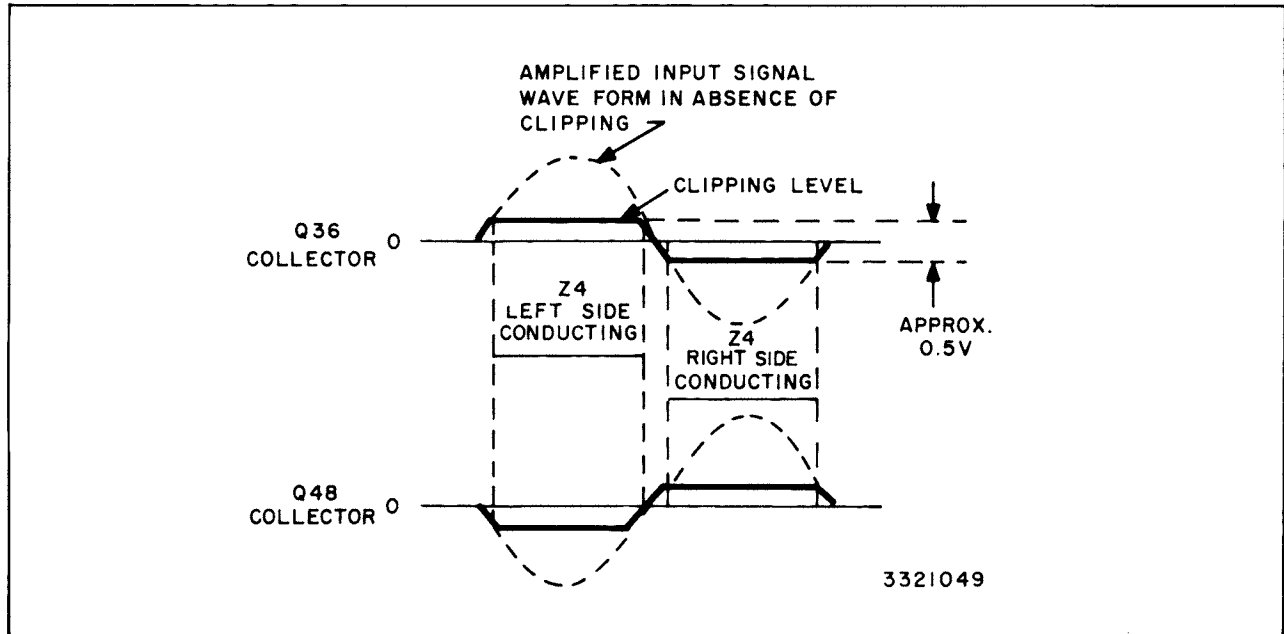


Figure 77—Waveforms showing Conduction Cycle of First Limiter Diodes

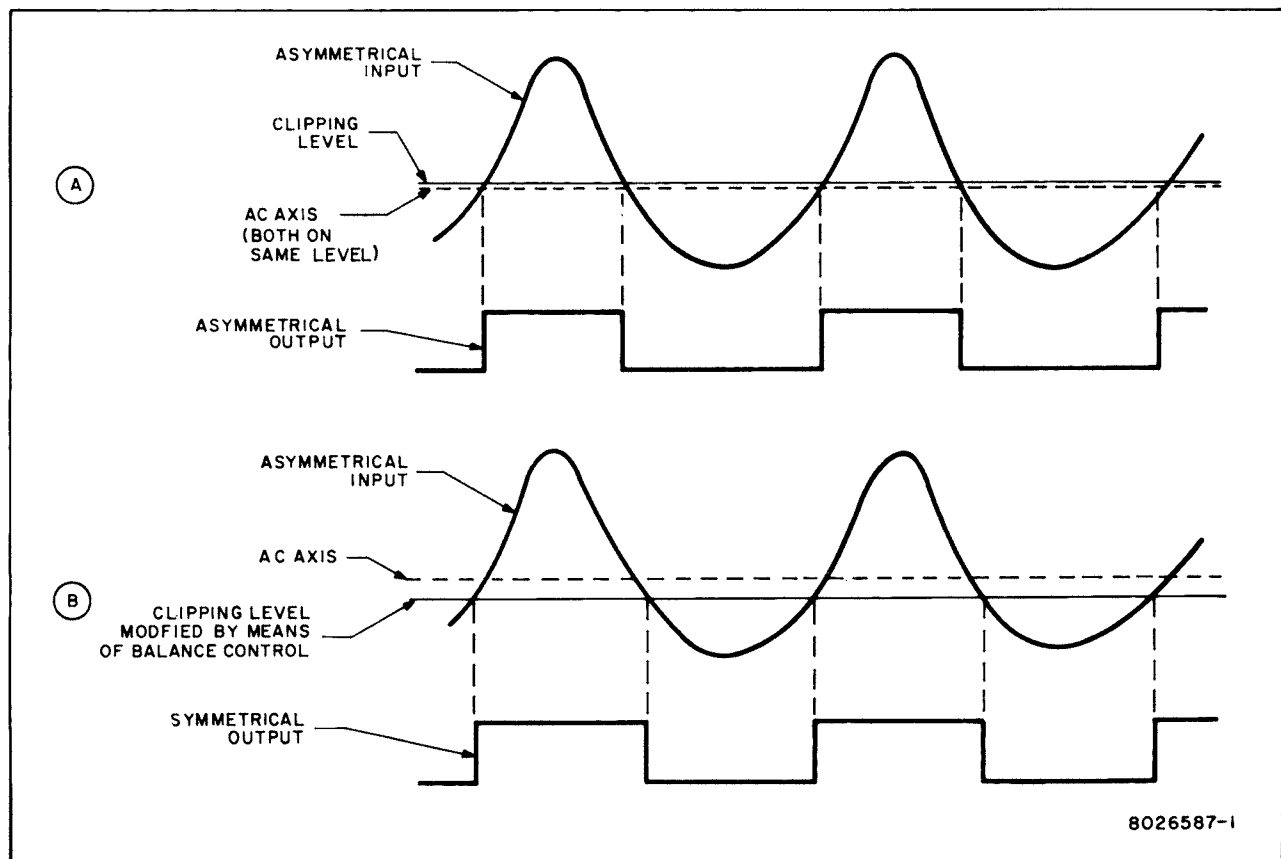


Figure 78—Balance Control Operation

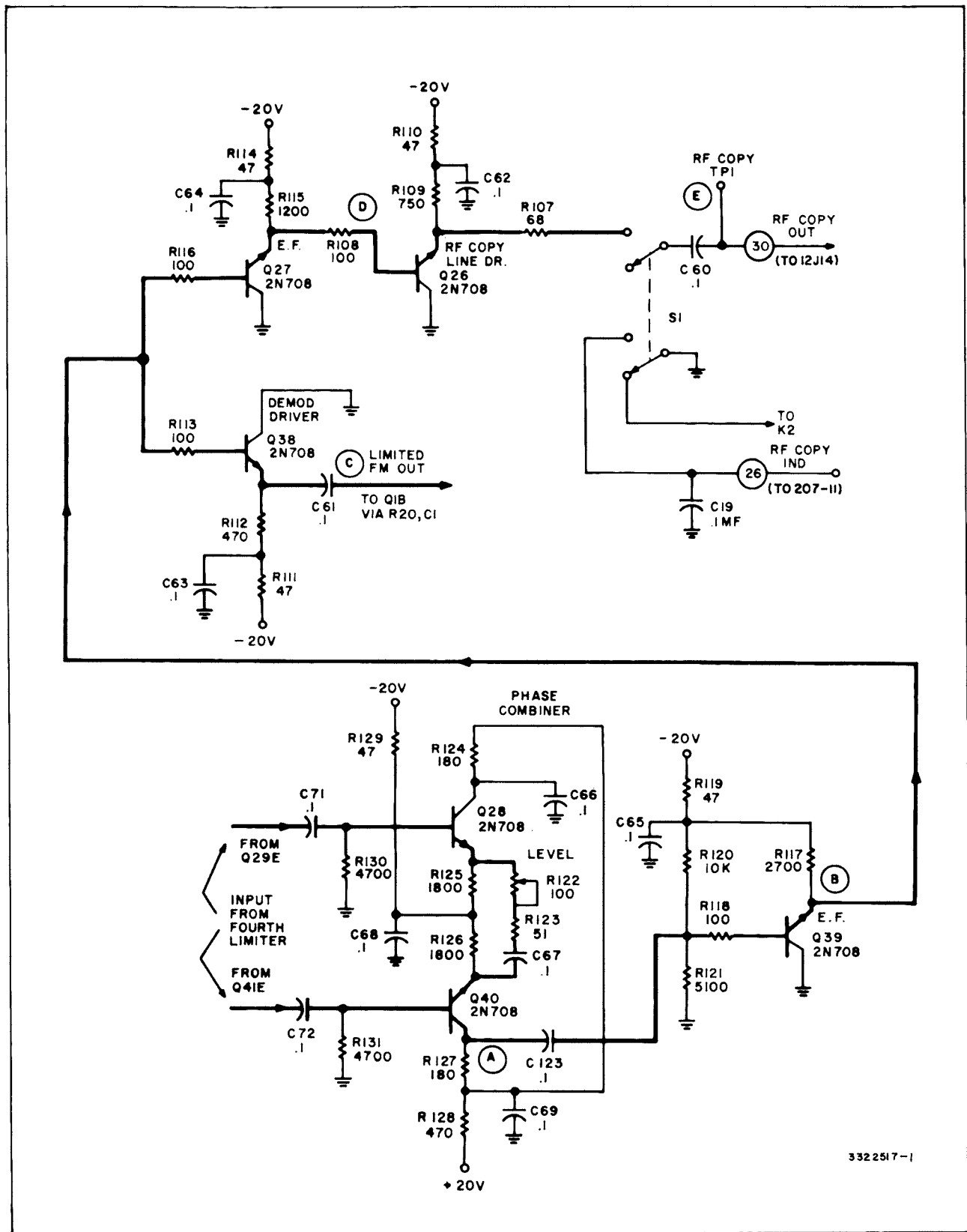


Figure 79—Phase Combiner, R-F Copy and Demodulator Driver Circuits

spective video amplifier. The amplified output is then coupled by an emitter follower to the video line driver, which feeds the line to the Demodulator Output (module 303A).

CIRCUIT

Phase Splitters

The FM signal (figure 81) from the Limiter is terminated in 75 ohms by R1 and coupled through R20 and C1 to the base of Q1, an emitter follower. Two outputs are taken off the emitter of Q1. One is coupled through C5 to the base of Q3, which together with Q4 forms a phase splitter pair. The other output signal is first passed through delay circuitry before being applied to a similar pair of phase splitters, Q12, Q13. The delay is needed in order to obtain properly phased gating signals with which to drive the diode discriminator. (This will be demonstrated later.)

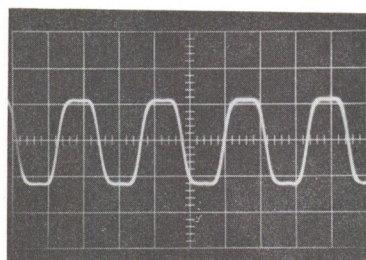
The signal entering the delay branch from the emitter of Q1 is fed through R15 to base of Q2, the delay line driver, an emitter follower. From the emitter of Q2, the signal is coupled through C4 and R8, where it enters the delay cable. The latter is of such length and characteristics as to provide a delay of approximately .03 microsecond. The output of the delay cable

is applied to the emitter of Q10, a common base amplifier.

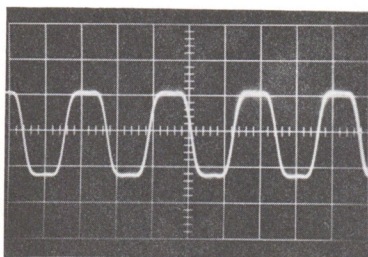
Both ends of the delay line are terminated in 75 ohms. At the receiving end, 75 ohms is obtained by the 68 ohms of R8 in combination with the emitter impedance of Q2. And, similarly, at the receiving end, the 68 ohms of R36 together with the emitter impedance of Q10, appears as 75 ohms to the signal.

The loss in level incurred by the signal due to the terminations at the input and the output of the delay cable is recovered in Q10. The output signal on the collector of Q10, now restored to the same level as that appearing on the base of Q1, is coupled through C23 to the base of Q11, an emitter follower. From the emitter of Q11, the signal is coupled through C25 to the base of Q12, which, in combination with Q13, forms the other phase splitter pair. Other than the phase shift caused by the .03 microsecond relay, the signal appearing on the base of Q12 is the same as the undelayed signal appearing on the base of Q3.

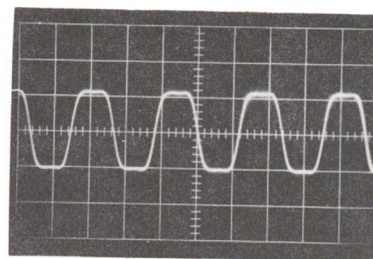
Since the phase splitter circuits in each branch are identical, only one, Q3 and Q4, will be discussed. The operation of Q3, Q4 is similar to that of a differential amplifier. Transistor Q3 is a common emitter amplifier and Q4 is a common base amplifier. The emitters



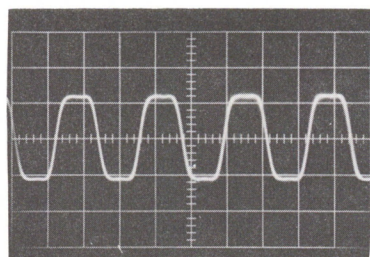
A. Q40 collector, .1 μ s/cm, 1v/cm



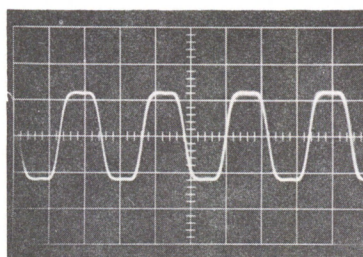
B. Q39 emitter, .1 μ s/cm, 1v/cm



C. Q38 emitter, .1 μ s/cm, 1v/cm



D. Q26 base, .1 μ s/cm, 1v/cm



E. TP1, .1 μ s/cm, 1/2 v/cm

Figure 80—Typical Waveforms; Phase Combiner, R-F Copy and Demodulator Driver Circuits

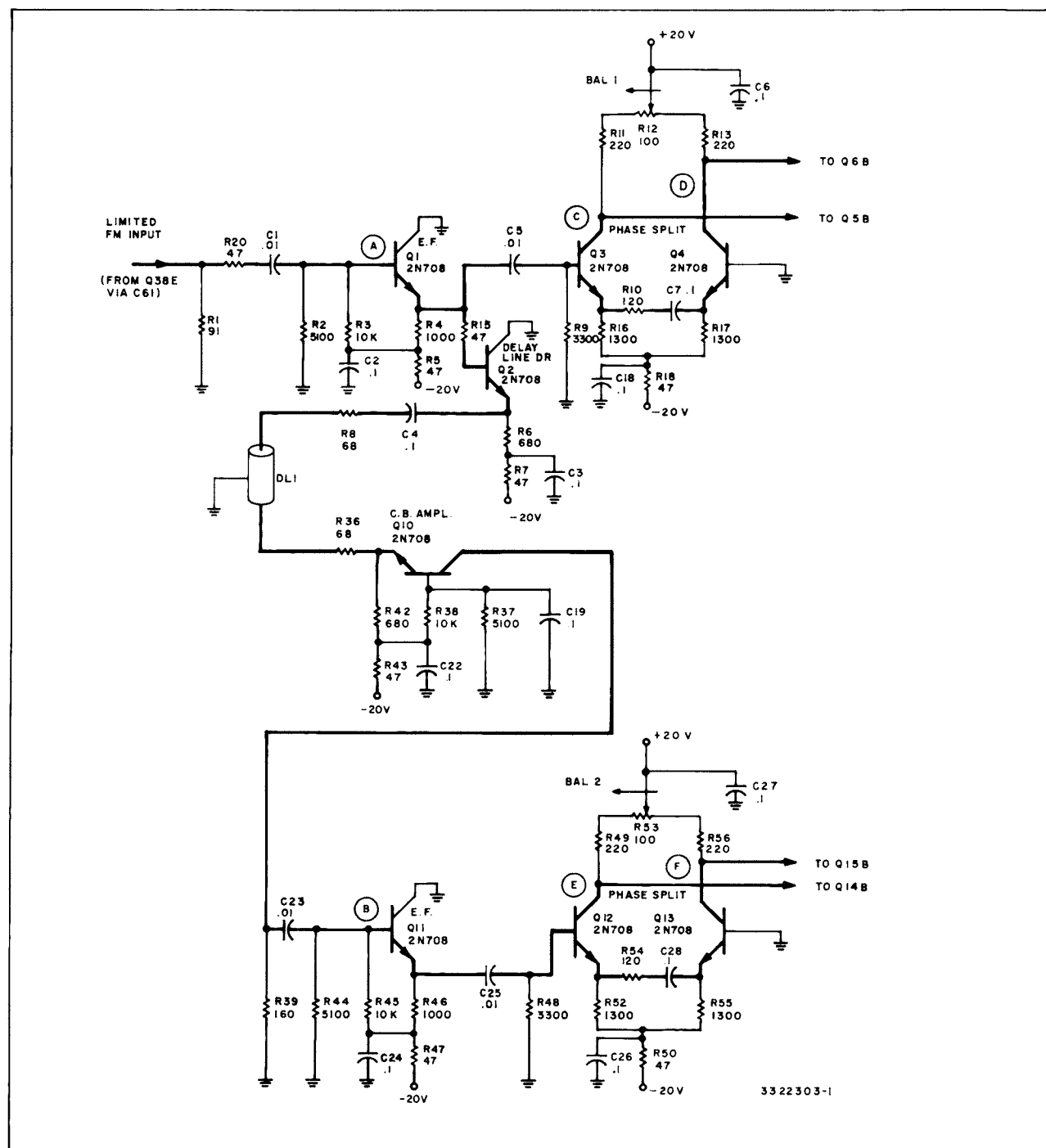


Figure 81—FM Input, Delay and Phase Splitter Circuits

of these two transistors are ac coupled through R10 and C7. With this arrangement, the bias conditions between the two transistors are such that one conducts when the signal is positive and the other conducts when the signal is negative. A positive going signal on the base of Q3 forward biases this transistor causing it to conduct. At this time a replica of the same signal appears on the emitter of Q3, and hence is also present on the emitter of Q4 by virtue of the ac cou-

pling between these two elements. However, since this is a positive going signal, it reverse biases Q4, cutting off the latter. When the signal on the base of Q3 goes negative the opposite occurs. Transistor Q3 becomes reverse biased and is cut off. Therefore the signal representing reverse bias on the emitter of Q4 is no longer present and this transistor conducts. The resultant output available at the collectors of Q3 and Q4 is two signals 180° out of phase.

Connected in series between load resistors R11 and R13 in the collectors of Q3 and Q4, respectively, is a potentiometer, R12, designated BAL-1. Likewise in the collector circuits of Q12 and Q13 is a similar potentiometer, R53, designated BAL-2.

The purpose of these potentiometers is to change the relative load impedance on the collectors of the phase splitters to compensate for differences in the characteristics of the discriminator diodes. Access holes, appropriately labeled, are provided on the front panel of the module to enable either of these potentiometers to be adjusted by inserting a slender screwdriver to turn the trimmer control. However, the trimmers on the balance potentiometers are not operational controls, therefore they should not be readjusted in the course of normal operation or routine maintenance.

Diode Discriminator

The complementary outputs of the phase splitters in both branches are fed to individual emitter followers which drive the diode discriminator (see figure 83). The output signals on the collectors of Q3 and Q4 are fed to the bases of Q5 and Q6, through R21 and R40, respectively. The delayed output signals on the collectors of Q12 and Q13 are fed to the bases of Q14 and Q15, respectively.

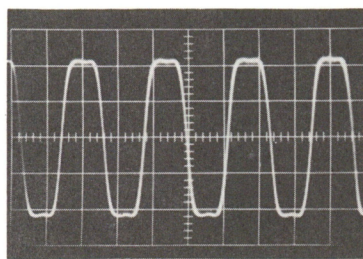
The outputs from the emitter followers are connected to the discriminator network in such a manner that a delayed and an undelayed signal are combined

in pairs to form a gating signal at the junction of the two resistors at the input to each diode. The output of the discriminator is a series of fixed-width positive pulses, the frequency of which is twice that of the gating signals.

A graphical analysis of the operation of the diode discriminator network is shown in figure 85. This illustration shows the phase and polarity of the gating signals applied to the diodes, over several cycles of carrier during deviation typical of a frequency modulated signal. The fixed-width positive output pulses are shown below the input pulses. The chart beneath the discriminator output waveform shows the order in which the diodes conduct.

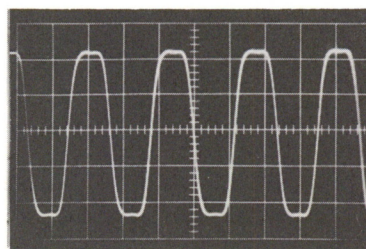
Assuming the frequency of the discriminator input signals to be as shown in figure 85, and considering time interval t_1 to t_2 with all four signals applied across the discriminator, the diodes will conduct in the following manner.

The positive signal from Q6 and the delayed negative signal from Q15 combine at the junction of R63, R66 as the gating signal to CR1. Because these two signals are of opposite polarity, the resultant potential at CR1 is zero, tending to prevent conduction. At the same time, the positive signal from Q6 is also joined with the delayed positive signal from Q14 to form the gating input to CR2 at the junction of R67, R68. Since the polarity of the resultant gating signal is positive, CR2 conducts and a positive pulse appears at the output of the discriminator during interval



.1 μ s/cm, 0.5v/cm

KEY	LOCATION
A.	Q1 base
B.	Q11 base



.1 μ s/cm, 1v/cm

KEY	LOCATION
C.	Q3 collector
D.	Q4 collector
E.	Q12 collector
F.	Q13 collector

Figure 82—Typical Waveforms; FM Input, Delay and Phase Splitter Circuits

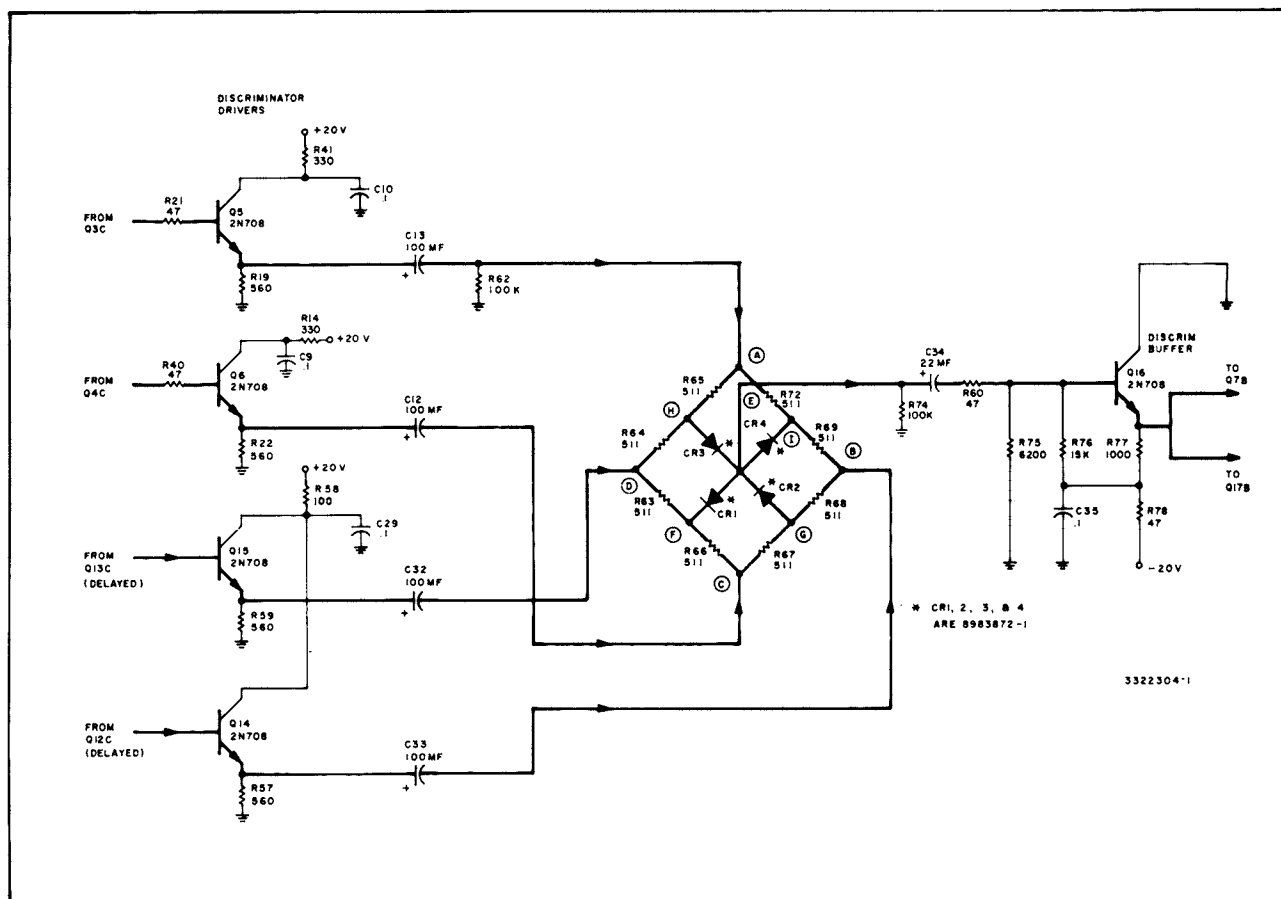


Figure 83—Discriminator Drivers, Diode Discriminators and Buffer Circuits

t_1 - t_2 . The gating input to CR3 is formed at the junction of R64, R65 by the negative signal from Q5 and the delayed negative signal from Q15. Since the resultant of these combined signals is also negative, the effect is to turn off CR3. The negative signal from Q5 and delayed positive signal from Q14 combine at the junction of R69, R72 as the gating input to CR4. However, the resultant of these two signals is zero, thus preventing CR4 from conducting.

While CR1 and CR4 do not pass their gate signals since the resultant is zero or ground potential at the junction of the input resistors and the cathodes of these diodes, they are in a quiescent state. This is due to the positive output voltage, which is present at the junction of all four diodes. Therefore this loads the output with the resistors to which the cathodes of CR1 and CR4 are connected.

From time t_2 to t_3 a similar gating action takes place, with the polarity of the undelayed signals from Q5 and Q6 remaining the same, but with the polarity of the delayed signals from Q14 and Q15 now reversed. During this interval CR1 is cut off; CR2 and CR3 tend to be cut off; but CR4 conducts, transfer-

ring its negative gate signal to the output.

The discriminator diodes continue to conduct in this fashion throughout the remaining intervals as the gating signal to each diode assumes the proper polarity.

As can be seen from the lightly shaded areas on the input pulses, positive gating signals occur twice during one alternation of each input cycle, thus the frequency of the discriminator output pulses is twice that of the input wave. Note, also, that as the frequency of the output pulses increases, the interval between becomes shorter. However, because the pulse width remains constant, due to the previously established .03 microsecond delay between the input signals, the average output level becomes more positive (greater number of positive pulses per unit of time) as frequency increases.

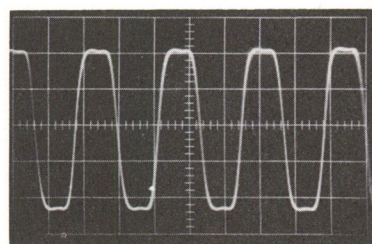
The pulse output of the discriminator is coupled through C34 and R60 to the base of Q16, an emitter follower which serves as a buffer between the discriminator and the following filter circuits. From the emitter of Q16, the signal is fed to the base of either of two filter drivers, Q7 or Q17.

Filtering and Video Recovery

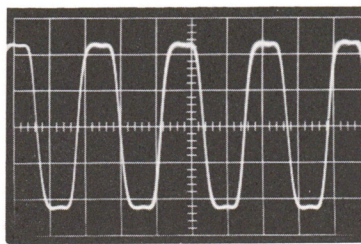
The discriminator output signal contains both unwanted high frequency components of the carrier and the desired video information, as related to the average duty cycle. In order to recover the frequency component representing the original video, this signal must be filtered (see figure 86). Furthermore, two separate filter circuits are necessary to accommodate the bandwidth requirements of the different line rates on domestic and international standards. Only one filter circuit is active, and this is determined by the line rate on which the TR-22 is being operated. If the TR-22 is used on 405 or domestic 525-line operation,

a 4.2 mc filter plugged into J1 in the channel no. 1 filter circuit, is used. When used on other international standards, the Demodulator uses the filter in J2. The channel no. 2 filter circuit is 5.0 mc and is employed for 625-line operation, or 819. Selection of the appropriate filter for either 405/525 or 625-line rates is done by means of the VI SP and VN SP busses. (Just how this is accomplished will be described later.)

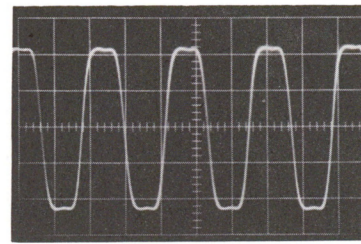
The output from the emitter of either filter driver (Q7 or Q17) is applied to the appropriate filter, which is terminated at both ends in 91 ohms. The filter is designed to eliminate all frequencies above



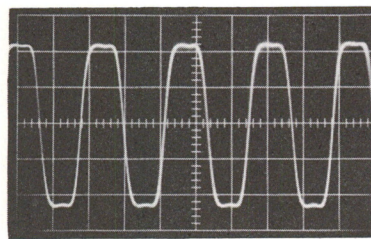
A. Junc. R65, R72, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



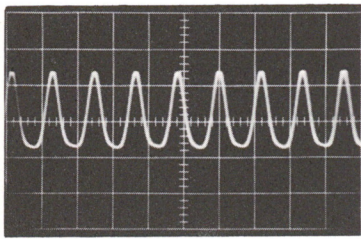
B. Junc. R69, R68, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



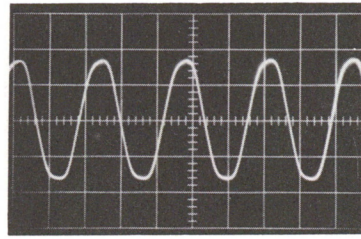
C. Junc. R66, R67, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



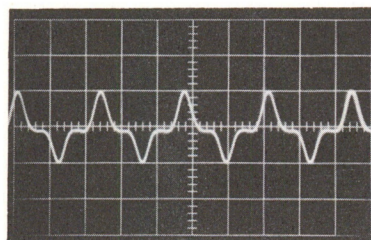
D. Junc. R64, R63, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



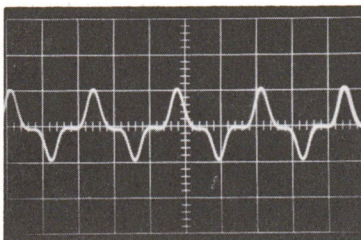
E. Junc. CR1, CR2, CR3, CR4, $.1 \mu\text{s}/\text{cm}$, $.5\text{v}/\text{cm}$



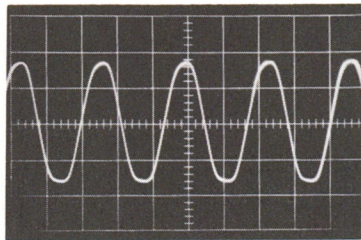
F. CR1 cathode, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



G. CR2 anode, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



H. CR3 anode, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$



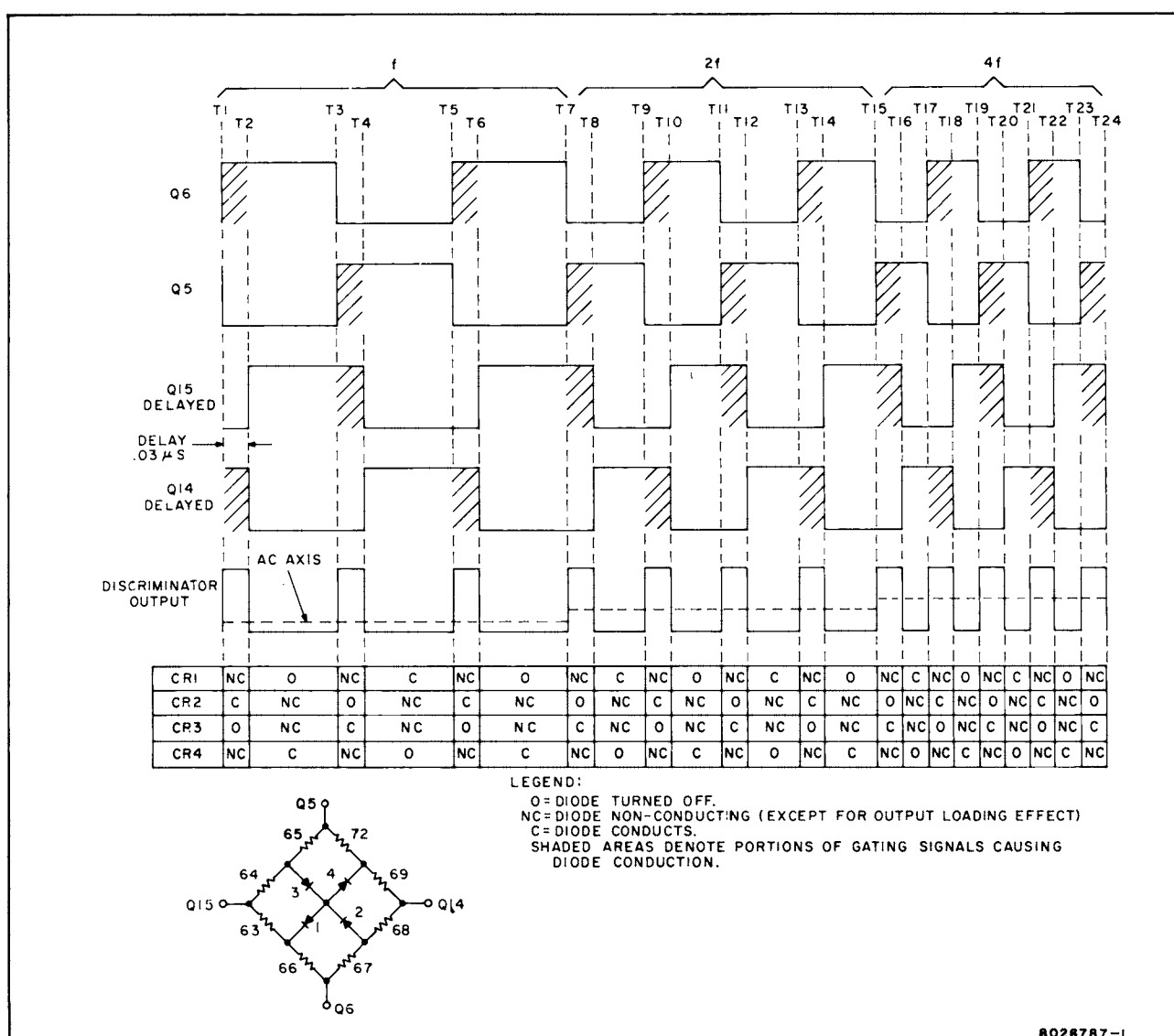
I. CR4 cathode, $.1 \mu\text{s}/\text{cm}$, $1\text{v}/\text{cm}$

Figure 84—Typical Waveforms, Discriminator Drivers, Diode Discriminator and Buffer Circuits

the video band, and deliver at the output a varying average dc whose amplitude changes are a function of the video frequency modulated input. The result of this is an output signal that is a replica of the video signal initially applied to the recorder. As mentioned earlier, the discriminator output frequency is twice that of the input. The purpose of frequency doubling is to facilitate the separation of the video and the carrier components in the filter, since with some standards the spectra of the two signals overlap. In other words, the carrier frequency, which represents the sync and blanking region, may extend down into the filter bandpass, overlapping the video component. By using the technique of frequency doubling prior to filtering, such a condition is prevented. Asymmetry, whether present in the FM signal from the

Limiter or caused by unbalance in the discriminator diodes, will introduce an unwanted component of the carrier fundamental frequency into the filter. In addition to the desired double carrier frequency, this unwanted component may be within the bandpass range of the filter and, therefore, fail to be eliminated from the video output of the filter.

The filtered signal is fed to the emitter of one of two common base video amplifiers (Q18 or Q19) where the signal is amplified to a level suitable for driving the succeeding video output stage. Shunt high frequency compensation is provided by coil L1 and variable capacitor C39 in the collector circuit of the output common base amplifier. Use of a variable capacitor in the high frequency compensation network



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Figure 85—Diode Discriminator Conduction Cycle

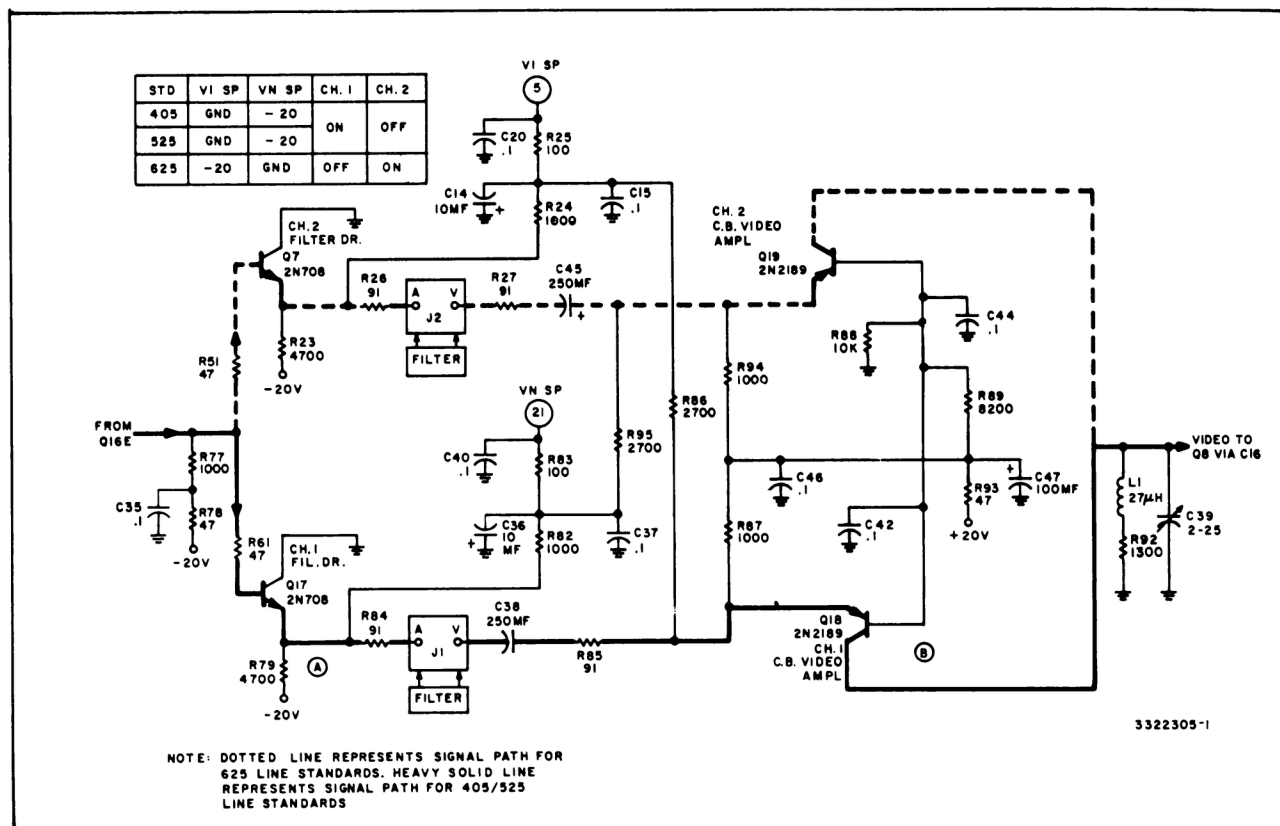


Figure 86—Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits

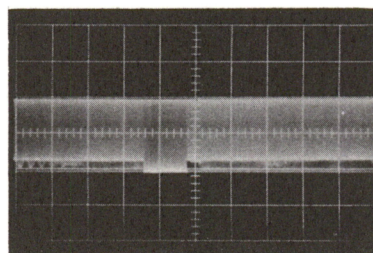
enables the pass band at the high end to be adjusted for a flat response.

International Standards Filter Selection

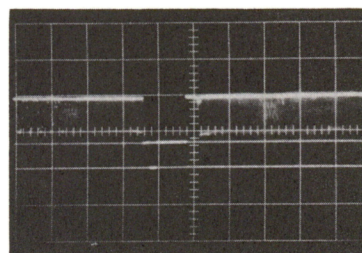
As mentioned previously, switching between the two filter circuits for operation on international standards is controlled by the VI SP and VN SP busses. The desired line rate is selected by means of the TV STANDARDS switch, which is located on the front

panel of the Vertical Advance (module 228A).

When the 625-line rate is chosen, the 5.0 mc filter (channel 2) circuit is placed in operation. The -20 volts on the VI SP bus biases Q7, the channel no. 2 filter driver, so that it will conduct, while simultaneously cutting off Q18, the channel no. 1 video amplifier. The VN SP bus, which is at ground potential, cuts off Q17, the channel no. 1 filter driver, but allows Q19, the channel no. 2 video amplifier, to



A. Q17 emitter, 1 ms/cm, .5v/cm



B. Q18 collector, 1 ms/cm, .5v/cm

Figure 87—Typical Waveforms, Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits

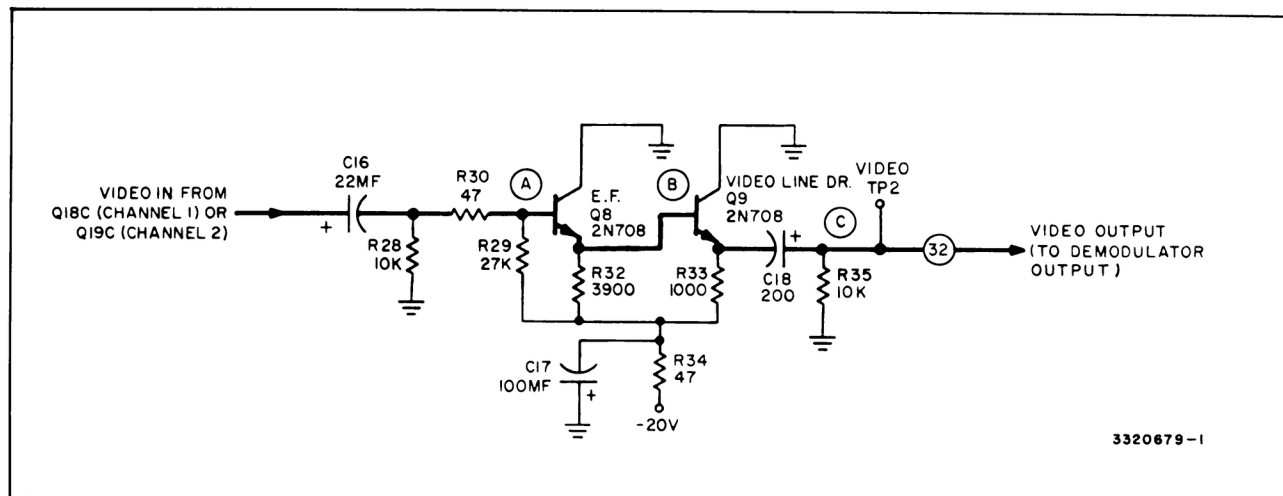
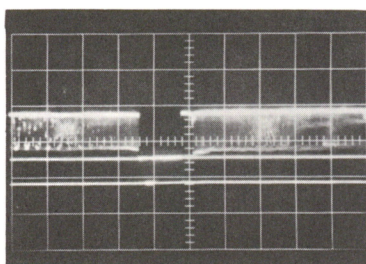
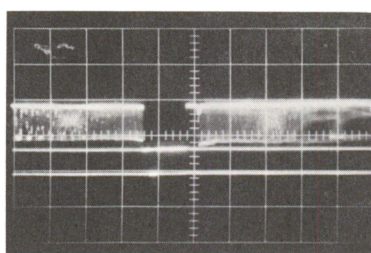


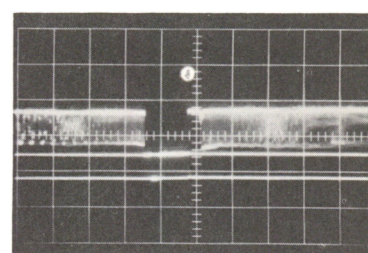
Figure 88—Emitter-Follower and Video Line Driver Circuits



A. Q8 base, 1 ms/cm, .5v/cm



B. Q9 base, 1 ms/cm, .5v/cm



C. TP1, 1 ms/cm, .5v/cm

Figure 89—Typical Waveforms, Emitter-Follower, and Video Line Driver Circuits

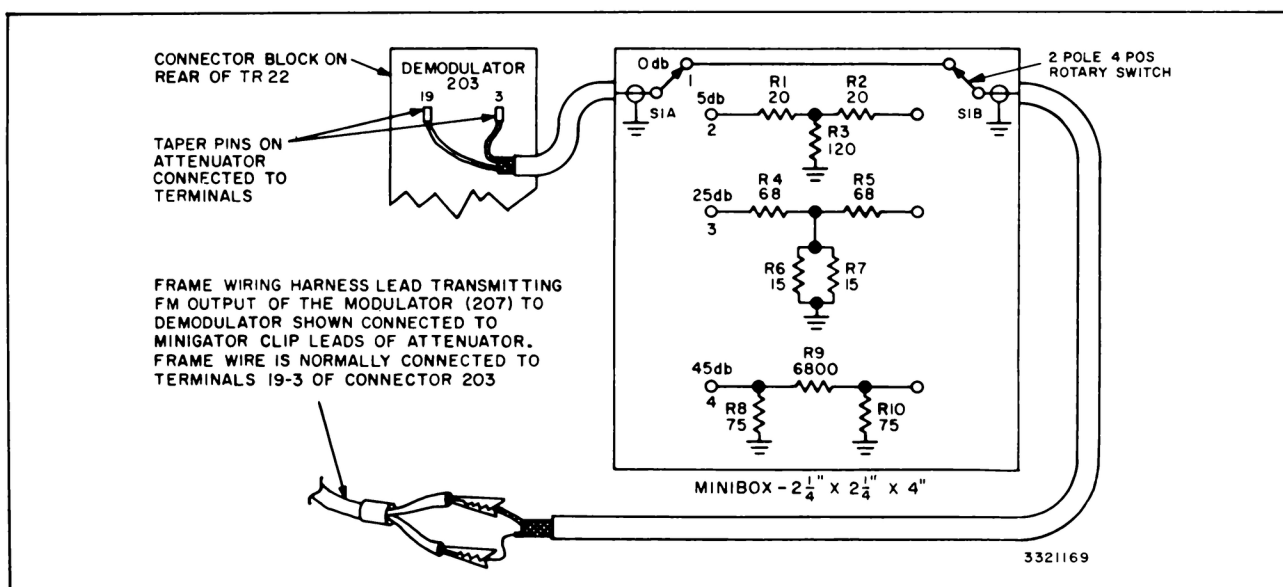


Figure 90—Schematic of Video Attenuator Showing Connection Details

conduct. Therefore the output of the diode discriminator will pass through the channel no. 2 filter circuit.

When either the 405- or 525-line rate is selected, the VI SP and VN SP potentials are reversed and the channel no. 1 filter network is in operation. In this case the VN bus is at -20 volts, allowing Q17 to conduct, while cutting off Q19. The VI SP bus is at ground potential and this permits Q18 to conduct, while preventing Q7 from conducting. Under these conditions, the output of the diode discriminator flows through the channel no. 1 filter circuit.

Video Output

The video output on the collector of either Q18 or Q19 is coupled through C16 to the base of Q8 (see figure 88). Transistors Q8 and Q9 form a dc coupled cascade emitter follower amplifier, which isolates the preceding stages from the video output line. From the emitter of Q9, the signal is coupled through C18 to drive the line to the Demodulator Output (module 303A).

ADJUSTMENTS

Balance Procedure

The demodulator discriminator circuit is balanced at the factory and the two balance potentiometers, R12 and R53 are ordinarily not disturbed during the life of the equipment. However, in the event that the balance should be upset due to the replacement of discriminator diodes or for some other reason, balance can be re-established by following the procedure outlined below.

In performing certain steps of the balance procedure, it will be necessary to attenuate the Demodulator (module 203B) input signal by 5, 25, and 45 db. This may be done by interposing a video attenuator in the coaxial line connecting the FM output of the Modulator (module 207B-S) to the Demodulator (module 203B). In lieu of a commercial attenuator, a network such as the one shown schematically in figure 90 can be used to provide the necessary attenuation. Figure 91 is an over-all view of the attenuator. In assembling the latter, use 75-ohm miniature coaxial cable for the signal leads. To install the attenuator, first remove the coaxial lead from terminals 19-3 of connector 203B on the rear of the machine. Connect the attenuator (see figure 90) between terminals 19-3 and the free end of the coaxial lead previously removed.

1. Apply a composite video signal to the input of

the TR-22; select MONO STD and place the TR-22 in the E-E mode of operation (MOD-DEMODO button on Play panel.)

2. Check the sync tip frequency and deviation; adjust if necessary. (Instructions covering these adjustments are given in the Operation Manual, IB-31197-1, under *Initial Setup*.)

3. Remove the (203B) Demodulator module and reinsert it in the machine using the test module extender.

4. Switch the CRO to DEMOD OUT and select the vertical interval for display.

5. Switch the attenuator to the 5 db position and adjust the first limiter balance control, R208, (on the front panel) for minimum RF unbalance of the signal at sync and blanking levels.

6. Change the attenuation to 25 db and adjust the second limiter balance control, R206, (internal top "trimpot") for minimum RF unbalance at sync and blanking levels.

7. Switch to 45 db of attenuation and adjust the third balance control, R205, (internal bottom "trimpot") for minimum unbalance as before.

8. Set the attenuator to 0 db attenuation and adjust level control, R122, to obtain a 2 volt peak to peak signal at the base of Q1.

NOTE

A small thin screwdriver is required to adjust DEMOD BAL No. 1 and No. 2 controls located behind the special guide bushings on the front panel of the module.

9. Adjust DEMOD BAL No. 1 and No. 2 for minimum unbalance at the blanking level.

10. If good balance is not attained repeat steps 5 through 9.

11. Remove the attenuator and restore the free ends of the coaxial lead to the original connections and reinsert module in its normal location.

Video Response Procedure

1. Mount the Demodulator in an extender and replace it in the machine.

2. Connect a multiburst signal to the video input of TR-22; select MONO STD and place the TR-22 in the E-E mode of operation.

3. Switch the CRO to DEMOD OUT and select the HOR interval for display.

4. Observe the CRO and adjust C39 for flattest response of the high end of the band.

5. Remove the extender and replace the Demodulator in the machine; disconnect the multiburst signal from the video input.

DEMODULATOR OUTPUT (Module 303A)

Module 303A is a double width module with two circuit boards. Board 1 contains the output amplifiers for the post-emphasized video signal from the FM Standards Module, 205A, and a sensor circuit which determines whether the quality of the tape video signal is good enough to permit automatic operation of the guide servo system and provides a control signal which switches the guide servo to manual operation when the quality is unacceptable. Board 2 contains a clamped sync separator which provides sync to the sensor circuit on board 1, module 317 in the head-wheel servo system, and module 225 of the monochrome ATC system.

MODULE 303A, BOARD 1

While reading the following circuit descriptions, refer to the block diagram, figure 92 and the simplified schematics.

VIDEO OUTPUT AMPLIFIER CIRCUITS

The video output amplifier section of the demodulator output module amplifies the post-emphasized video signal from the FM standards module and provides four video outputs. Two of these outputs have fixed levels and two have variable levels remotely controlled by the video LEVEL control, R15, on the Video Control module, 131B. The first fixed video output goes to the picture monitor, and the second, to the CRO waveform monitor. Similarly the first variable output goes to the video input of the monochrome ATC system, which is the Fixed Delay Line, FDL1. The second variable output goes to a bypass relay, 11K11A on the ATC relay bank. When the monochrome ATC system is in the bypass condition, this relay feeds the video signal directly to the input of the Video Output module, 131B, and to the clamped sync separator on Board 2 of the ATC Reference Module, 226B.

The circuit of the video output section (see figure 93), consists of an input emitter follower, Q5, which feeds two amplifier chains, one of which provides the two fixed video outputs, and the other, the two variable outputs. The fixed level amplifier consists of an

emitter follower, Q6, followed by a series line driver, Q7, Q8. The variable level section consists of a lamp and photocell circuit, V1, DS1, DS2, a common base amplifier, Q4, an emitter follower Q3, and a series line driver, Q1, Q2. The emitter follower and line driver are identical to those in the fixed level section. The lamp and photocell arrangement, and the common base amplifier permit remote control of the video input level by a dc voltage obtained from the video LEVEL control, R15, on module 131B.

Input Emitter-Follower, Q5

The 2-volt post-emphasized video signal from the output of the FM standards module is fed through P1-17 and capacitor C6 to the base of the input emitter follower, Q5 (see figures 93 and 94). The output of this stage is fed through R46 to the base of emitter follower Q6 in the fixed video section, and through R1, to the photocell circuit in the input of the variable video section.

Fixed Video Section (Q6, Q7, Q8)

The output of emitter follower Q6 is fed to the base of one of the two transistors, Q7, in the series line driver. Signal from the collector of Q7 is applied through capacitor C7 to the base of Q8. A Zener diode CR2, provides a constant voltage difference of 12 volts between the collector of Q7 and the base of Q8. The output of the line driver is taken from the junction of the emitter of Q7 and the collector of Q8. Thus the circuit can be considered to be an emitter follower, Q7, with Q8 as dynamic emitter load, or a common emitter amplifier, Q8, with Q7 as a dynamic collector load.

The output of Q7 and Q8 is fed to three paths. One goes directly to capacitor C41 in the input of the clamped sync separator circuit on the same module. The other two go through individual resistors and capacitors (R19, C10; R20, C11) to the picture monitor and CRO respectively. The capacitors provide dc isolation, and the resistors provide the required 75 ohm termination to the coaxial lines. These two outputs may be observed at test points TP3 and TP4 (see B, figure 94).

Variable Video Section (V1, DS1, DS2, Q4, Q3, Q2, Q1)

The video output of emitter follower Q5 is fed to the first stage in the variable video section, Q4, through a voltage divider. One element of this divider is a photocell, V1. The photocell acts as a variable re-

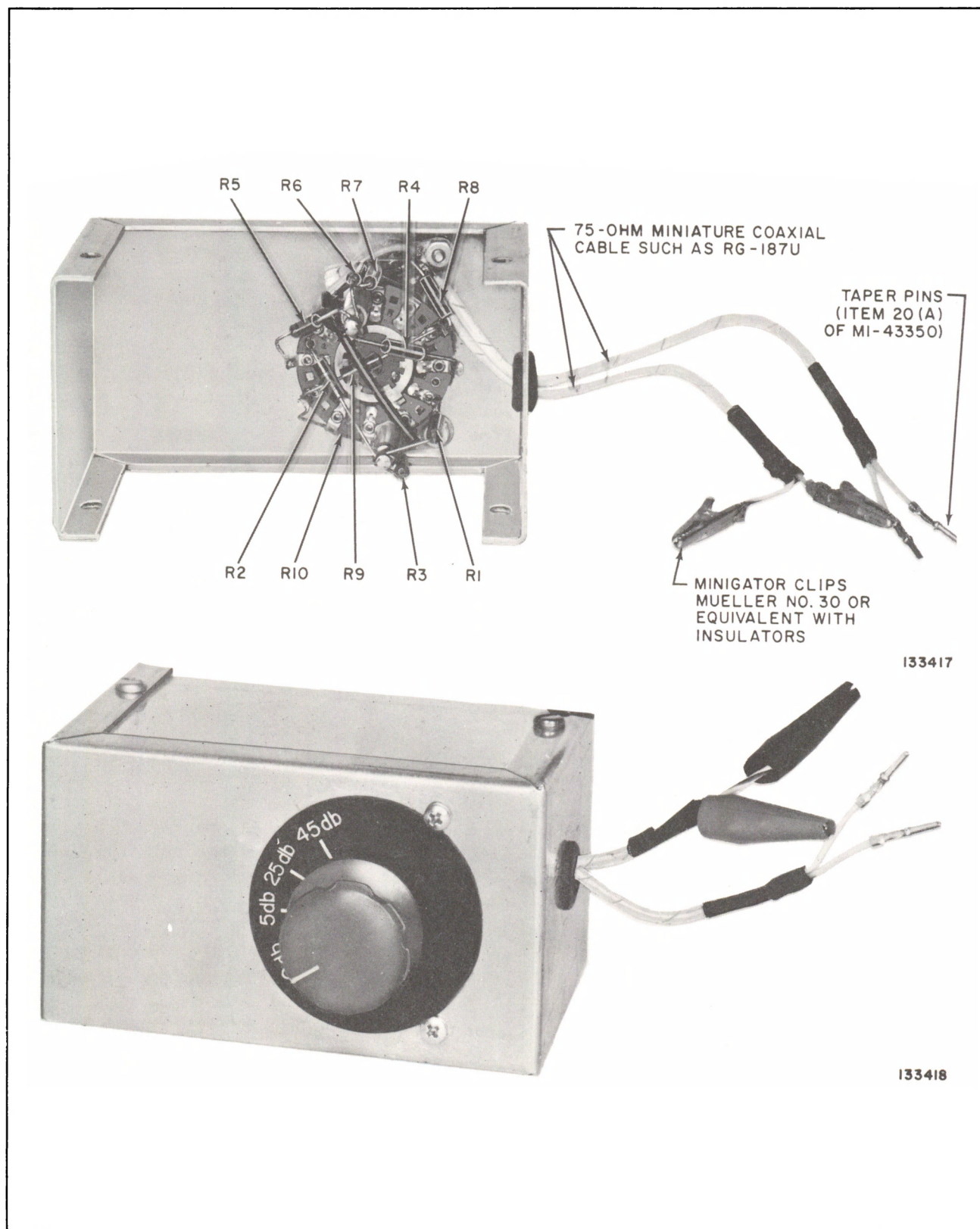


Figure 91—Over-all View of Video Attenuator

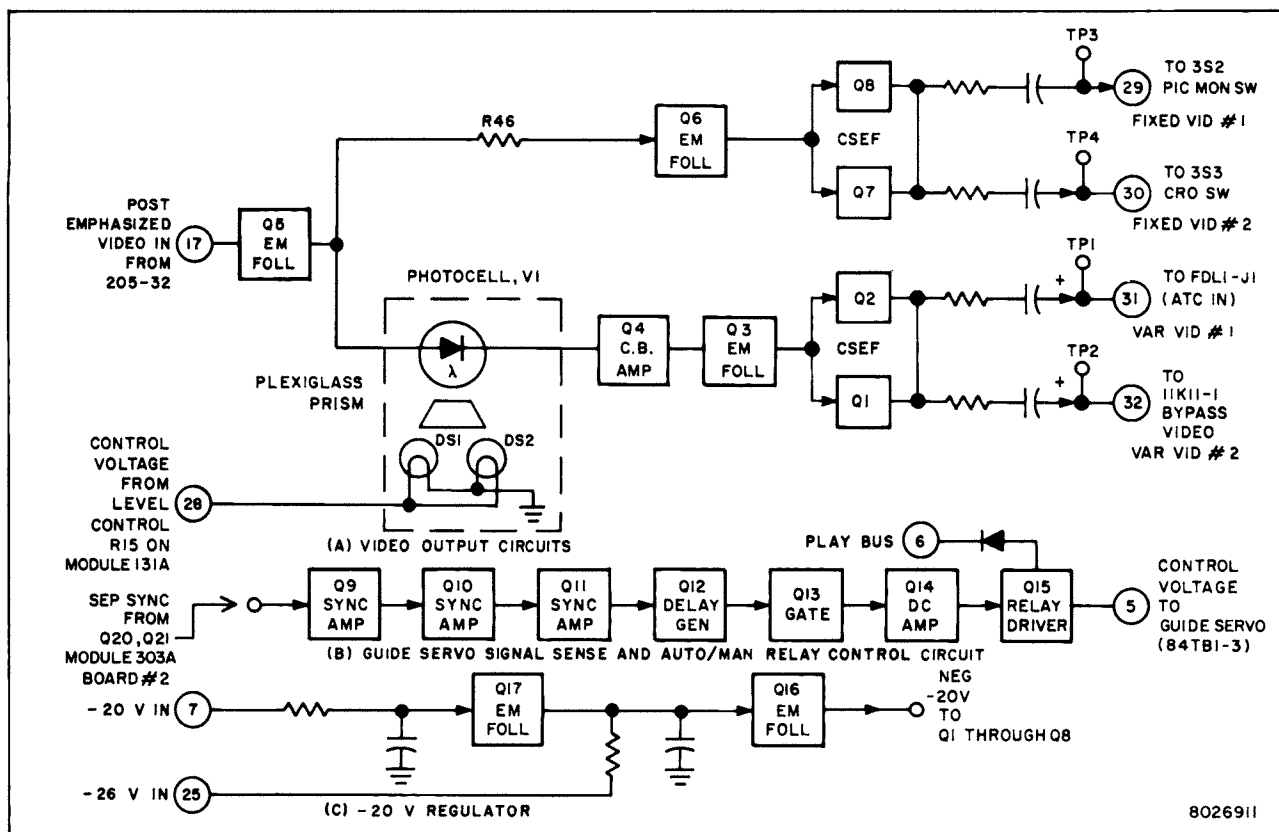


Figure 92—Block Diagram, Board 1 of Demodulator Output Module

sistor controlled by the light from two lamps, DS1, and DS2, which is transmitted through a plexiglass prism. The filament current of the lamps, and consequently the light output is determined by a dc voltage fed from the circuit of the video LEVEL control, R15, on module 131B. Q4 is a common base amplifier which provides the low impedance required by the photocell, and acts as a voltage amplifier. The output of Q4 is fed to a circuit consisting of emitter follower Q3, and series line driver Q1 and Q2, which is identical to the fixed video section. Two outputs are obtained from this section, one of which goes through P1-31 to the fixed delay line, FDL1, which constitutes the video input of the monochrome ATC system, and the other which goes through P1-32 to the bypass relay, 11K11A. The two outputs may be observed at test points TP1 and TP2 (see figure 94).

SIGNAL SENSE CIRCUIT FOR GUIDE SERVO CONTROL

The module contains a circuit which senses the quality of the video signal and prevents the guide servo from entering the automatic mode if sync is absent or the signal is too noisy. The circuit consists of a signal sense circuit, Q9, Q10, Q11, Q12, Q13, a dc amplifier, Q14, and a relay driver, Q15.

The signal sense circuit is shown in figure 95. The circuit consists of a three stage sync amplifier, Q9, Q10, Q11, a delay generator, Q12, and a gate, Q13. The purpose of the circuit is to provide a negative dc voltage at the junction of two 10K resistors, R36, R38, if sync is not present in the video output of the module or if the signal is noisy. This negative voltage controls the dc amplifier and relay driver so that the guide servo cannot enter the automatic condition even if the GUIDE SERVO switch on the control panel is on AUTOMATIC, and the recorder is in the PLAY mode.

The first and third sync amplifiers, Q9, and Q11, are saturating type amplifiers, and the second, Q10 is an emitter follower. The delay generator Q12, and the gate, Q13, respectively, are pulse delay, and pulse narrowing circuits.

The output of the gate is fed to Q14, the dc amplifier. This transistor, in turn, controls Q15, the relay driver, turning it off or on. The output of the latter goes to the guide control relays, and is of such potential that with sync present the guide control will be in the automatic condition, and without sync the guide control will switch to the manual condition.

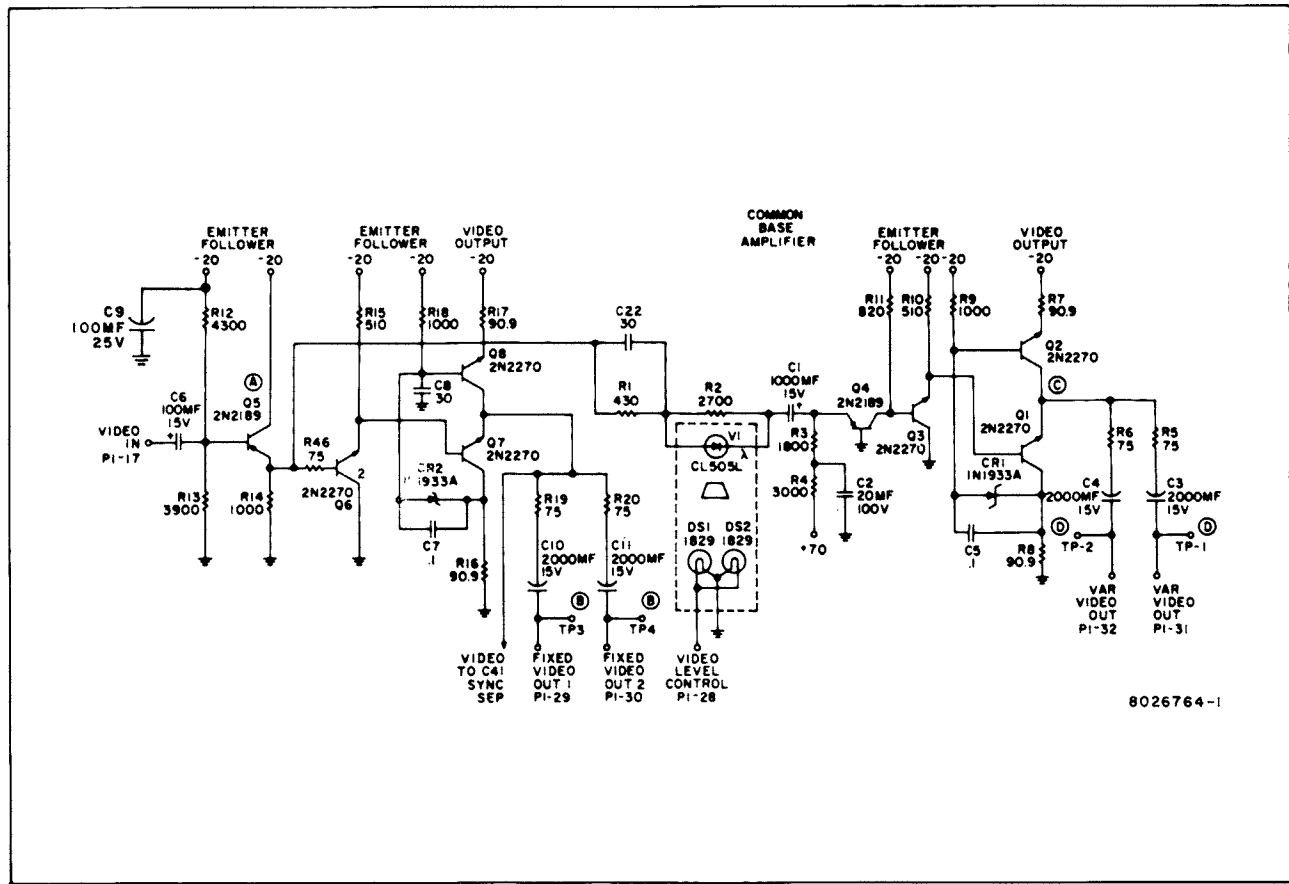


Figure 93—Video Output Circuits, Board 1

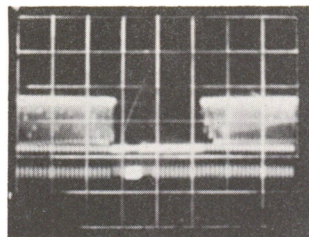
When a signal containing sync is fed through the Demodulator Output module, sync on the order of 4 volts peak-to-peak is coupled through C12 and R22 to the base of Q9. (See A, figure 96.) Amplified and inverted sync at the collector of Q9 (see B, figure 96) is applied to the base of Q10. The output from the emitter of Q10 is fed to the base of Q11 which provides an output signal of approximately 20 volts peak-to-peak (see C, figure 96).

During the sync pulse interval, time t_1 - t_2 (see A, figure 97) the positive potential at the base of Q11 saturates this transistor, causing its collector to go to -20 volts. When the sync pulse interval ends (t_2), the collector of Q11 goes from -20 volts towards ground and the resulting positive transition is coupled to the base of Q12, cutting off the latter (see B, figure 97). Transistor Q12 remains cut off until C15, charging through R29, develops sufficient negative potential to turn it on again (t_3). Transistor Q12 will continue to conduct until the next positive transition occurs on the collector of Q11 (t_6). The effect of this is to produce a negative pulse (see C, figure 97) at the collector of Q12 during t_2 - t_3 , which is delayed with respect to incoming sync by the width of a horizontal sync pulse.

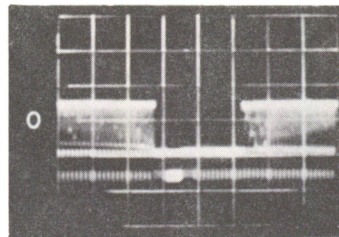
During the negative going pulse period of Q12, (t_2 - t_3) capacitor C17 charges through the base-emitter diode of Q13, R31 and R30, to -20 volts. Similarly, C16 charges through diode CR3, R31 and R30, to -20 volts. At the trailing edge of the pulse (t_3) a positive 20 volt pulse goes through C17 which cuts off the base-to-emitter diode of Q13. This pulse also cuts off diode CR3.

Under these conditions the end of R33 connected to C16 is at -20 volts because of the charge on C16, and the other end of R33, which is connected to the base of Q13 is at +20 volts because of the charge on C17. The charge on C17, however, leaks off rapidly, and when the base of Q13 goes slightly below ground, the base-to-emitter diode of Q13 conducts, because of the negative charge still remaining on C16. The resulting waveform on the base of Q13 (see D, figure 97) is a positive triangular pulse starting at the trailing edge of the delayed pulse from Q12 (t_3). The width of this pulse (t_3 - t_4) is determined by the time constant in the base circuit of Q13. During the pulse the base-to-emitter diode of Q13 is cut off, and between the pulses the base-to-emitter diode conducts.

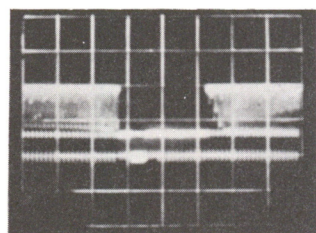
The collector of Q13 is not connected directly to



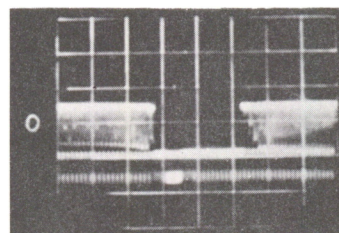
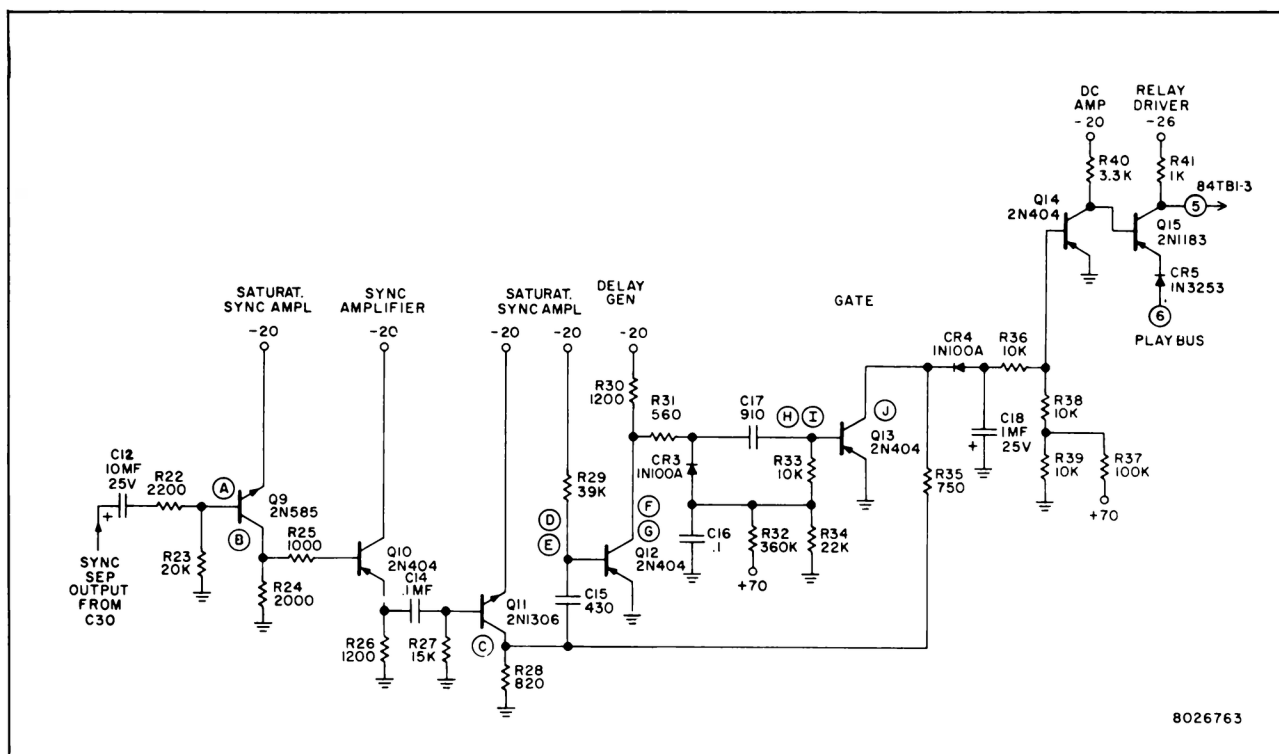
A. Q5 base, 0.5 ms/cm, 1v/cm.

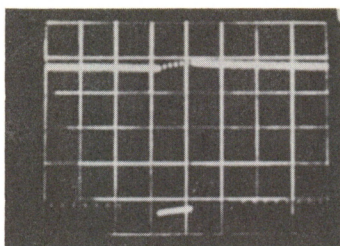


B. TP3, TP4, 0.5 ms/cm, 0.5v/cm.

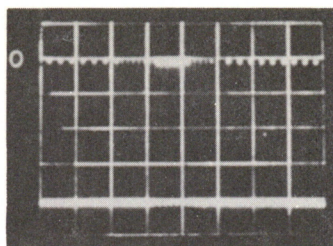


C. Q1 emitter, 0.5 ms/cm, 1v/cm.

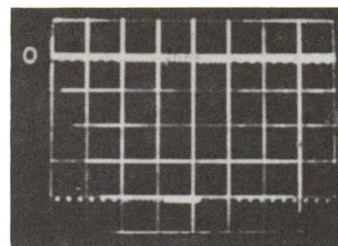
D. TP1, TP2, 0.5 ms/cm, 0.5v/cm
(ATC bypassed).**Figure 94—Typical Waveforms, Video Output Circuits****Figure 95—Signal Sense Circuit, Board 1**



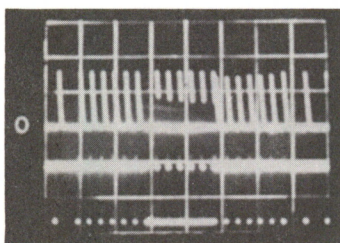
A. Q9 base, 0.2 ms/cm, 0.2v/cm.



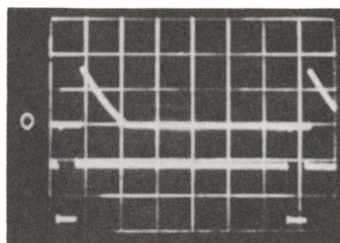
B. Q9 collector, 0.2 ms/cm, 5v/cm.



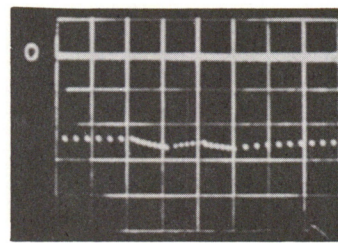
C. Q11 collector, 0.2 ms/cm, 5v/cm.



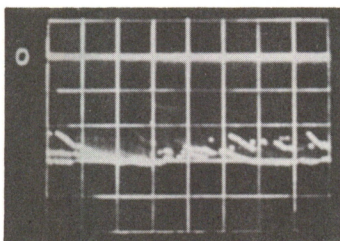
D. Top: Q12 base, 10v/cm,
Bottom: Sync. in (C12) 2v/cm.
(Sweep times 0.1 ms/cm)



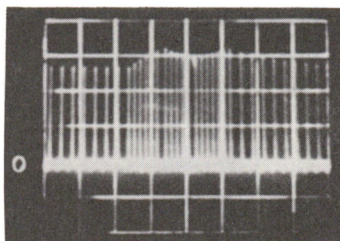
E. Top: Q12 base, 10v/cm,
Bottom: Sync. in (C12) 2v/cm.
(Sweep times 10 μ s/cm)



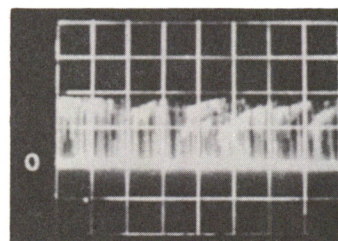
F. Q12 collector, 0.2 ms/cm, 5v/cm.



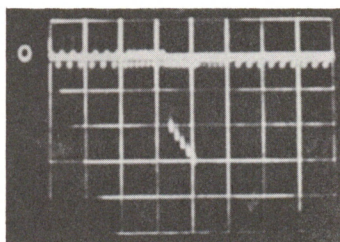
G. Q12 collector (Noise),
0.2 ms/cm, 5v/cm.



H. Q13 base, 0.2 ms/cm, 2v/cm.



I. Q13 base (Noise),
0.2 ms/cm, 5v/cm.



J. Q13 collector, 0.2 ms/cm,
0.5v/cm.

Figure 96—Typical Waveforms, Signal Sense Circuit, Board 1

a negative supply voltage, but instead, is connected through R35 to the collector of the third sync amplifier Q11. Because of this connection, the emitter-to-collector circuit of Q13 can conduct only during the sync pulse, when Q11 also conducts (t_1 - t_2). During the sync pulse Q13 saturates, and its collector goes to ground. Between sync pulses Q13 is cut off, but since the collector of Q11 is at ground, the collector of Q13 is also at ground at all times, regardless of the signal on its base (see E, figure 97).

With the collector of Q13 at ground, the dc amplifier Q14 is cut off. Current from the -20 volt bus then causes Q15 to saturate so that its collector essentially goes to ground when its emitter is connected through CR5 to the grounded play bus. Transistor Q15 is in series with the AUTO/MANUAL guide control relays, K1 and K2, so that when the collector of Q15 is at ground the relays will be activated and switch to automatic operation, provided this mode has been previously selected by means of the AUTO/MANUAL switch.

When there is no sync signal present, the final amplifier, Q11, is saturated continuously and its collector is at -20 volts. The gate, Q13, is cut off by the positive bias on its base which is developed across R32 and R33 from +70 volts. The -20 volts on the collector of Q11 therefore also appears on the collector of Q13. The -20 volts on the collector of Q13 is coupled through CR4 to the base of Q14, the dc amplifier. This voltage is sufficiently negative to overcome the positive bias (developed across R38, R39) on the base of Q14, driving this transistor into saturation and grounding its collector. Since the collector of Q14 is directly coupled to the base of Q15, the relay driver, the base of the latter is also at ground potential. With the base of Q15 grounded, this transistor is cut off and the guide servo relays are de-energized, causing the guide servo to switch to MANUAL operation regardless of the selection made with the AUTO/MANUAL switch.

When excessive noise occurs between the sync pulses, the collector of Q11 goes to -20 at intervals during noise, instead of remaining at ground as it normally would during the period between sync pulses. Because transistor Q13 is cut off during the gate interval, (t_3 - t_4) its collector will follow the negative excursions on the collector of Q11 (see F, figure 97). The negative fluctuations which appear on the collector of Q13 are coupled through CR4, charging C18. The negative voltage stored on C18 will cause Q14 to saturate, cutting off Q15. Thus K1 and K2 are prevented from becoming energized.

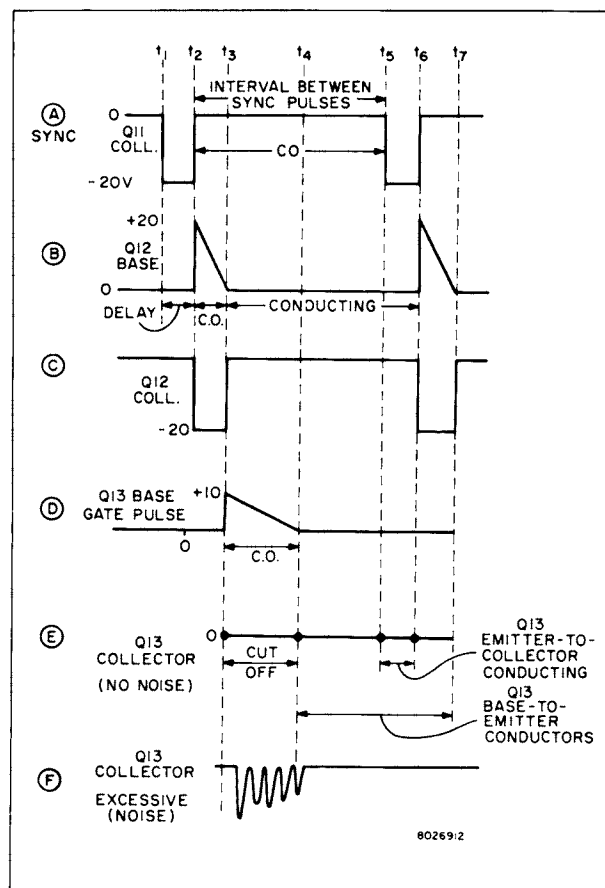


Figure 97—Timing Relations, Signal Sense Circuit

MODULE 303A, BOARD 2, FUNCTIONAL DESCRIPTION

The clamped sync separator on board number 2 of module 303A (see block diagram, figure 98) is specially designed to extract sync from the video signal without introducing any timing errors. This is accomplished by insuring that clipping occurs at exactly one-half the level of the sync pulse regardless of the video input level, switching spikes, dropouts, or noise. The circuit includes a level sensor, a switching pulse suppressor, a noise immunity multivibrator and a back porch clamp.

Video Amplifiers and Half-Level Clipper

As shown in the block diagram, figure 98, video from drivers Q7 and Q8 is fed to an emitter follower, Q35, which provides isolation. The output of Q35 is fed through a low pass filter which removes high frequency video and noise, amplified by two stages, Q34 and Q33, and then fed to a CSEF, Q31, Q32. The out-

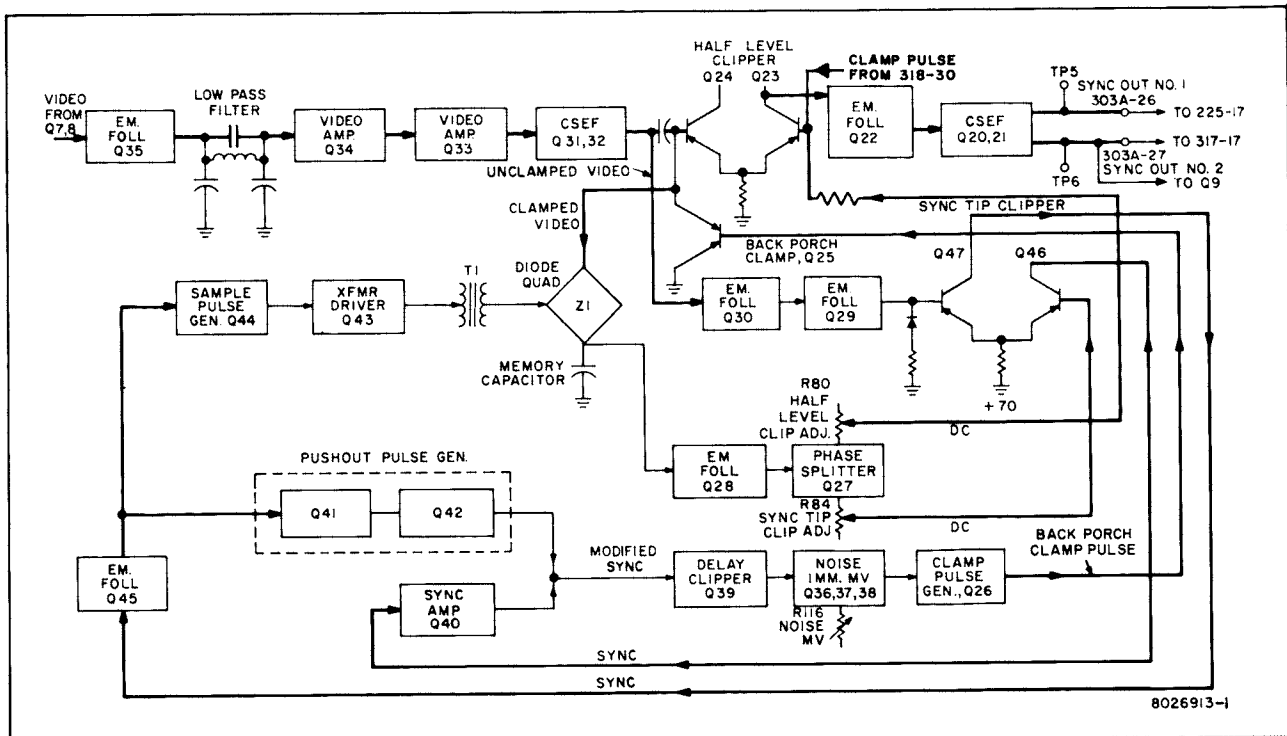


Figure 98—Block Diagram, Clamped Sync Separator Circuit, Board 2

put of the CSEF is ac coupled to the base of transistor Q24, which forms one section of the half-level clipper. At this point the back porch of the video signal is clamped to ground by a bidirectional switch, Q25. (See Back Porch Clamp.) A dc voltage from a phase splitter, Q27, is applied to the base of the second section of the clipper, Q23. This voltage is maintained at exactly one-half the level of incoming sync by a sensing circuit (described later). The clipper is so designed that only one of the two transistors conducts at a time. Q23 conducts throughout the portion of video more *positive* than the half-level of sync, and Q24 conducts throughout the portion of video which is more *negative* than the half-level of sync. The switching action occurs very rapidly and reproduces negative sync at the collector of Q23, timed exactly with the half-level point of the sync. Because of the half-level clipping action, the sync pulse at the collector of Q23 has a constant width, regardless of the input level. A $3.0\ \mu\text{sec}$ clamp pulse from module 318 is also fed to the base of Q23. This is timed to coincide with head switching, and is used to suppress transients caused by head switching, appearing in the Q23 output. The sync pulse from Q23 is fed to a CSEF, Q20, Q21 and then to two outputs. Output number 1 goes to module 317 in the headwheel servo system, and output number 2 goes to the ATC error detector module 225, where it serves as the tape sync from which the ATC error signals are derived.

Half-Level Sensor and Sync Tip Clipper

The half-level sensor consists basically of a keyed diode and detector, Z1. Video from the base of Q24 is fed to one of the four terminals of Z1, and a memory capacitor is connected from another terminal to ground. Equal and opposite keying pulses are applied from a transformer, T1, to the other two terminals just after the leading edge of sync. The diodes are open at all times, except when the keying pulses are present. When the pulses are applied, the memory capacitor charges to the level of the sync tip in the video signal. When the diodes are open, the capacitor has essentially no discharge path; and, therefore it remains fully charged. The capacitor is connected to the base of an emitter follower, Q28, having a very large input impedance which prevents the capacitor from discharging during the intervals between clamp pulses. The output of this stage is fed to a phase splitter, Q27, which produces two oppositely phased outputs proportional to the clamp voltage. One of these outputs is fed through a potentiometer, R80, to the base of Q23, in the half-level clipper. This potentiometer is adjusted so that its output is half of the sync tip voltage. The second output is fed through another potentiometer, R94, to another sync tip clipper circuit described in the next paragraph.

The keying pulses for the diode quad are made from sync provided by a clipper circuit, Q47 and Q46, similar to the half-level clipper. The clipping level of

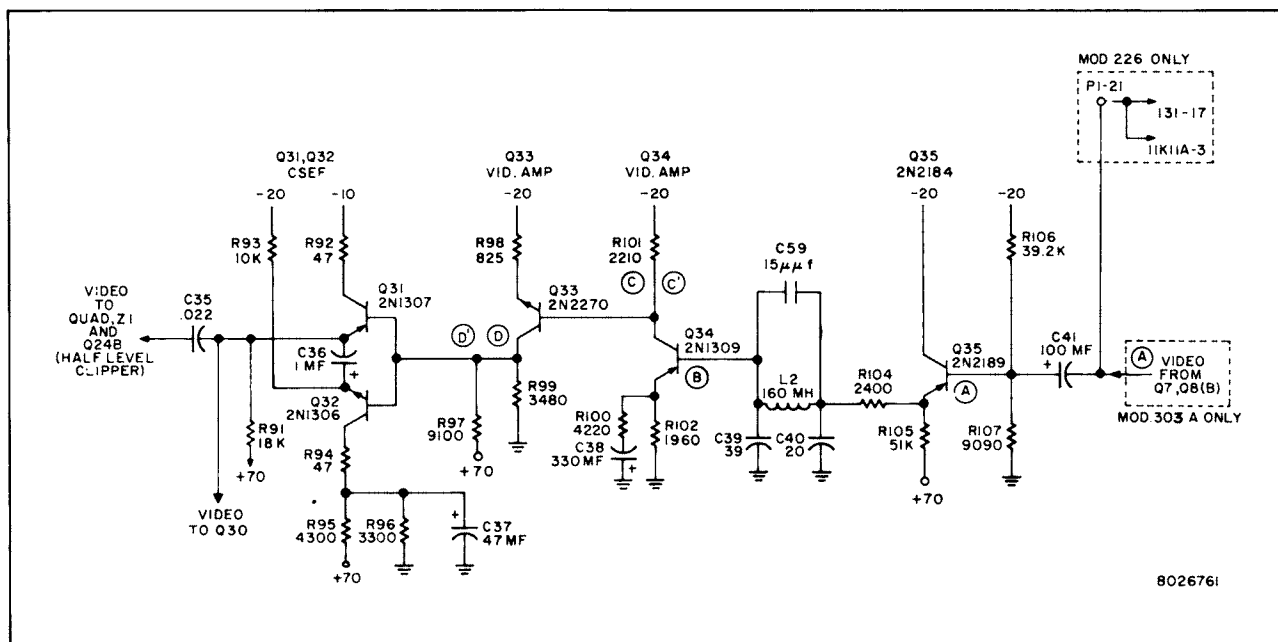


Figure 99—Video Amplifier Section of Clamped Sync Separator

Q47 and Q46 is determined by the second dc output of phase splitter, Q27, which is applied to the base of Q46 from R84. The video input to this clipper is obtained from the unclamped output of CSEF stage Q31, Q32. This signal is fed through two emitter followers, Q30 and Q29, to the base of Q47. A diode, CR21, in the base circuit of Q47 sets the dc level of the video signal to permit accurate clipping. Sync from Q47 is fed through an emitter follower, Q45, to a pulse generator, Q44. The output of Q44 is a narrow pulse whose leading edge is delayed slightly from the leading edge of sync. This pulse is amplified by driver Q43 and split into two equal pulses of opposite phase by transformer T1. The two pulses are applied to the quad, Z1, from opposite sides of the secondary of T1.

Back Porch Clamp Circuit

To insure that the sync timing information contained in the video is accurately reproduced by the sync separator, an elaborate clamp circuit is used to clamp the video to ground. The clamping is done during the back porch at the input to the half-level clipper. This is at the same point at which the half-level sensor measures the amplitude of sync tip with respect to the ground clamping point.

The back porch clamp circuit consists of the following circuits:

1. Switching Pulse Suppressor (Q39, Q40, Q41, Q42).

2. Noise Immunity Multivibrator (Q38, Q37, Q36).
3. Clamp Pulse Generator (Q26).
4. Bidirectional Switch (Q25).

The switching pulse suppressor (Q39, Q40, Q41, Q42) provides 10 volt negative going modified sync to the input of the noise immunity multivibrator. The modified sync is essentially the same as the original, except that switching pulses are eliminated and the horizontal sync and equalizing pulses are replaced by horizontal rate "pushout" pulses slightly wider than normal horizontal sync.

The noise immunity multivibrator, Q38, Q37, Q36; removes noise during the active scan time of the video signal, from the output of the switching pulse suppressor and divides by two during the 9H interval. The multivibrator output keys the clamp pulse generator, Q26, at the trailing edge of modified sync.

Q26 rings a tuned circuit which produces a high amplitude pulse of accurately controlled width. This pulse causes the bidirectional switch, Q25, to clamp the back porch level of the video input at the base of the half-level sync clipper Q23 to ground during the back porch of every horizontal blanking interval. However, in the 9H vertical period, clamping occurs at the black level intervals after every other equalizing pulse, and during every other serration of vertical sync. The clamp pulse width is controlled within close tolerances to prevent clamping too near the edges of sync.

CIRCUIT DESCRIPTIONS

The circuit of the clamped sync separator (see block diagram, figure 98) will be described in the following order:

1. Video Amplifier Circuits.
2. Path of unclamped video signal through emitter followers Q30, Q29 and sync tip clipper, Q47, Q46.
3. Signal path from sync tip clipper, through the half-level sensor, to the base of half-level clipper stage Q23.

4. Path from sync tip clipper through switching pulse suppressor, noise immunity multivibrator, clamp pulse generator, and back porch clamp.

5. Path of clamped video signal through the half-level clipper and sync output circuits.

Video Amplifiers (Q31, Q32, Q33, Q34, Q35)

The video signal from series amplifier stages Q7, Q8, on board 1 of module 303A is ac coupled to emitter follower Q35. (See A, figure 99.) This stage

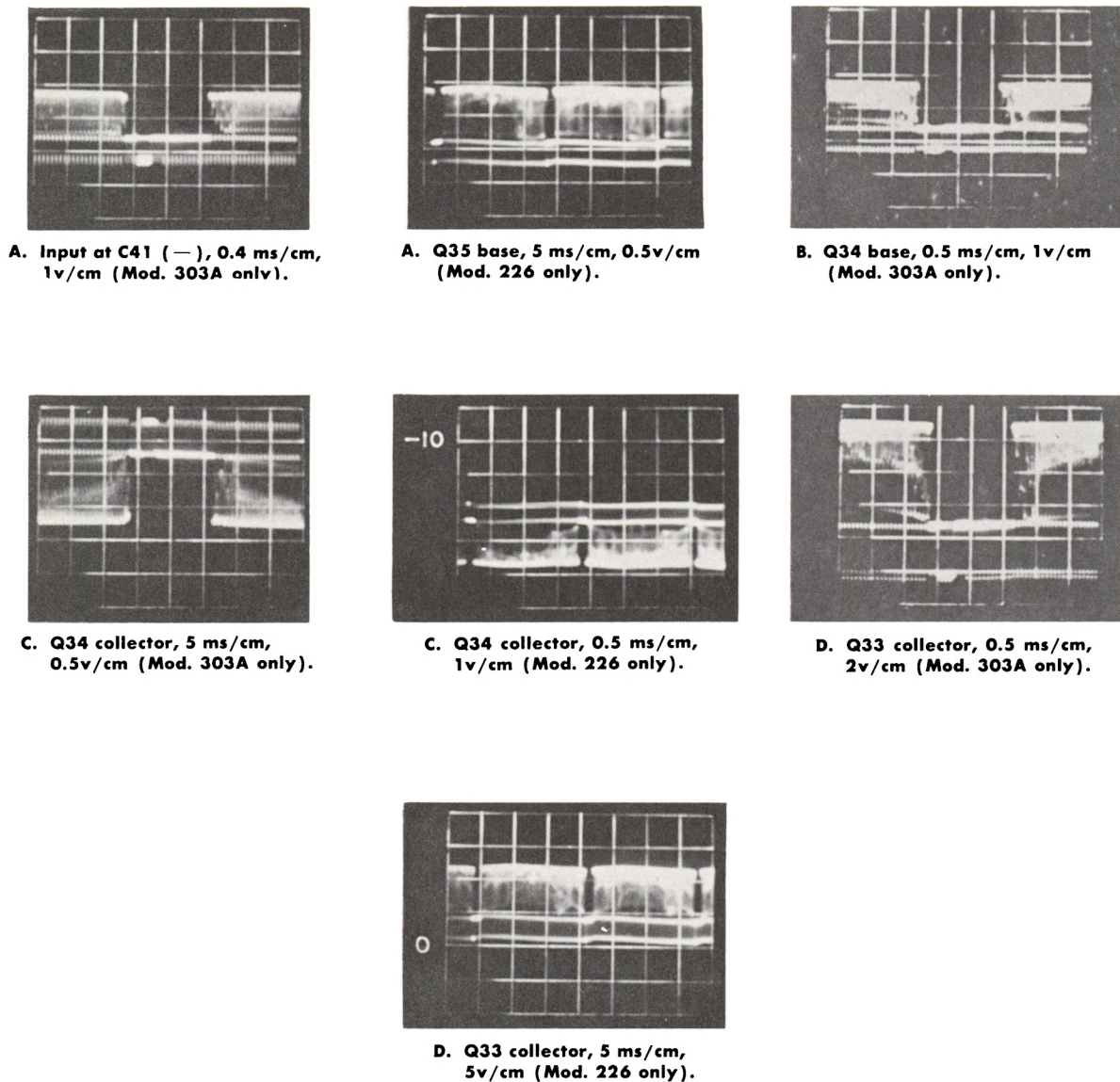


Figure 100—Typical Waveforms; Video Amplifier Section of Clamped Sync Separator

has a high input impedance to prevent loading of the video output line of Q7, Q8. The output of Q35 is fed through a low pass filter consisting of coil L2, capacitors C39, C40, and resistor R104, to the first video amplifier stage, Q34 (see B, figure 100). The filter removes high frequency video and noise but passes all frequencies below 1.2 megacycles. The gain of Q34 is determined by the parallel value of R100 and R102 in its emitter circuit.

The output of Q34 is amplified by Q33, which provides a gain of approximately 3.1. The video output of Q33 has an amplitude of approximately 10 volts peak-to-peak (see D, figure 100). This signal is fed to a CSEF stage Q31, Q32. Both of these transistors are biased on continuously to prevent a crossover region where neither transistor conducts. To prevent a heavy flow of dc current which would normally occur with both transistors biased on, the emitters are isolated from each other by a dc blocking capacitor, C36.

The output of the CSEF stage is taken from the emitter of Q31, and fed to two paths. In the first path, the signal is ac coupled through capacitor C35 to the base of half-level clipper stage Q24, and diode quad Z1. The video in this path is clamped to ground by back porch clamp Q25. In the second video path,

the video is dc coupled through two emitter followers, Q30 and Q29, to the base of Q47 in the sync tip clipper circuit. The emitter followers produce the proper drive, and isolate Q31, Q32 from the effects of the dc setting diode, CR21, in the base circuit of Q47.

Sync Tip Clipper (Q46, Q47)

The sync tip clipper consists of two transistors, Q46, and Q47, connected to a differential clipper circuit similar to that of Q23, Q24. (See circuit description under Half-Level Clipper.) The video signal having an amplitude of 10 volts peak-to-peak is taken from the output of CSEF stage Q31, Q32, and fed through two emitter followers, Q30, Q29 and capacitor C55, to the base of Q47. (See figure 101.) The base of Q47 is connected to the cathode of a dc setter diode which is biased on by R49. CR21 sets the tip of sync at approximately -1 volt. Consequently the 10 volt video signal on the base (see A, figure 102) goes from about -1 volt at the sync tips to $+9$ volts at the white peaks.

The base of Q46 is connected to a voltage divider in the collector circuit of phase splitter Q27 in the half-level sensor circuit. This divider provides a dc

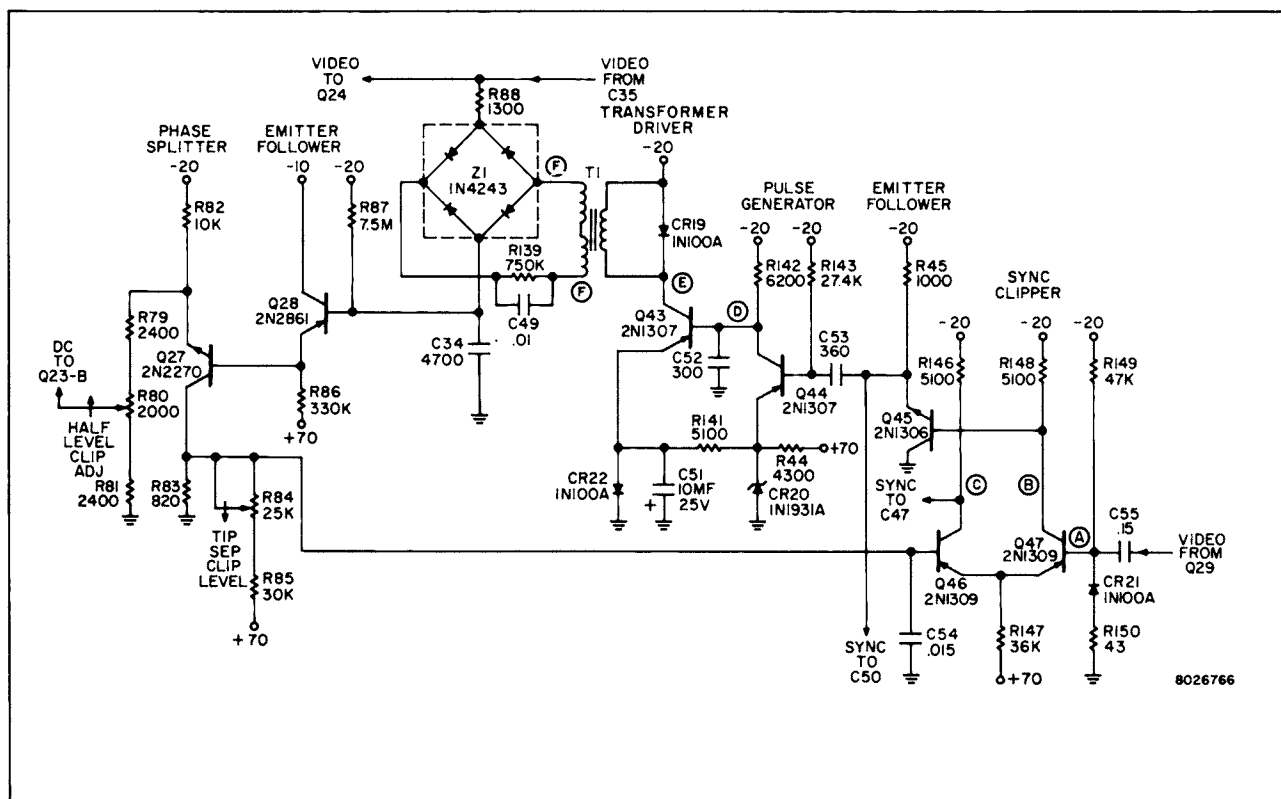
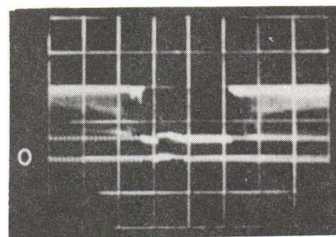
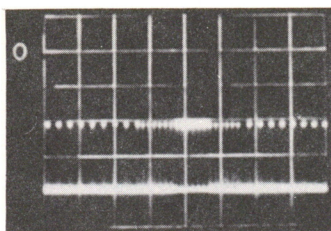


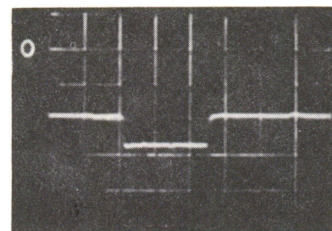
Figure 101—Sync Tip Clipper and Half-Level Sensor



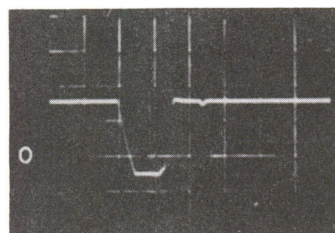
A. Q47 base, 0.5 ms/cm, 5v/cm.



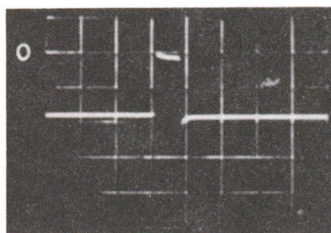
B. Q47 collector, 0.2 ms/cm, 5v/cm.



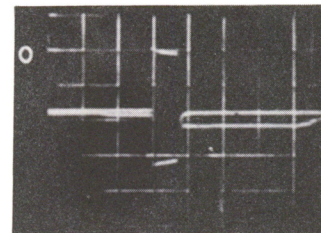
C. Q46 collector, 2 μs/cm, 5v/cm.



D. Q44 collector, 2 μs/cm, 5v/cm.



E. Q43 collector, 2 μs/cm, 10v/cm.



F. Top: T1-3, 10v/cm, Bottom: T1-5, 10v/cm, 2 μs/cm.

Figure 102—Typical Waveforms, Sync Tip Clipper and Half-Level Sensor

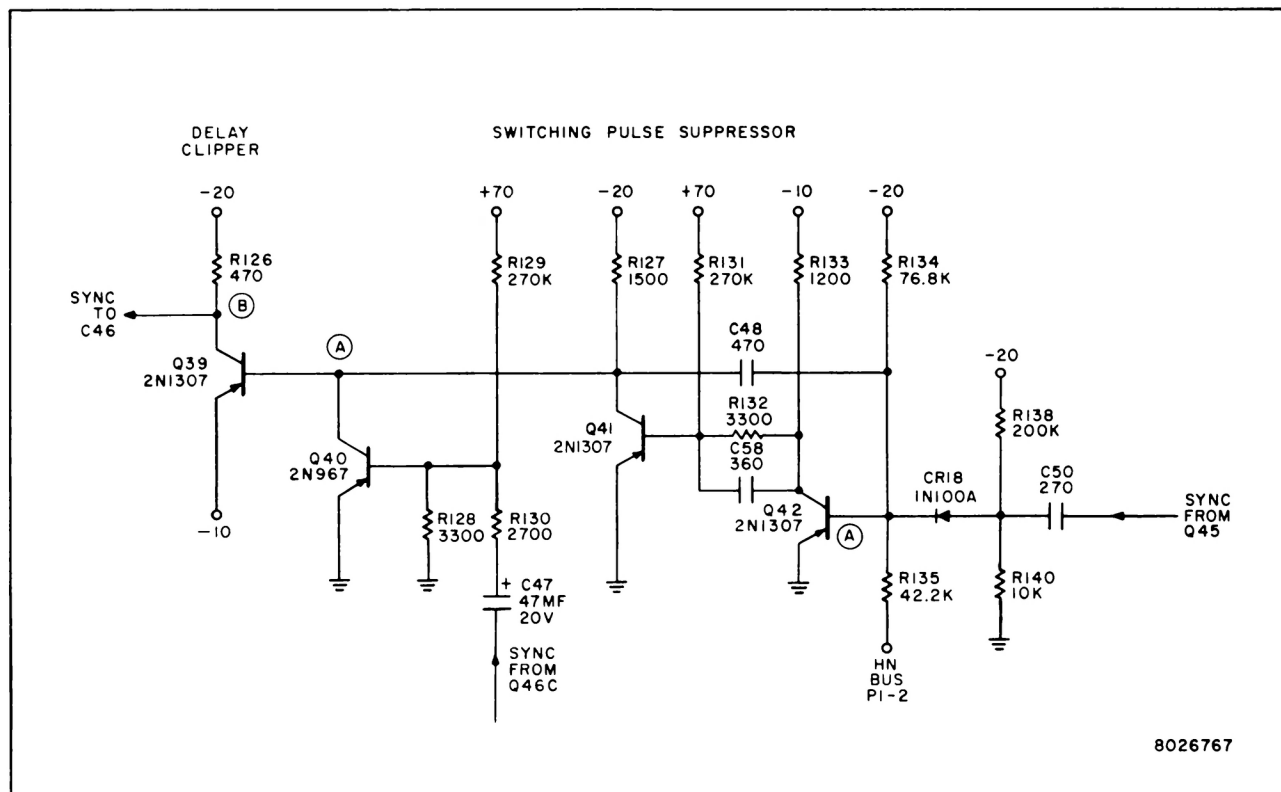


Figure 103—Switching Pulse Suppressor

voltage which depends both on the video level measured by the half-level sensor and the adjustment of TIP SEPARATION CLIPPING LEVEL potentiometer, R84. (See Adjustments.) Q46 is conducting and Q47 is cut off except when the video signal is more negative than the bias on Q46 base. The resulting outputs consist of a negative going sync pulse from -10 to -20 volts at the collector of Q46, (see C, figure 102) and a positive going sync from -20 to -10 volts at the collector of Q47 (see B, figure 102).

The negative sync from Q46 is fed through C47 to the base circuit of Q40 in the switching pulse suppressor (see figure 103). The positive sync from Q47 is fed to an emitter follower Q46. The output of Q45 goes to the input pulse generator Q44 in the half-level sensor, and, through C50, to stage Q42 in the switching pulse suppressor.

Half-Level Sensor (Q44, Q43, Z1, Q28, Q27)

The half-level sensor (see figure 101) consists of a pulse generator, Q44, transformer driver, Q43, keyed diode quad detector circuit, Z1, emitter follower, Q28, and phase splitter, Q27.

1. Pulse Generator, Q44.

The pulse generator, Q44, consists of a PNP transistor connected as a boxcar, or pulse narrowing circuit. The emitter of Q44 is connected to $+8$ volts established by Zener diode, CR20 and resistor, R44. Since the base is connected to -20 volts through R143 the transistor is normally conducting, and its base is approximately at $+8$ volts.

Positive going 10 volt sync pulses from Q45 are applied through C53 to the base of Q44. At the leading edge of sync, the base of Q44 goes 10 volts positive with respect to $+8$ volts and the transistor becomes cut off. Capacitor C53 then starts to discharge from $+18$ volts towards -20 volts through R143, but when the base reaches $+8$ volts, Q44 again conducts. The resulting output pulse (see D, figure 102) is narrower than the input pulse because the timed constant of C53 and R143 is made short so that the keying pulse is narrower than the equalizing pulse.

2. Transformer Driver (Q43).

In the steady state condition, the average current through Q43 establishes a dc charge on C51 of approximately -2 volts. Since the time constant of C51 and R141 returned to $+8$ volts is long compared to the 15,750 cps pulse rate of Q43, C51 does not have time to discharge between pulses and the bias on Q43 is essentially dc. Under the condition of no signal at

the input, there is no average current flowing through Q43 since it is normally off. Therefore the charge on C51 is held from going to $+8$ volts by diode CR22. This circuit action prevents collector to emitter breakdown at Q43 and a reverse polarity condition on C51 under no signal conditions.

The collector of pulse generator Q44 is connected directly to the base of Q43 which drives phase splitting transformer T1. Since the collector of Q44 (see D, figure 102) is normally at $+8$ volts and the emitter of Q43 is normally at -2 volts, Q43 is biased off. When a negative going pulse derived from the leading edge of sync occurs at the collector of Q44 the change from $+8$ to -2 volts (the conduction point of Q43 clamps the waveform) is slowed by the time constant at C52 and R142 returned to -20 volts. When Q43 is driven into saturation by the narrower boxcar pulse on its base, it produces a positive going narrow pulse of 18 volts (see E, figure 102) which has been delayed from the leading edge of sync by the action of C52 and R142. This delay in the half-level sensor keying pulse path insures that the amplitude sensing occurs only during the actual tip of sync and not on the leading edge of sync. Diode CR19, across the primary of T1 prevents inductive ringing.

3. Diode Quad (Z1).

The secondary of T1 is connected across two opposite terminals on diode quad Z1. Video from the CSEF stage, Q31, Q32 is fed through R88 to the third terminal of Z1, and also directly to the base of Q24 in the half-level clipper. The fourth terminal of Z1 is connected to memory capacitor C34.

When the pulse from Q43 is applied, two high amplitude narrow pulses of opposite polarity appear at opposite ends of the secondary (see F, figure 102). These pulses key all four diodes on simultaneously. The quad then acts as a switch, and feeds the video signal directly to the memory capacitor, C34, which charges to the level of the sync tip. The voltage on C34 with respect to ground is equal to the amplitude of the sync pulse because the back porch is clamped to ground by Q25. (See Back Porch Clamp.) During the pulse C49 and R139, between one end of the secondary and the quad, develop a bias voltage which cuts off the quad between pulses. When the quad is cut off the memory capacitor essentially has no discharge path except through 7.5 megohm resistor R87, to -20 volts. Thus the charge remains on the capacitor until the next keying pulses arrive.

4. Emitter Follower (Q28) and Phase Splitter (Q27).

The voltage on the memory capacitor, C34, is fed through very high input impedance emitter follower, Q28, to the base of a phase splitter, Q27. The emitter of Q27 is connected to the end of a voltage divider to ground, consisting of 2400 ohm resistors R79, 2000 ohm potentiometer R80 (HALF-LEVEL CLIPPER ADJUST), and 2400 ohm resistor R81. The voltage from the arm of R80 is fed to the base of half-level clipper stage Q23. R80 is adjusted to make this voltage equal to half the amplitude of the sync in the video fed to the other clipper stage, Q24.

An additional output, from a voltage divider in the collector circuit of the phase splitter, is fed to the base of Q46 in the sync tip clipper circuit. This voltage establishes the clipping level of the sync tip clipper, and can be adjusted with the TIP SEPARATION CLIPPING LEVEL potentiometer, R84.

Back Porch Clamp Circuit

1. Switching Pulse Suppressor (Q39, Q40, Q41, Q42).

The switching pulse suppressor (see figure 103) includes a delay clipper, Q39, transistor switch, Q40, and a pushout pulse generator consisting of a one-shot multivibrator, Q41, Q42. This circuit removes switching pulses from sync obtained from clipper Q46, Q47, and replaces the horizontal sync and equalizing pulses with pushout pulses slightly wider than horizontal sync. The differentiated trailing edge of this modified sync is used to trigger the noise immunity multivibrator, Q38, Q37, Q36.

The output of the switching pulse suppressor is taken from the collector of Q39. Therefore the action of the circuit can be understood by observing the voltage at this point under various conditions.

The collectors of transistor switch, Q40, and stage Q41 of the pushout pulse generator are both connected to the base of Q39. Both Q40 and Q41 are normally cut off since they are PNP transistors whose emitters are at ground and whose bases are returned to +70 volts (i.e., they form an "OR" gate). Q39 is a PNP transistor with its emitter at -10 volts and its base returned to -20 volts through a resistor. Therefore, when Q40 and Q41 are both cut off Q39 saturates and its collector goes to the potential of its emitter, or -10 volts. However, when Q40, Q41, or both, conduct, the base of Q39 becomes grounded and its collector goes to -20 volts.

Negative going sync pulses from differential clipper stage Q46 are fed to the base of Q40, and positive going sync pulses from emitter follower Q45 are fed

through a differentiating network and diode to the base of Q42. At the leading edge of horizontal sync, Q40 saturates and grounds the base of Q39. Simultaneously, the positive going differentiated leading edge of the sync from Q45 cuts off Q42 and causes Q41 to conduct. Thus, in effect the base of Q39 is grounded through two switches in parallel and Q39 is cut off. Q40 remains saturated as long as its base is negative, or normally, throughout the sync width. Q41, however remains saturated for the duration of the one-shot period of the multivibrator, which is slightly greater than the width of horizontal sync (see A, B, figure 104).

If the sync input to Q40 contains a switching pulse, the base of Q40 goes positive during the switching pulse and Q40 becomes cut off. However, the switching pulse always occurs during the one-shot period of the multivibrator. As a result, the pulse from the multivibrator "pushes out" the switching pulse, and the base of Q39 remains grounded through Q41.

At the end of the one-shot period Q41 becomes cut off. Q39 then conducts, and its collector (see B, figure 104) goes from -20 to -10 volts. Thus, in effect, the original horizontal sync pulse has been replaced by a 10-volt pulse whose width is equal to that of the pushout pulse.

When an equalizing pulse appears in the input to Q40 and Q42 the action is similar to that previously described for a horizontal sync pulse, since the one-shot period is greater than the width of the equalizing pulse. Therefore, in the output of Q39, an equalizing pulse is replaced by a pushout pulse.

During the vertical sync interval the action of the circuits is somewhat different. Serrated vertical sync consists of six wide pulses separated by narrow serrations. For purposes of this discussion each wide section will be referred to as a "vertical sync pulse". At the leading edge of each vertical sync pulse both Q40 and Q41 conduct and Q39 becomes cut off. Q41 conducts only for the width of the pushout pulse. However, since the vertical sync pulse fed to Q40 is wider than the pushout pulse, Q40 continues to conduct, after Q41 becomes cut off, until the trailing edge of the vertical sync pulse. As a result, the output of Q39 reproduces normal serrated vertical sync.

The width of the pushout pulse (see A, bottom waveform, figure 104), which is equal to the one shot period of the multivibrator (see A, top waveform, figure 104), depends on the negative voltage to which timing capacitor C48 discharges during the period. This voltage is determined by the potential on

the HN bus. The base of Q42 is connected to a voltage divider which goes from the HN bus, through resistors R135 and R134, to -20 volts. When the recorder is operating on 525- or 625-line standards the HN bus is at -20 volts, and therefore C48 discharges towards -20 volts. Under these conditions the one-shot period is about 5.2 microseconds. On 405-line standards, the HN bus is grounded, and the capacitor discharges towards a voltage of approximately -7 volts. This increases the one-shot period to correspond with the greater width of horizontal sync. In either set of standards the pulse is slightly wider than horizontal sync.

2. Noise Immunity Multivibrator (Q38, Q37, Q36).

The noise immunity multivibrator (see figure 105) removes noise (blanks during active scan) from the sync output of delay clipper Q39 and provides a sharp negative going edge to the clamp pulse generator, Q26 at the trailing edge of the modified sync. In addition, the multivibrator divides by two during the 9H vertical interval.

The circuit is a one-shot multivibrator whose unstable or one-shot period is a very high percentage of the time between trigger pulses. Since the circuit can be triggered only during the relatively short stable period, the output remains constant during the unstable period regardless of the presence of noise in the input signal.

To make the transition period between the unstable and stable states as short as possible the circuit includes an auxiliary transistor switch Q37 that reduces the time constant in the capacitor charging circuit by a factor of 10 to 1.

The noise immunity multivibrator consists of a monostable circuit, Q36 and Q38, with an auxiliary transistor switch in the collector circuit of Q36 (see figure 105). In the stable state Q36 is cut off and Q38 is conducting. This occurs because Q38 is biased on by the current withdrawn from its base through diode CR16 to voltage divider R118, R116 which runs from the HN bus to -20 volts. Under these conditions the collector, base, and emitter of Q38 are essentially at ground, the base of Q36 is at about 0.9 volt, and the collector of Q36 is at -20 volts. This means that capacitor C45, between the collector of Q36 and the cathode of CR16 must be charged to -10 volts with respect to the Q38 base.

Triggering of the multivibrator is accomplished by applying the negative 10 volt modified sync from the collector of delay clipper, Q39, through the differentiating network consisting of C46, R124, R125, and

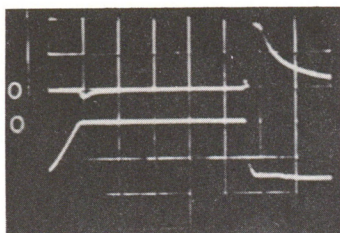
CR17 to the base of Q38. Diode CR17 allows only the positive going portion of the differentiated sync pulse to reach the base of Q38 (see figure 106). This pulse starts the one-shot period by cutting off Q38 and allowing Q36 to conduct. A 10 volt negative going edge coincident with the trailing edge of modified sync then appears at the collector of Q38 and triggers the clamp pulse generator Q26. Because the one-shot period is greater than half of a TV line the multivibrator divides by two during the 9H interval of vertical blanking.

At the start of the unstable period, the collector and base of Q36 go essentially to ground. Since the charge on C45 cannot change instantly, $+10$ volts is applied to the cathode of diode CR16. At the end of the trigger pulse the anode of CR16 goes to about $+0.5$ volt with respect to ground because it is returned to voltage divider R123, R122 connected between ground and $+70$ volts. Thus, since the cathode is at $+10$ volts the diode becomes cut off and disconnects the base of Q38 from C45. Therefore, the leakage current of Q38 is prevented from affecting the time period of the one shot multivibrator.

During the unstable interval the 10-volt charge on C45 discharges to a voltage determined by voltage divider R118, R116, which is connected between the HN bus and -20 volts. The rate of discharge, which determines the length of the unstable period, depends on the voltage at this point. This voltage depends on the adjustment of NOISE MV potentiometer R116 and the potential of the HN bus.

When the recorder is on 525- or 625-line standards, the HN bus is at -20 volts, and R116 is adjusted so that the interval between the leading and trailing edges of the multivibrator pulse is approximately 55 microseconds. On 405-line standards the HN bus is grounded. This increases the width of the pulse to approximately 87 microseconds.

As soon as the charge on C45 reaches about 0.5 volt, diode CR16 conducts and connects the base of Q38 to the capacitor. When the voltage goes slightly below ground Q38 starts to conduct and its collector rises from -10 volts to ground. The collector of Q38 is connected to the base of normally cut-off transistor switch, Q37, through capacitor C44. When the collector of Q38 makes the transition from -10 to ground a positive pulse passes through C44, which causes Q37 to saturate. Q37 then connects a 47-ohm resistor, R112, across the 470-ohm collector resistor of Q36, R110. This reduces the time constant of the charging path of timing capacitor C45 to about 1/10



Top: Q38 base, Bottom: Q38 collector. (2 μ s/cm, 5v/cm)

Figure 106—Typical Waveforms, Noise Immunity Multivibrator

and causes it to produce the clamp pulse.

3. Clamp Pulse Generator and Back Porch Clamp (Q26, Q25)

Q26 is normally conducting since it is an NPN transistor with its emitter connected to -20 volts and its base returned to ground through R78. (See figure 107.) At the trailing edge of modified sync, the noise immunity multivibrator produces a sharp negative going 10-volt edge at the collector of Q38. This pulse is fed through C33 to the base of Q26 and it cuts Q26 off. The sudden transition from the conducting to the non-conducting state shock excites coil L1 in the collector circuit of Q26 and causes it to ring. However, a damping circuit consisting of diode CR15 and resistor R75 allows it to ring for only one positive going half cycle. This half cycle constitutes a sharp positive going pulse approximately 1.5 microseconds wide (see A, figure 108).

The clamp pulse from Q26 is applied to the base of NPN bidirectional switch Q25 (B, figure 108). One collector/emitter element of Q25 goes to ground, and the other goes to the base of Q24 in the half-level clipper circuit. Q25 is normally cut off, since its base is returned to -20 volts through R73, CR15, R75 and R74. However, when the clamp pulse occurs Q25 saturates and clamps the video signal at the base of Q24 to ground (see C, figure 108).

Half-Level Clipper (Q23, Q24)

The clamped video signal (see figure 107) is fed to the base of Q24 in the half-level clipper circuit. This circuit is a differential clipper or "long-tailed pair" consisting of two transistors, Q23, and Q24. The emitters of these two transistors are tied together and connected through a large resistor (R71, 19.6K) to $+70$ volts.

A dc voltage equal to exactly one-half of the voltage between ground and the tip of the sync pulse is applied from potentiometer R80 in the half-level sensor, to the base of Q23. Since Q23 is a PNP it can conduct only when its emitter is more positive than this voltage. Similarly, Q24, which is also a PNP can conduct only when the voltage on its emitter is more positive than the video signal applied to its base. Because of the connection between the emitters of the two transistors, Q24 conducts when the video signal applied to its base is more negative than the dc voltage on the base of Q23, and Q23 is cut off during this period. Similarly, when the video level is more positive than the dc voltage the action reverses and Q24

is cut off, while Q23 conducts. The resulting output of Q23 is a negative going sync pulse having exactly half the amplitude of the sync in the video signal, and a constant width, regardless of the video level (see D, figure 108). Also a clamp pulse from the FM Switcher (module 318) is fed to the base of Q23. When the clamp pulse goes to ground potential, Q23 is cut off. The 3 μ sec clamp pulse is present every sixteenth sync pulse to suppress the switching transients caused by head switching.

Sync Output Stages (Q22, Q21, Q20)

The clipped sync from Q23 is fed to an emitter follower, Q22, and then to a complementary symmetry emitter follower, Q21, Q20 (see figure 109, and A, figure 110). Two outputs are taken from the CSEF stage through individual ac coupling networks each provided with test points. In module 303A sync output number 1 goes through P1-26 to the Tape Sync Processing Module, 317, in the headwheel servo system. This output may be observed at test point TP5 (see B, figure 110). Sync output number 2 goes to the input of the sync sensor circuit for the guide servo system, Q9 on module 303A, and also through P1-27 to the ATC error detector module, 225. This output, which may be observed at test point TP6, provides the timing information from which the ATC error signals are derived.

ADJUSTMENTS

The sync separator adjustments involving R84 (SYNC TIP CLIP ADJ), R80 (HALF LEVEL CLIP ADJ) and R116 (NOISE MV) are critical and have been carefully made at the factory. Readjustment will be required only if the settings on these controls have been disturbed or if components affecting the adjustments have been replaced.

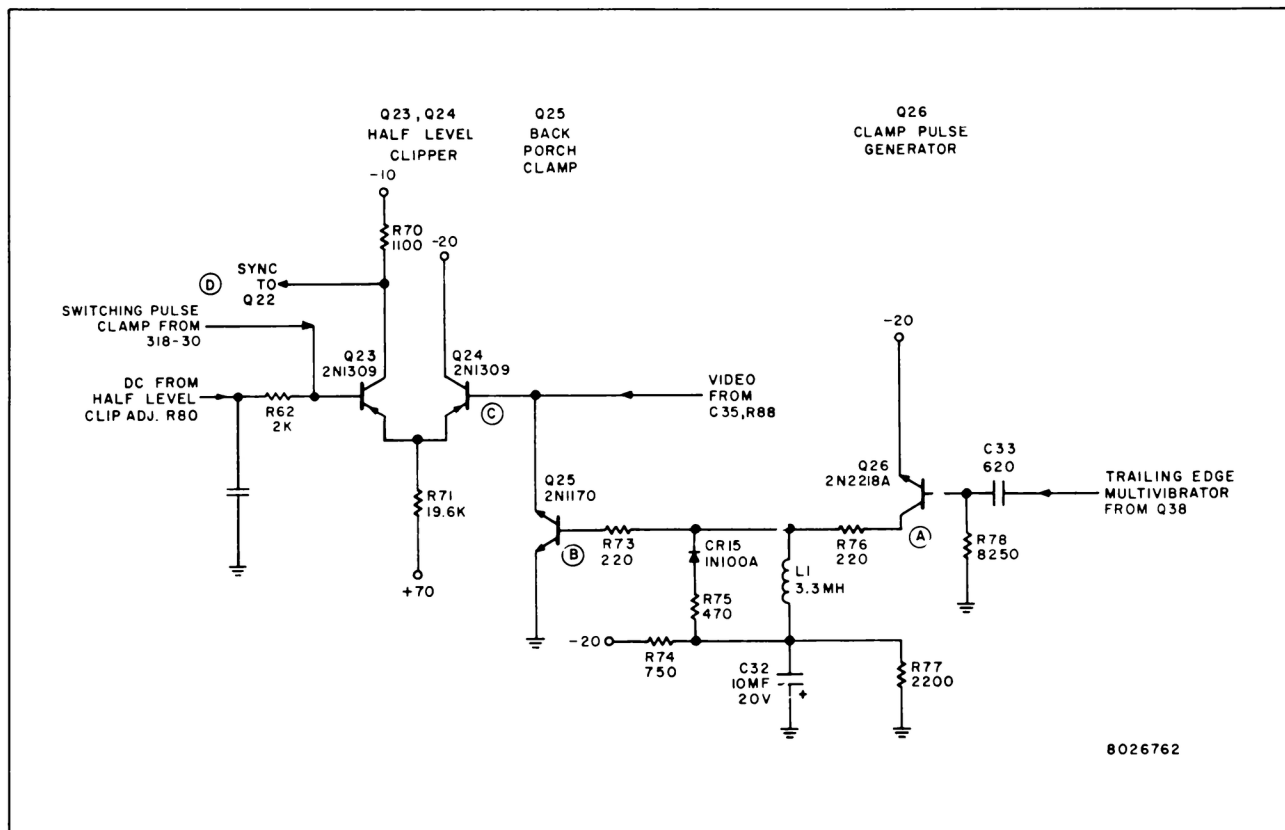
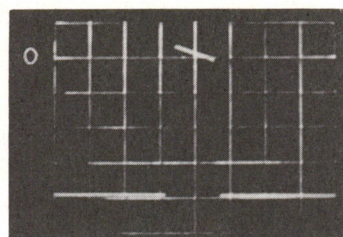
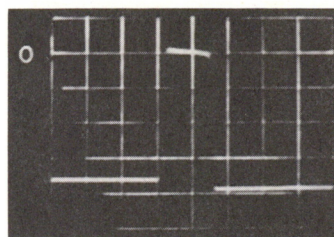


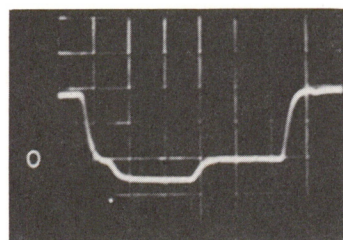
Figure 107—Half-Level Clipper and Back Porch Clamp



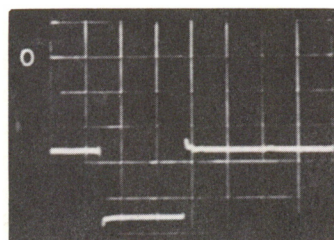
A. Q26 collector, 1 μ s/cm, 5v/cm.



B. Q25 base, 1 μ s/cm, 5v/cm.



C. Q24 base, 2 μ s/cm, 5v/cm.



D. Q23 collector, 2 μ s/cm, 2v/cm.

Figure 108—Typical Waveforms, Half-Level Clipper and Back Porch Clamp

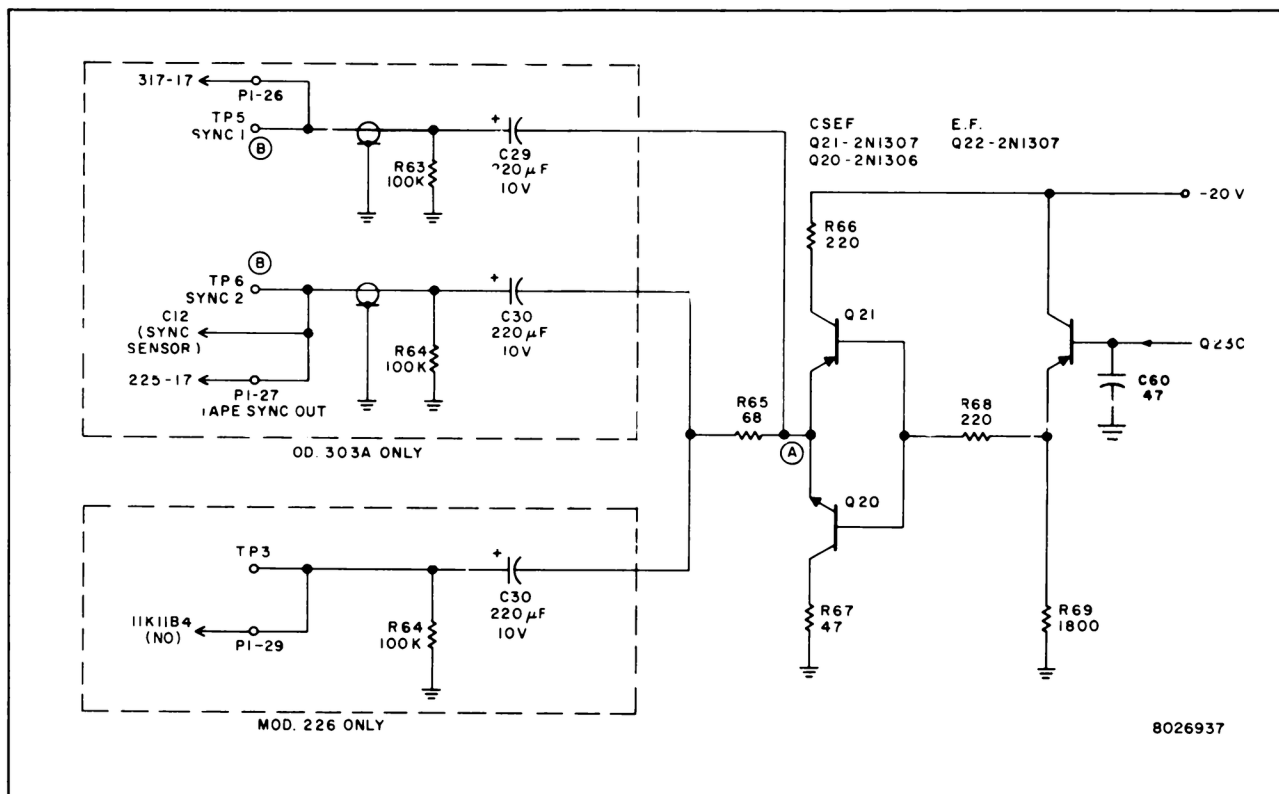
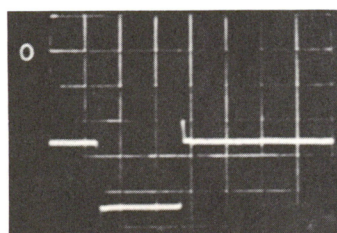
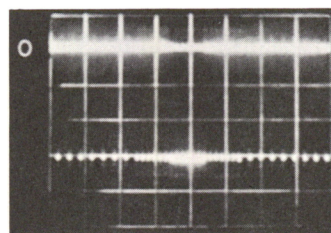


Figure 109—Sync Output Amplifiers



A. Q20, Q21 Emitter, 2 μ s/cm, 2v/cm.



B. TP5, TP6, 2 ms/cm, 1v/cm (Mod. 303A Only)

Figure 110—Typical Waveforms, Sync Output Amplifiers

The adjustment procedure is in two sections. The first section is the Performance Check and this includes the adjustment of R84. The second section covers the adjustment of R80 and R116. When troubleshooting the sync separator stages, always go through the Performance Check procedure first, then proceed with the Adjustment of R80 and R116, if required.

RECOMMENDED TEST EQUIPMENT

Dual Trace Oscilloscope, such as Tektronix 535A with CA plug-in amplifier.

Video attenuator box.

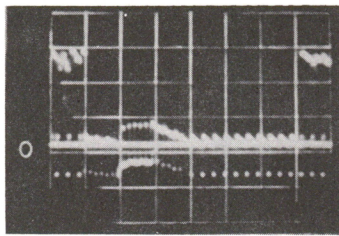
Source of composite monoscope signal.

3-volt negative bias source (battery or regulated dc source with adjustable output voltage).

.022 μ f capacitor.

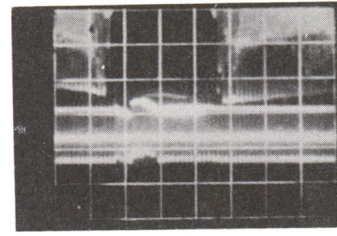
Performance Check

1. Remove the Demodulator Output (module 303A) from the TR-22. Disconnect the minus (input) side of capacitor C41 from the terminal. Using coaxial cable with alligator clips, connect an attenuator between this terminal and the minus side of C41.



A. Q47 base (Vert. Interval).
B. Q46 base (DC Line), (2 ms/cm, 1v/cm)

**Figure 111—Sync Tip Clipper Check
(Low Level Video)**



A. Q47 base (Vert. Interval).
B. Q46 base (DC Line), (0.5 ms/cm, 2v/cm)

**Figure 112—Sync Tip Clipper Check
(Normal Level Video)**

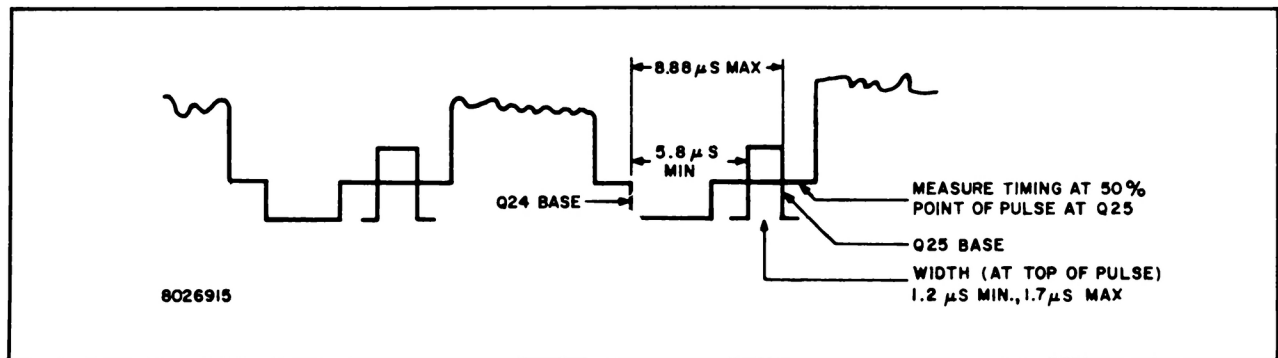


Figure 113—Timing of Clamp Pulse on Back Porch (525-Line Standards)

2. Place module 303A in an extender and insert it in the TR-22.

3. Place the TR-22 in STOP mode and on 525-line standards.

4. Apply a monoscope signal to the video input of the TR-22. Set the attenuator for zero attenuation. Press the DEMOD OUT button of the CRO and adjust the LEVEL control on the Video Input (module 103) for 1-volt peak-to-peak on the CRO. (With the video adjusted to this level, the amplitude of the video input at C41 should be approximately 2 volts.)

5. Adjust the attenuator to obtain .8 volt at C41.

6. Set the oscilloscope for dc measurement and match both probes. Connect one probe to the base of Q47 and the other probe to the base of Q46. Observe the vertical interval on the base of Q47 at a vertical rate. Switch the oscilloscope to alternate. The dc line on the base of Q46 should be just below the black level of the lowest set of sync pulses, as shown in figure 111. If necessary adjust R84 (SYNC TIP CLIP ADJ) to obtain this result.

7. Restore the video level at C41 to 2 volts. The dc line on the base of Q46 should pass through approximately in the center of the sync pulses (figure 112).

8. Connect one oscilloscope probe to the base of Q24 and the other probe to the base of Q25. Adjust the sweep rate until two complete patterns are displayed, and then check the timing as shown in figure 113. Absence of the clamp pulse from the back porch of one of the two sync pulses indicates that the noise immunity multivibrator (Q36, Q37, Q38) is dividing by two. If this occurs check the adjustment of R116 (NOISE MV) as instructed in steps 6 and 7 under Adjustment R80, R116.

a. If required switch to 405-line standards and adjust the oscilloscope until two complete patterns are displayed. The timing of the clamp pulse should meet the limits shown in figure 114. If the clamp pulse is absent, proceed as just instructed for the same condition on 525-line standards.

9. Switch to 525-line standards; switch the oscillo-

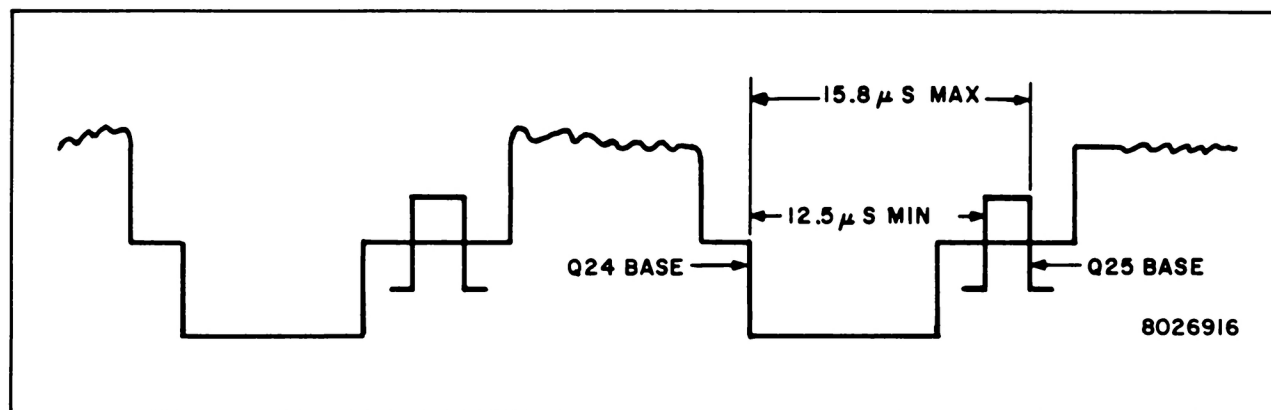
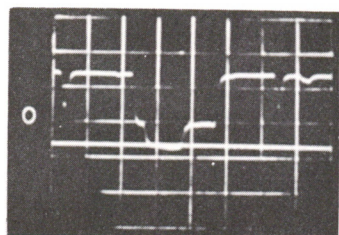


Figure 114—Timing of Clamp Pulse on Back Porch (405-Line Standards)



**Top: Junction C34, Z1, 5v/cm,
Bottom: Junction R88, C35, 5v/cm.
(Sweep rates 5 μs/cm)**

Figure 115—Sync Tip DC Level Check

scope inputs to dc. Connect both probes to the junction of R88 and C35 and match the probes. Then connect one probe to the junction of C34 and Z1. The dc level at C34/Z1 should be the same as that of the sync tip at C35 and the back porch should be at ground.

10. Observe the output of the sync separator at TP6 at the horizontal rate and then at the vertical rate. The sync amplitude should be 3.2 to 3.4 volts. All equalizing pulses, vertical pulses and horizontal pulses must be present at normal amplitude.

Adjustment of R80, R116

1. Disconnect C35 from the junction of Q31 emitter and Q30 base. Also disconnect the lead from the junction of R72 and the base of Q24. Bypass the base of Q24 with the .022 μf capacitor. Connect the bias source to the junction of R88 and Z1 and adjust the bias to -3 volts.

2. Adjust the video level at C41 to 2 volts.

3. Switch the oscilloscope inputs to dc and con-

nect both probes to the junction of C35 and R88. Calibrate both probes to read the same with respect to ground. Connect one probe to the junction of C34 and Z1. The voltage at this point should be the same as the bias applied to C35 (see figure 115).

4. Remove the probe from the junction of C35 and R88 and connect it to the arm of R80, the HALF LEVEL CLIP ADJ. Adjust R80 until the voltage is equal to half of the voltage at C34. (Measure both voltages with respect to ground.)

5. Remove the -3 volt bias supply. Remove the .022 μf capacitor and reconnect the lead to the junction of R72 and the base of Q24. Reconnect C35 to the junction of Q31 emitter and Q30 base.

6. Connect one probe to the collector of Q38 and the other to the base of Q47. Adjust R116 (NOISE MV) for a pulse width of 55 microseconds, as shown in figure 116.

7. If required, switch to 405-line standards. The width of the pulse at the collector of Q38 should be 87 microseconds, as shown in figure 117. Compare the pulse with the horizontal sync at the base of Q47 to make certain the latter is not dividing by two. If division occurs, readjust R116 slightly and recheck the pulse width on 525-line standards as instructed in step 6.

VIDEO CONTROL (Module 131B)

(Refer to Block Diagram Figure 118)

The video input signal is fed from the Demodulator Output (module 303A) through an attenuator network to the video amplifier, Q1. This circuit has a normal gain of one which is adjusted by the video level R48.

The master video level control for the machine is located on the front of this module, although it con-

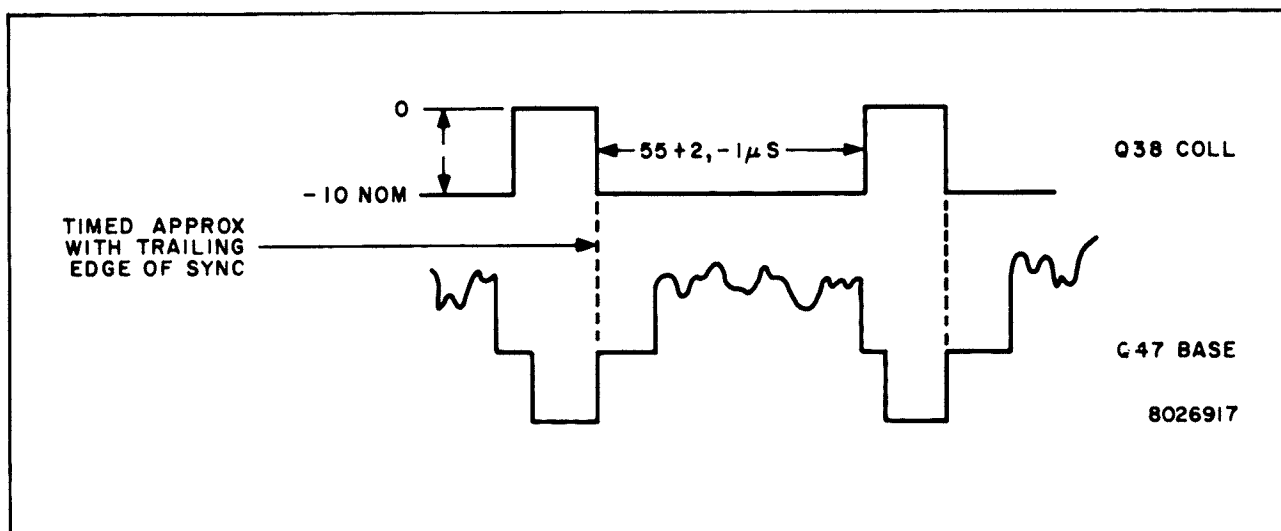


Figure 116—Noise Immunity Multivibrator Timing, R116 Adjusted for 525-Line Standards

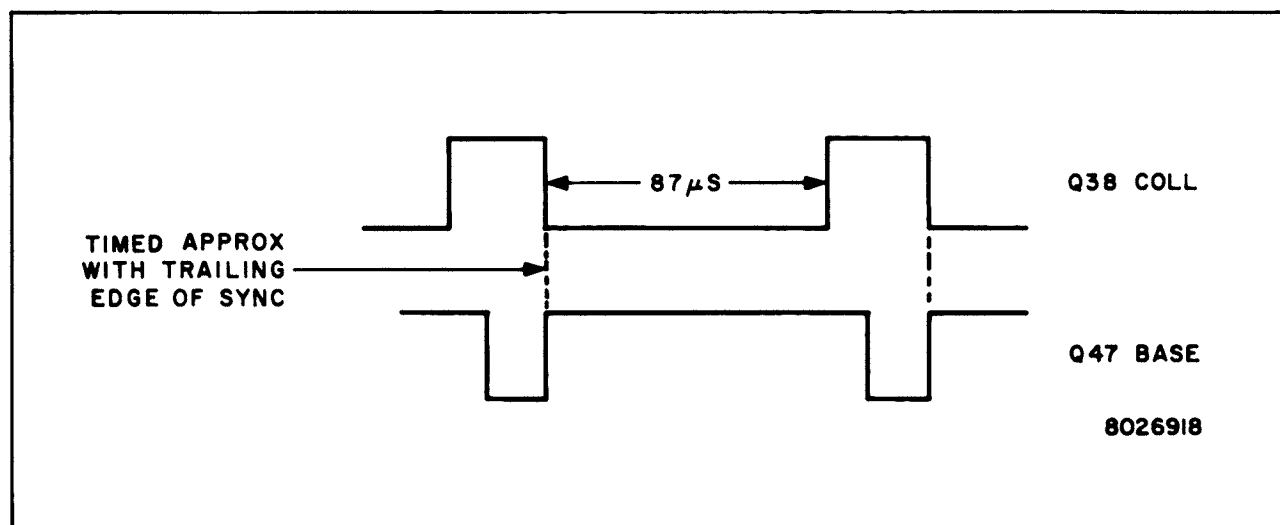


Figure 117—Noise Immunity Multivibrator Timing, R116 Adjusted for 405-Line Standards

trols the current passed by transistor, Q8 which in turn controls the illumination to a pair of lamps in the Demodulator Output (module 303A). These lamps are used for the illumination of a Photo Electric cell in the 303A to actually control the gain of the Demodulator Output module.

Relay K1 selects either R15 (local) control or a similar control on the remote control panel if used with the machine. Likewise relay K1 selects local pedestal control R43, or one on the remote control panel. The pedestal control adjusts the dc level at which the sync is clipped in the video output module.

Clamping for monochrome amplifier Q5 base is performed at this point to eliminate tilt and any residual hum that might exist in the signal. The clamp pulse of 1.5 microseconds width is developed

in the sync logic (module 230B) and the amplifier Q12 supplies signal of the proper level to the clamp driver, Q9. Q9 is actually a phase splitter which supplies both negative and positive clamp pulses to opposite sides of the clamp quad Z1. Clamping takes place on the back porch.

Normally, gain control R48 is set for unity gain between the input of module (131B) and the actual video output of the machine.

Video is applied via 11K11A and P226-21 from the Demodulator Output (module 303A) or if the MATC system is in use, from the Delay/Output (module 223A). The incoming video is coupled through C1 to the base of Q1, the video amplifier (see figure 119.) The gain of this stage is unity and this is set at the factory by means of potentiometer R48. The latter

is an internal control, the setting of which should not be disturbed unless the gain of Q1 is affected due to component replacement or for some other cause. Shunt peaking is employed for high frequency compensation of this stage. Coil L1 in the collector load is used for this purpose.

The output from the collector of Q1 is direct coupled to the base of Q2, a second video amplifier. This amplifier is connected in an emitter follower configuration to provide a low impedance source for driving the succeeding feedback amplifier. From the emitter of Q2, the signal is coupled through R13, R5, and C6 to the base of Q3, which in conjunction with Q4 forms the feedback pair.

The video gain control, Q8, an emitter follower, and the associated control components, K1 and potentiometer R15, are part of a variable gain control circuit for setting the video level. (Potentiometer R15 is a front panel control designated LEVEL). The other part of the circuit is in the Demodulator Output (module 303A) and consists of a photocell (V1), two lamps (DS1, DS2), and a plexiglas prism.

The LEVEL control determines the bias on Q8 which serves as the current source for the lamps. Light from the lamps is transmitted through the prism to the photocell which acts as a variable resistance in the path of the signal being applied to the Demodulator Output circuits. The resistance of the photocell is directly proportional to the light received from the lamps. Therefore, varying the light intensity by adjusting the LEVEL control changes the resistance of the photocell and consequently the video level.

The feedback amplifier is an arrangement of a common emitter amplifier (Q3) which inverts and amplifies the signal, and an emitter follower (Q4) which presents a low impedance output to the clamp circuit. The base of Q3 is biased by a voltage divider consisting of Q4, R14, R25, and R18. Transistor Q4 has to be in the circuit for normal transistor action of Q3. In case Q4 is disconnected, no dc current is applied to the R14, R18 portion of the voltage divider, thereby placing the base of Q3 at ground potential. Thus, Q3 will be cut off and no signal will flow to the collector of Q3. The output of the amplifier is fed to Q5, the first of two monochrome amplifiers. The high level of this signal insures stable clamping.

Transistor Q5 is an emitter follower, the base of which is clamped at the proper operating point by the bridge connected diodes in clamp Z1 (see figure 121). The clamp pulses are timed to occur during the back porch interval.

Blanking is supplied from the Sync Logic (module 230B) to the base of the blanking adder, Q7, which operates in conjunction with the black clipper, Q19, in the Video Output (module 233A).

The pedestal (PED) control, R43, in the emitter circuit of Q7 adjusts the dc level at which the sync is clipped by the black clipper, Q19. This makes the signal go either more positive or more negative with respect to the clamping reference, -12 volts. When blanking arrives, the blanking adder, Q7, conducts, allowing clipped sync and blanking to flow through it and be eliminated. At the same time, the black clipper, Q19, is cut off; therefore, no signal is passing through it. However, when the actual video signal (positive with respect to clamping reference) arrives after blanking, the actions of Q7 and Q19 are reversed. Transistor Q7 is cut off, acting as an open circuit, while Q19 conducts and allows the signal to flow through it. No usable signal appears on the emitters of Q7 and Q19 because Q19 acts as a common base amplifier whose signal input impedance is so low that it is almost a short circuit.

Diode CR2 sets the negative peak of the blanking signals at -12 volts. The -12 volts clamping reference is obtained from the base of the black clipper, Q19.

ADJUSTMENTS

In order to make the response adjustment described below, the Video Control module should be mounted in an extender.

1. Disable the clamp, Z1, by disconnecting the wire at the yellow dot on Z1 from the terminal on the board. Connect a 10K resistor between this terminal and the terminal with the green dot connection from Z1.
2. Withdraw the Video Output module from the recorder and place the SYNC switch, S1, in the OFF position; then replace the module.
3. Connect the sweep output of a video sweep generator, with the sweep rate set at 0 to 8 mc, to the junction of R1 and R2. Connect an oscilloscope lead to this junction and adjust the output of the generator to obtain a .5v peak-to-peak signal on the CRO.
4. Turn the PED (pedestal) control, R43, fully cw. Connect the oscilloscope to connectors 12J11-VIDEO OUT (SW) on the recorder. Terminate the oscilloscope in 75 ohms. Adjust coil L1 for flat response to 8 mc., i.e., the video input and output should be matched.

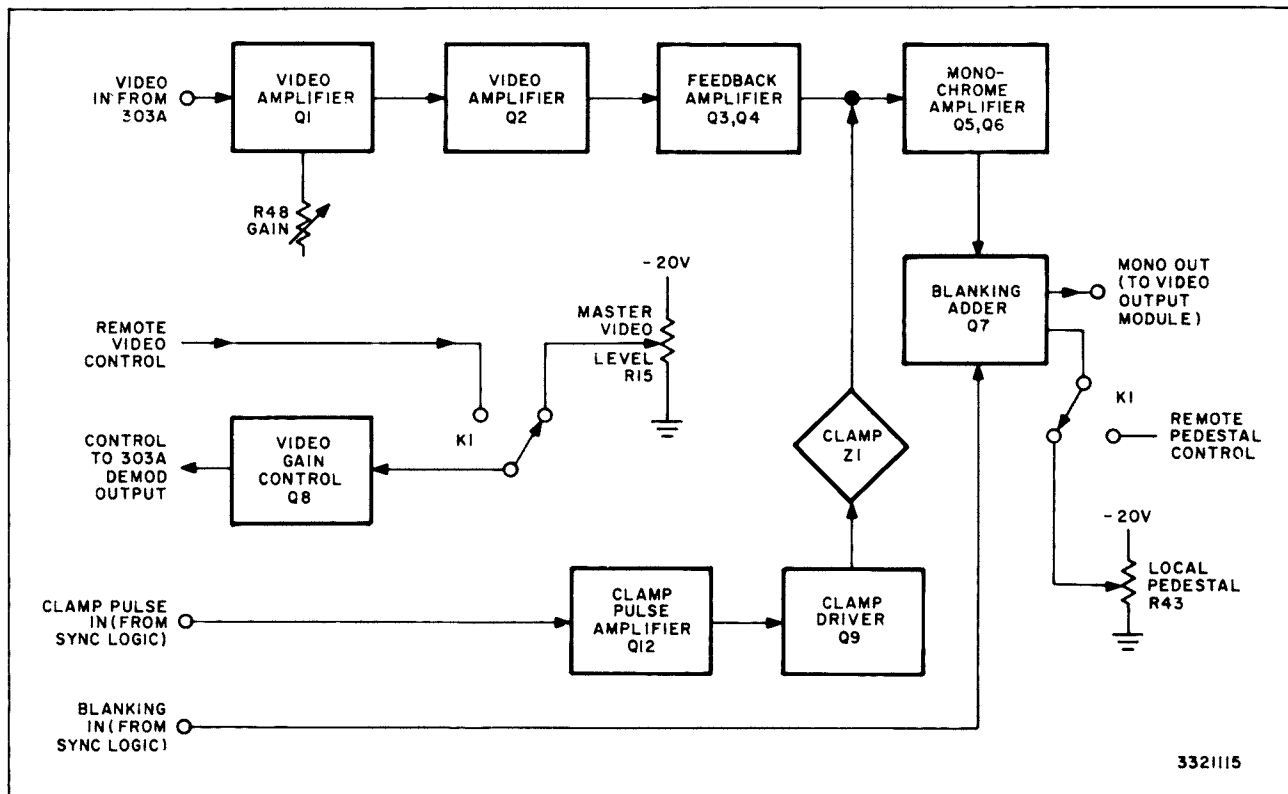


Figure 118—Simplified Block Diagram, 131B Video Control Module

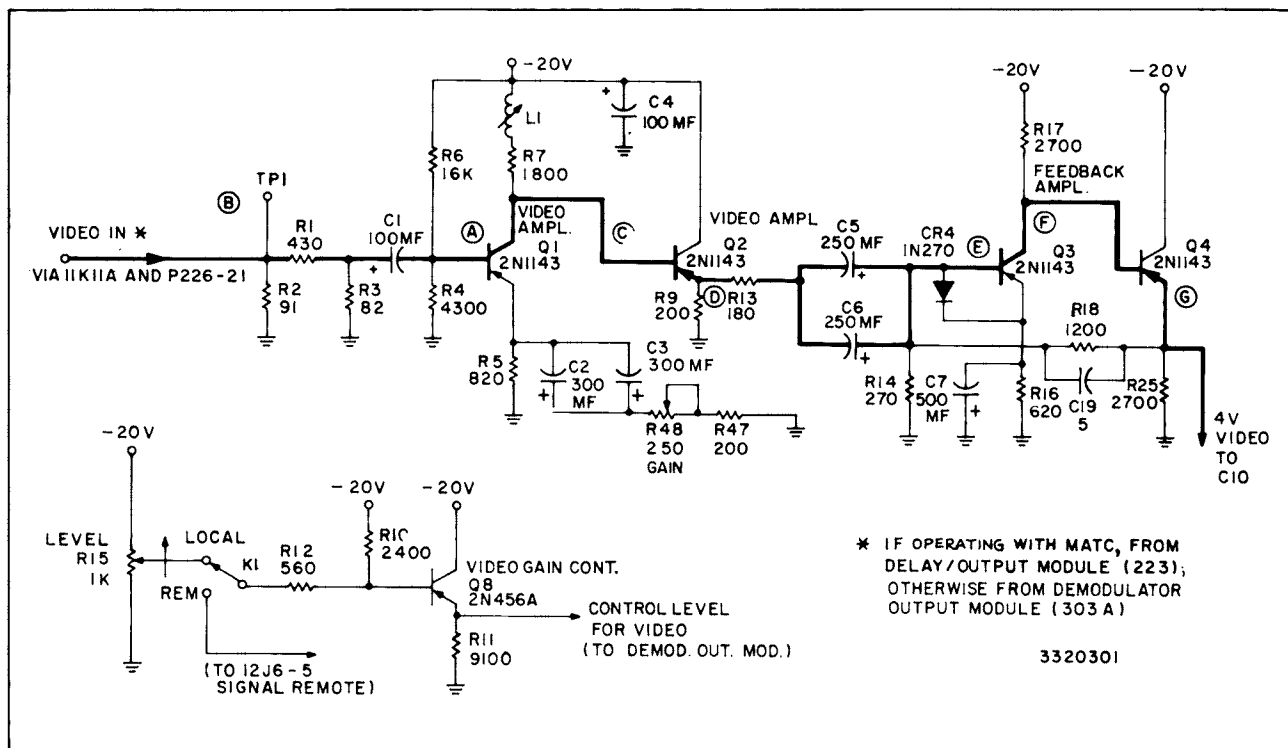


Figure 119—Video Feedback Amplifiers and Video Control Level

5. Remove the 10K resistor and re-connect quad Z1, and replace the module in the tape recorder. Return the SYNC switch to the ON position.

VIDEO OUTPUT (Module 233A)

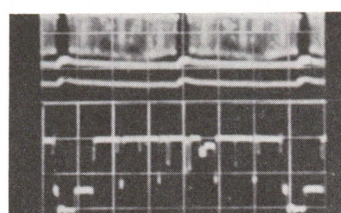
(Refer to Block Diagram Figure 123)

The Video Output module combines the video signal and the regenerated sync to form the composite video signal which is available at five separate outputs. An output is also provided by Q2 for a 4-volt peak-to-peak regenerated sync.

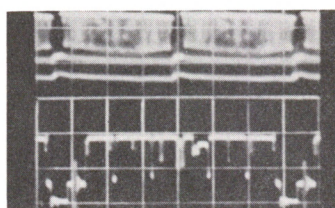
A 0.55 microsecond delay line is inserted in the monochrome video path to equal the delay of the sync signal path which is more complex.

If color operation is utilized in the machine, the boost and color signals are mixed via the chroma adder, Q9. Sync gain control transistor Q10 is controlled locally by the sync level control on the front of module 132 in the playback control area. If remote operation is used, a similar control on the remote panel is selected by a relay K1 in module 132.

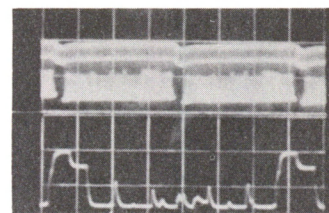
The -15 volt regulator is used to supply the series



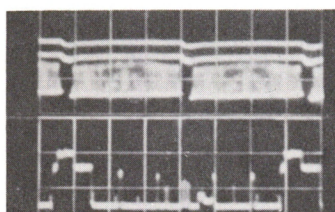
A. Q1 base
Top: 5 ms/cm, .1v/cm
Bottom: 10 μ s/cm, .1v/cm



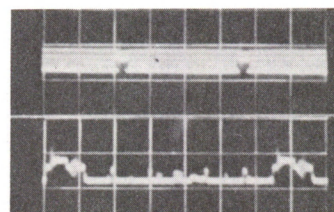
B. TP1
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



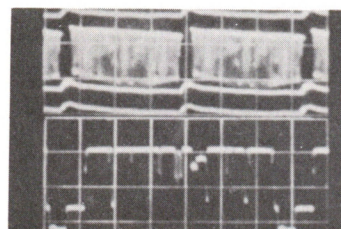
C. Q1 collector
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



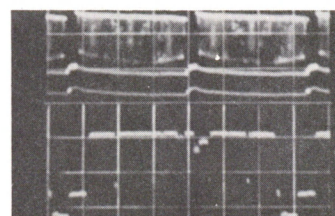
D. Q2 emitter
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



E. Q3 base
Top: 5 ms/cm, .05v/cm
Bottom: 10 μ s/cm, .05v/cm



F. Q3 collector
Top: 5 ms/cm, 2v/cm
Bottom: 10 μ s/cm, 2v/cm



G. Q4 emitter
Top: 5 ms/cm, 2v/cm
Bottom: 10 μ s/cm, 2v/cm

Figure 120—Typical Waveforms, Video Amplifiers and Video Gain Control Circuits

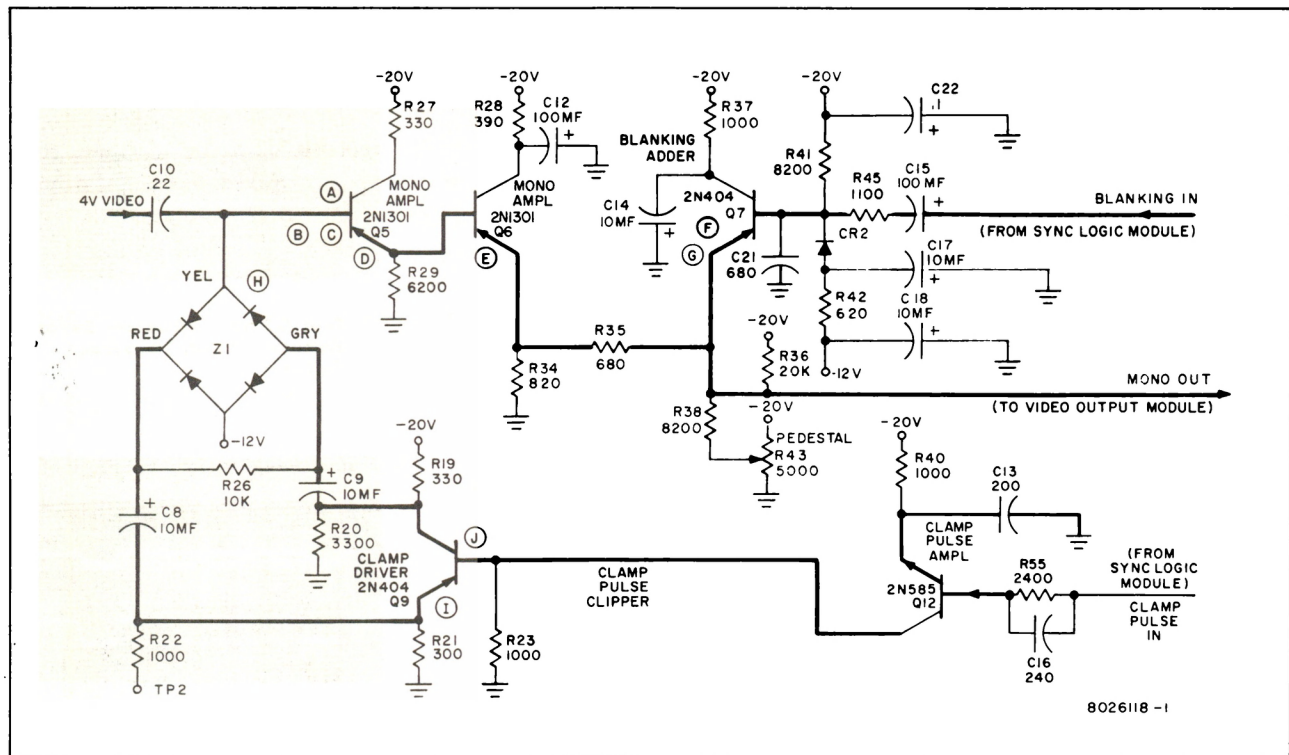


Figure 121—Mono-Amplifier, Blanking Adder and Clamp Pulse Amplifier, and Clipper and Driver Circuits

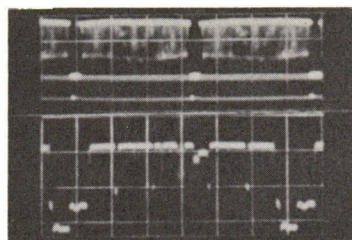
output amplifiers and the driver Q7, Q8.

As shown in the simplified schematic, figure 124 and waveforms in figure 125, the processed monochrome signal from the Video Control (module 131B) is fed to the black clipper, Q19. The clipper conducts when the emitter voltage is more positive than the -12 volts supplied to the base. The -12 volts is also supplied to the blanking adder, Q7, which is located in the Video Control module. Transistor Q7 in conjunction with Q19 effectively clips and eliminates all signals more negative than the clamping reference level. Thus sync and any unwanted signals are removed during the blanking interval. From the collector of Q19 the signal is fed to the delay circuitry. The latter consists of Q21, an emitter follower, the delay line itself, and Q20, a common base amplifier.

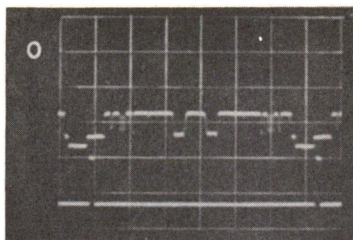
The emitter follower input provides proper driving impedance for the delay line and the common base amplifier provides proper termination of the line. The delay of the line is .55 microseconds, which compensates for the delay encountered by sync in the sync separator circuit in the Demodulator Output (module 303A). The delay insures that the proper timing relationship will be maintained between video and regenerated sync when the latter signal is reinserted in the video later. The delayed output on the collector of Q20 is direct coupled to a series amplifier.

The series amplifier consisting of Q7 and Q8 serves as the video output driver stage for each of the five identical series output stages. The series arrangement of Q7, Q8 provides signal polarities and amplitudes such that the voltage gain of the pair is unity and the output impedance low. Both ac and dc stabilization are incorporated to preserve constant levels.

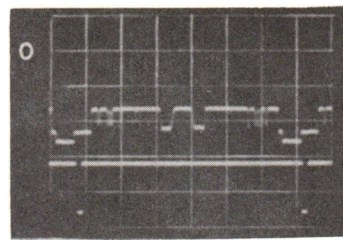
Regenerated sync from the Sync Logic module is fed to the base of the sync output amplifier, Q2, and to the base of the sync adder, Q1, through the pulse shaping circuits, R9, C3, and R8, C2 respectively. (See figures 126 and 127.) The sync gain control stage of Q10 is used to control the level of sync. This stage permits local or remote control of the sync amplitude. The SYNC GAIN potentiometer, R27, for local control is located on the FM Equalizer module. The sync output from Q1 is added to each of the five video outputs through the isolation resistors, R1, R2, R3, R4, and R5. The sync on-off switch, S1 (mounted on the component board) is normally in the On position, but may be turned to OFF to remove sync from the video signal at VIDEO OUT No. 5, if desired. The separate sync output is obtained from the collector of Q2 through resistor R10. The latter is 75 ohms to provide matching termination for the line.



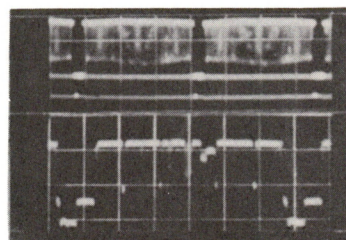
**A. Q5 base. Top: 5 ms/cm, 2v/cm
Bottom: 10 μs/cm, 2v/cm**



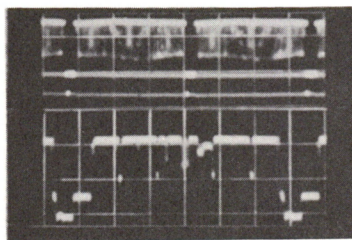
**B. Top: Q5 base, 10 μs/cm, 5v/cm
Bottom: Z1 gray, 10 μs/cm, 5v/cm**



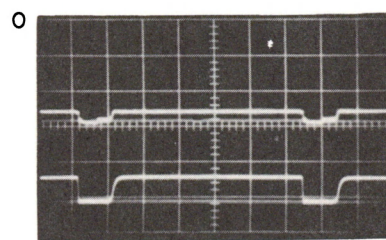
**C. Top: Q5 base, 10 μs/cm, 5v/cm
Bottom: Z1 red, 10 μs/cm, 5v/cm**



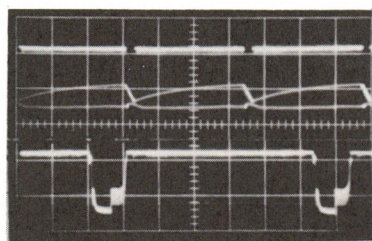
**D. Q5 emitter. Top: 5 ms/cm, 2v/cm.
Bottom: 10 μs/cm, 2v/cm**



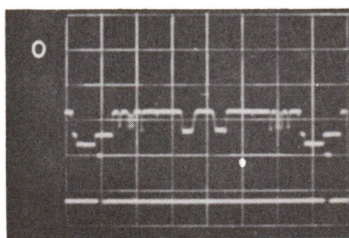
**E. Q6 emitter. Top: 5 ms/cm, 2v/cm.
Bottom: 10 μs/cm, 2v/cm**



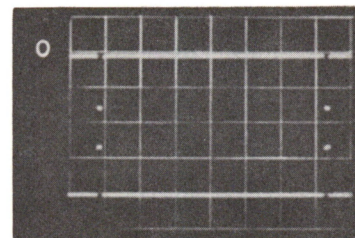
**F. Top: Q7 emitter, 10 μs/cm, 5v/cm
Bottom: Q7 base, 10 μs/cm, 5v/cm**



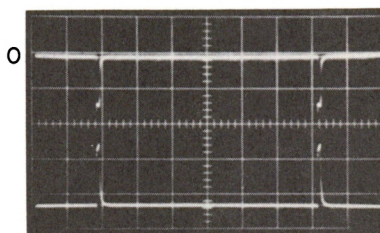
**G. Q7 emitter. Top: 5 ms/cm, 1v/cm.
Bottom: 10 μs/cm, 1v/cm**



**H. Top: Z1 yellow, 10 μs/cm, 5v/cm.
Bottom: Z1 gray, 10 μs/cm, 5v/cm**



**I. Top: Q9 emitter, 10 μs/cm, 5v/cm
Bottom: Q9 collector, 10 μs/cm, 5v/cm**



**J. Top: Q9 base, 10 μs/cm, 5v/cm
Bottom: Q12 base, 10 μs/cm, 5v/cm**

Figure 122—Typical Waveforms; Mono Amplifiers, Blanking Adder and Clamp Pulse Amplifier, and Clipper and Driver Circuits

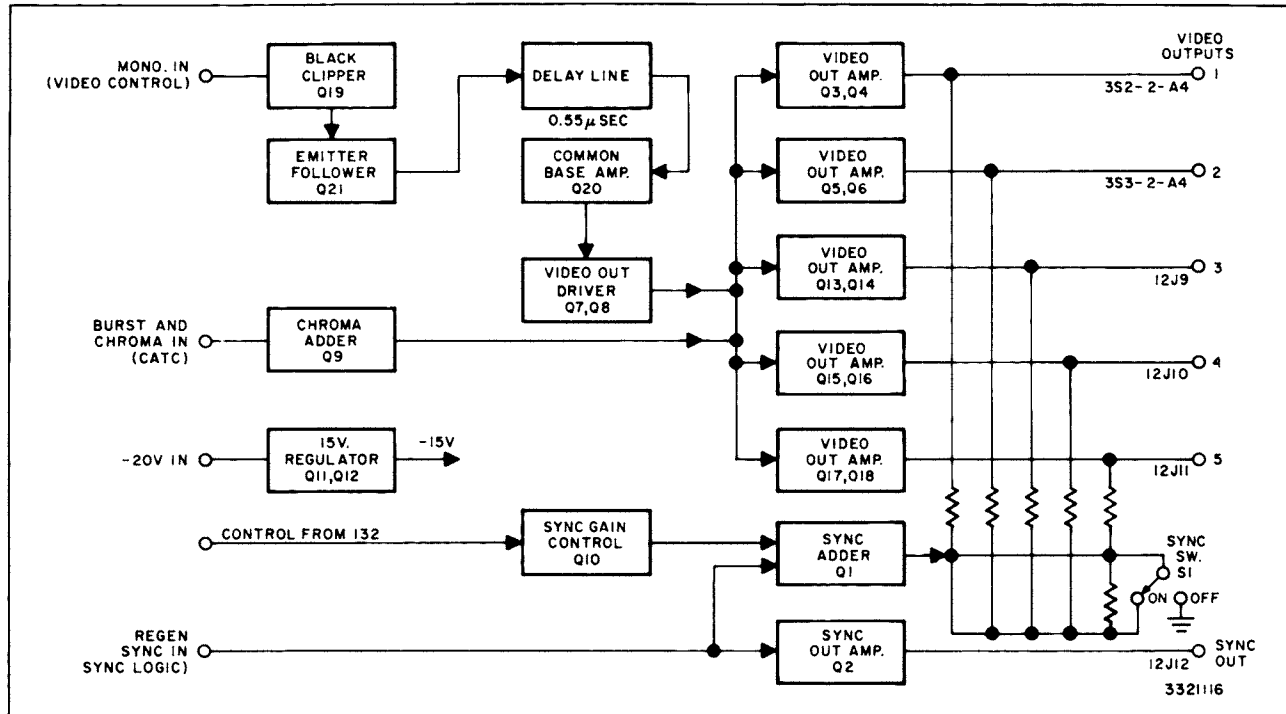


Figure 123—Video Output (Module 233A), Block Diagram

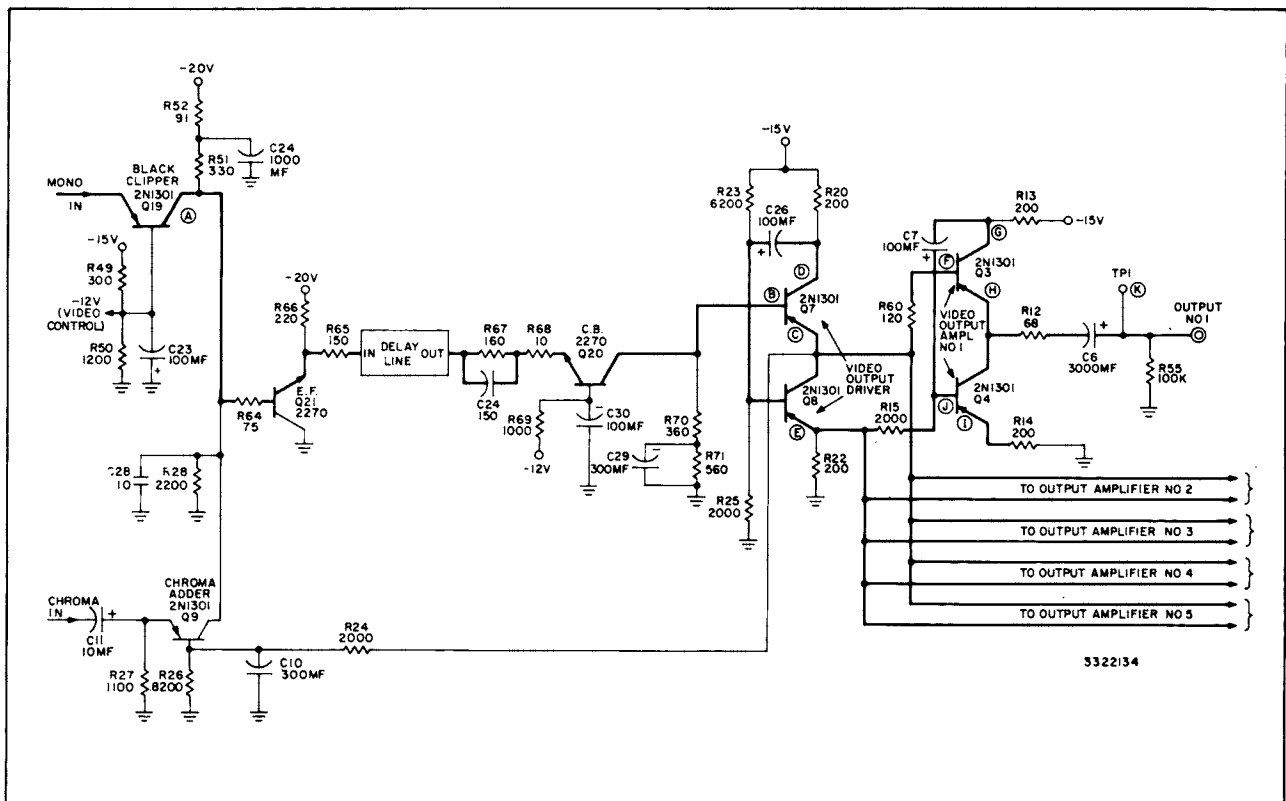


Figure 124—Black Clipper, Delay Line, Video Output Driver, Video Output Amplifier No. 1, and Chroma Adder

A -15 volt regulator stage, consisting of Q11 and Q12, (see figure 128) is used to furnish -15 volts to the series amplifiers. Q12 is the source of the -15 volts. Q11 acts as the bias supply for Q12, supplying all the base current needed by Q12. Q11 holds the bias voltage on the base of Q12 very close to -15 volts over a wide temperature range. Since the base of Q11 is biased at -15 volts, the emitter of Q11 and, consequently, the emitter of Q12 are at essentially the same voltage.

The -12 volts on the base of the black clipper, Q19, is obtained from the -15 volt supply through the voltage divider R49 and R50.

In a color system, Q9 is the burst and chroma adder (see figure 124). It also acts as part of the biasing network for Q7. The feedback loop to the base of Q9 serves as a dc stabilizer to the video output driver stage.

ADJUSTMENTS

Removal of Sync from Video Output No. 5

1. To remove sync, withdraw the Video Output module from the tape recorder. The Sync ON-OFF switch (S1) is located near the front of the board on the right side. Place S1 in the OFF position and replace the module in the tape recorder.

HORIZONTAL AFC (Module 227)

(Refer to Block Diagram Figure 129)

The Horizontal AFC module produces a 31.5-kc pulse (2H), a 15.75-kc horizontal square wave and a horizontal sync pulse for 525-line standards. The 31.5-kc pulse is provided for the Vertical Advance module and the 15.75-kc horizontal square wave for the Sync Logic module. For international standards operation, the counterpart of these pulses, for 405- and 625-line standards, are produced by this module. In contrast to the Horizontal AFC module, the Vertical Advance module and the Sync Logic module are closely tied together in that they trigger each other to achieve a continuous flow of correctly timed pulses.

HORIZONTAL PULSE ADVANCE TECHNIQUE

The sync signal can easily be recovered from the incoming composite video signal; however, the blanking signal, which cannot be removed reliably, must be regenerated from sync. The desired blanking pulse must precede by 1.7 microsecond (nominal front porch width) the sync signal from which it is regenerated. Since sync and blanking are both recurrent

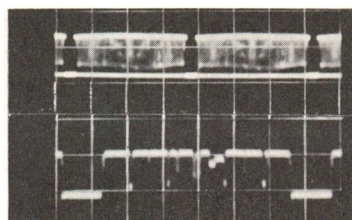
pulses, the position of the next sync pulse from the position of the preceding one may be predicted. Although a simple delay multivibrator with a nominal pulse width of 62.2 microseconds might seem useful to this purpose, its accuracy in pulse width and frequency is inherently inadequate for the application. Even if the tolerance of better than $+0.1\%$ required in the multivibrator to hold the front porch width to within 3% were met, changes in horizontal frequency of only $+1\%$ would reduce the front porch from its nominal 1.7 microseconds to 0.43 microseconds, which is less than half the allowable minimum.

Horizontal pulse advance is obtained through the 2H master oscillator multivibrator, Q1, Q2, for which the frequency and phase is controlled by an automatic phase control circuit referenced to the incoming tape sync. The block diagram, figure 130, illustrates this technique. The feedback loop which controls the phase of the multivibrator contains a 1.7 microsecond delay. The AFC (automatic phase control) loop aligns the two pulses appearing at the phase comparator. However, the multivibrator pulse is delayed by 1.7 microseconds before reaching the comparator through Q14 and Q15. The delayed pulse is lined up with the pulses generated from reference sync. Thus, the undelayed multivibrator pulse precedes sync by 1.7 microseconds and is properly timed to regenerate horizontal blanking. In this system, the feedback loop tracks any changes in horizontal frequency, eliminating variations in front porch width due to frequency changes; also, a one percent change in delay causes only one percent change in front porch width.

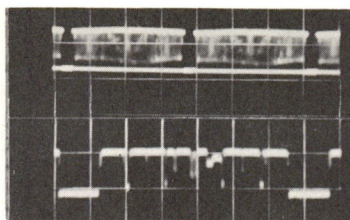
2H Master Oscillator and Start Circuit

The master oscillator is an astable multivibrator used to produce a square wave. The free running frequency of the master oscillator, as shown in figure 131, is determined by the charging time of capacitors C28 and C29 through resistors R32, R33 and R2-R65.* An afc current from the afc current amplifier, Q106, added to the charging current, corrects the frequency and phase of the master oscillator with respect to incoming sync. The frequency is set to approximately 31.5 kc by the 2H FREQ control, R2, using a fixed value of afc current. This fixed afc current is obtained by pressing the SET-RUN switch, S1, (figure 137) to the SET position. From the collector of Q1, the 31.5 kc square wave goes to the Vertical Advance module and also to the 2H trigger amplifier, Q8, where it is coupled to the base by capacitor C14.

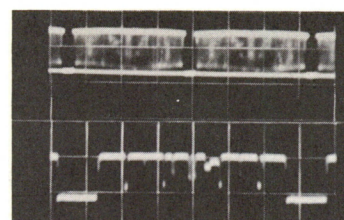
*Assuming 525 line standards.



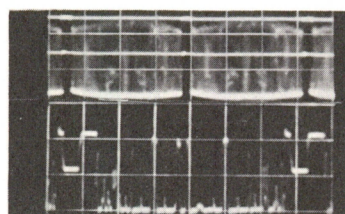
A. Q19 collector
Top: 5 ms/cm, 1v/cm
Bottom: 10 μ s/cm, 1v/cm



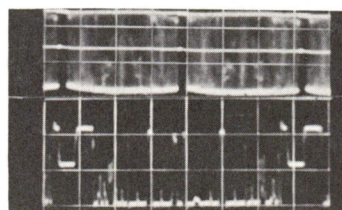
B. Q7 base
Top: 5 ms/cm, 1v/cm
Bottom: 10 μ s/cm, 1v/cm



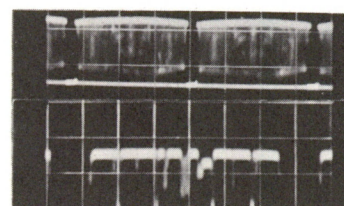
C. Q7 emitter
Top: 5 ms/cm, 1v/cm
Bottom: 10 μ s/cm, 1v/cm



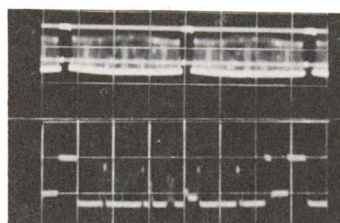
D. Q7 collector
Top: 5 ms/cm, 1v/cm
Bottom: 10 μ s/cm, 1v/cm



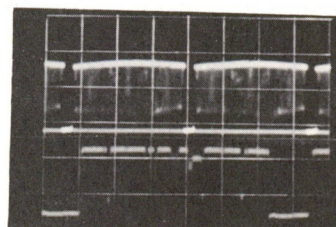
E. Q8 emitter
Top: 5 ms/cm, 1v/cm
Bottom: 10 μ s/cm, 1v/cm



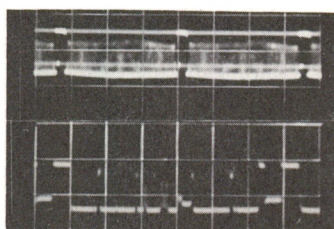
F. Q3 base
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



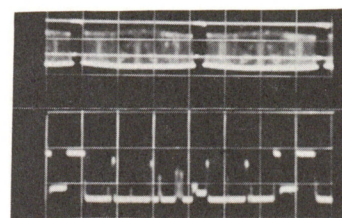
G. Q3 collector
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



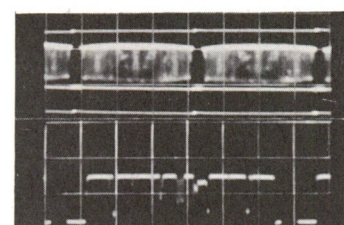
H. Q3 emitter
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



I. Q4 emitter
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



J. Q4 base
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm



K. TP1
Top: 5 ms/cm, .5v/cm
Bottom: 10 μ s/cm, .5v/cm

Figure 125—Typical Waveforms; Black Clipper, Video Output Driver, Video Output Amplifier No. 1, and Chroma Adder Circuits

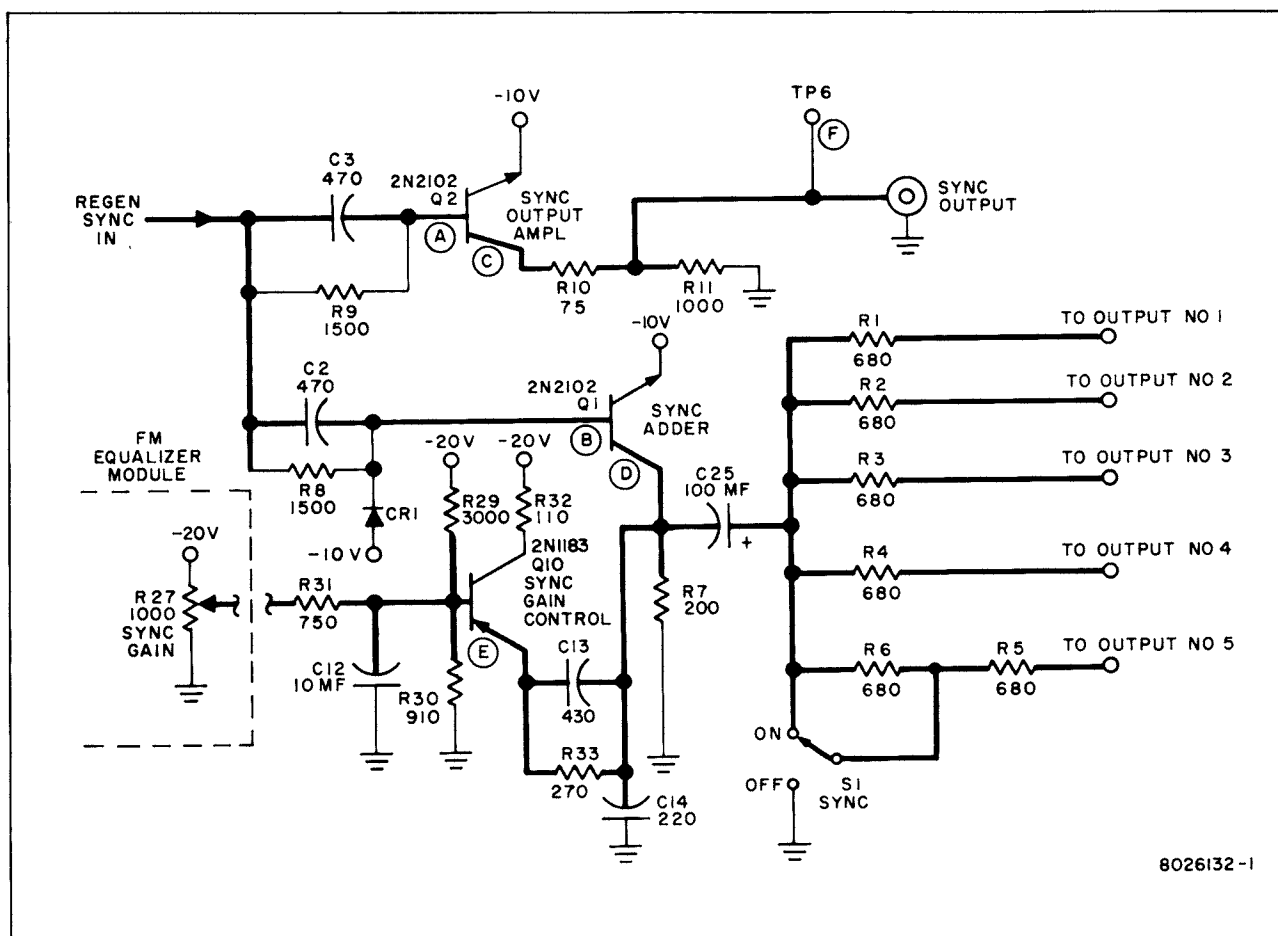


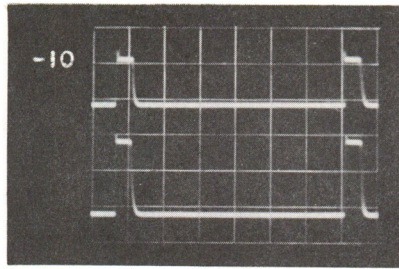
Figure 126—Sync Gain, Sync Adder, and Sync Output Amplifier Circuits

To provide a 15.75-kc square wave (half the 31.5-kc pulse) which is properly timed for the generation of horizontal blanking and horizontal drive in the Sync Logic module, the divide-by-two monostable multivibrator, Q9, Q10, is triggered from the trigger amplifier, Q8.

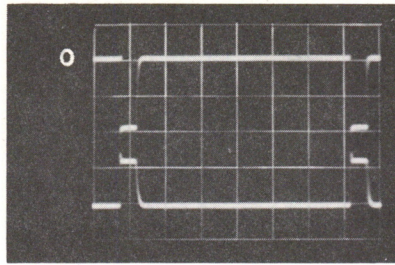
Refer to figure 133. A requirement for the Horizontal AFC module to switch to international standards requires new time constant components and switching systems for the HN and HI busses, along with a two-transistor starting circuit for the 2H master oscillator.

The starting circuit, Q18 and Q19, insures that the 2H master oscillator keeps running at all times. This circuit prevents a situation from arising that could lead to both transistors of the 2H master oscillator being saturated at the same time. Were such a condition to occur, even for an instant, the collectors of both Q1 and Q2 would assume the same potential as that of their emitters, approximately -10 volts, and the 2H master oscillator would remain at rest, generating no output.

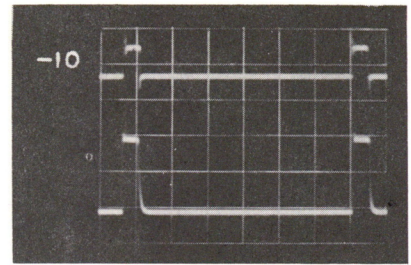
The start circuit transistors are turned on and off alternately by means of the biasing arrangement employed. The voltage at the junction of R4 and R7 cannot be more negative than -10 volts. Therefore, the voltage developed across the divider network consisting of R63, R81 and the parallel combination of R4 and R7 provides a bias on the base of Q18 that is more positive than the -10 volts on the emitter and thus cuts off this transistor. The bias voltage on the base of Q19 is developed across the voltage divider consisting of R67, R66, and R82. This voltage is more negative than that on the emitter of Q19, therefore this transistor is driven into saturation and virtually the full potential on the emitter (-10 volts) appears on the collector. The voltage on the collector of Q19 is applied across R32 and R33 to the bases of Q1 and Q2, respectively. Since there is -10 volts on the emitters of Q1 and Q2 already, the -10 volts on the bases of Q1 and Q2 causes them to become reverse biased. In this state, assuming perfect equilibrium between Q1 and Q2, no current will flow in the emitter-base circuit of either transistor, therefore both will be cut off. However, since there is inherently some un-



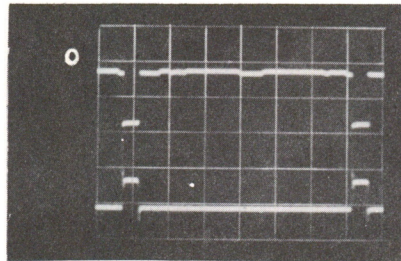
**A. Top: Q2 base, 10 μ s/cm,
5v/cm
Bottom: C3 input, 10 μ s/cm,
5v/cm**



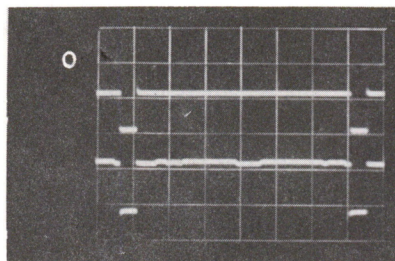
**B. Top: Q1 base, 10 μ s/cm,
1v/cm
Bottom: C3 input, 10 μ s/cm,
5v/cm**



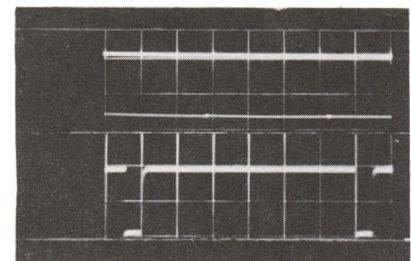
**C. Top: Q2 collector, 10 μ s/cm,
5v/cm
Bottom: Q2 base, 10 μ s/cm,
5v/cm**



**D. Top: Q1 collector, 10 μ s/cm,
5v/cm
Bottom: Q1 base, 10 μ s/cm,
1v/cm**



**E. Top: Q10 emitter, 10 μ s/cm,
5v/cm
Bottom: Q1 collector,
10 μ s/cm, 5v/cm**



**F. TP6
Top: 500 μ s/cm, 5v/cm
Bottom: 10 μ s/cm, 5v/cm**

Figure 127—Typical Waveforms; Sync Gain, Sync Adder, and Sync Output Amplifier Circuits

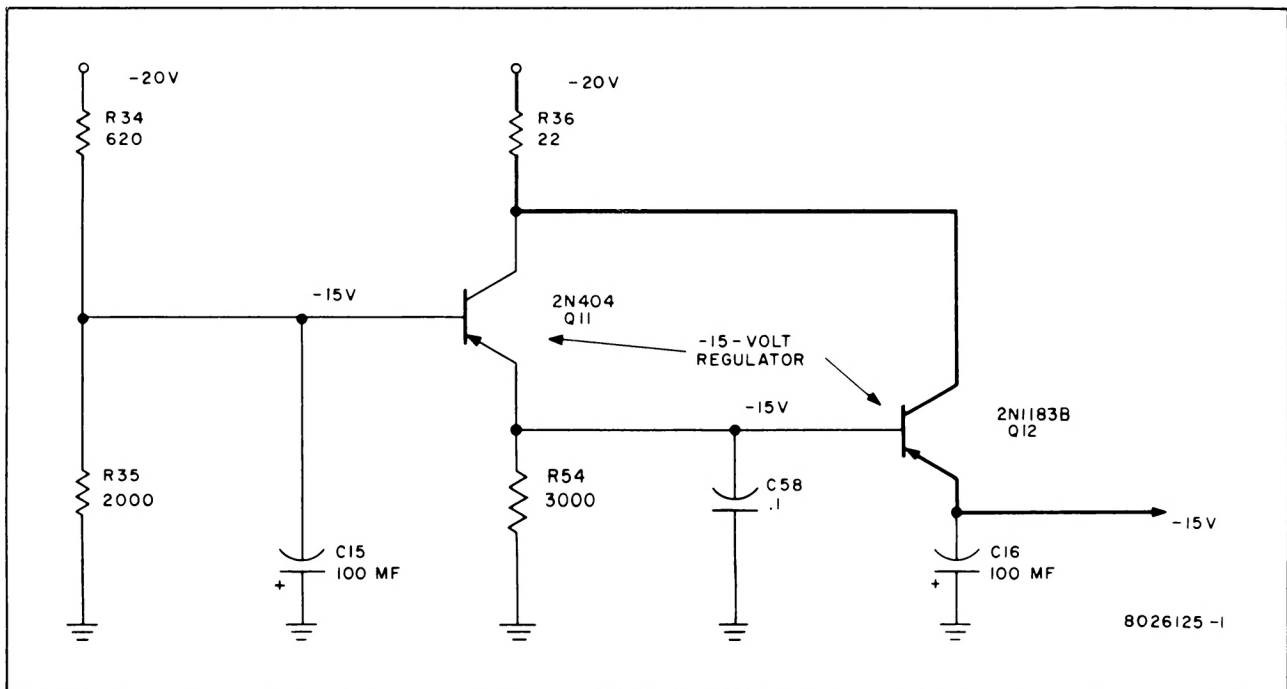


Figure 128—-15 Volt Regulator Circuit

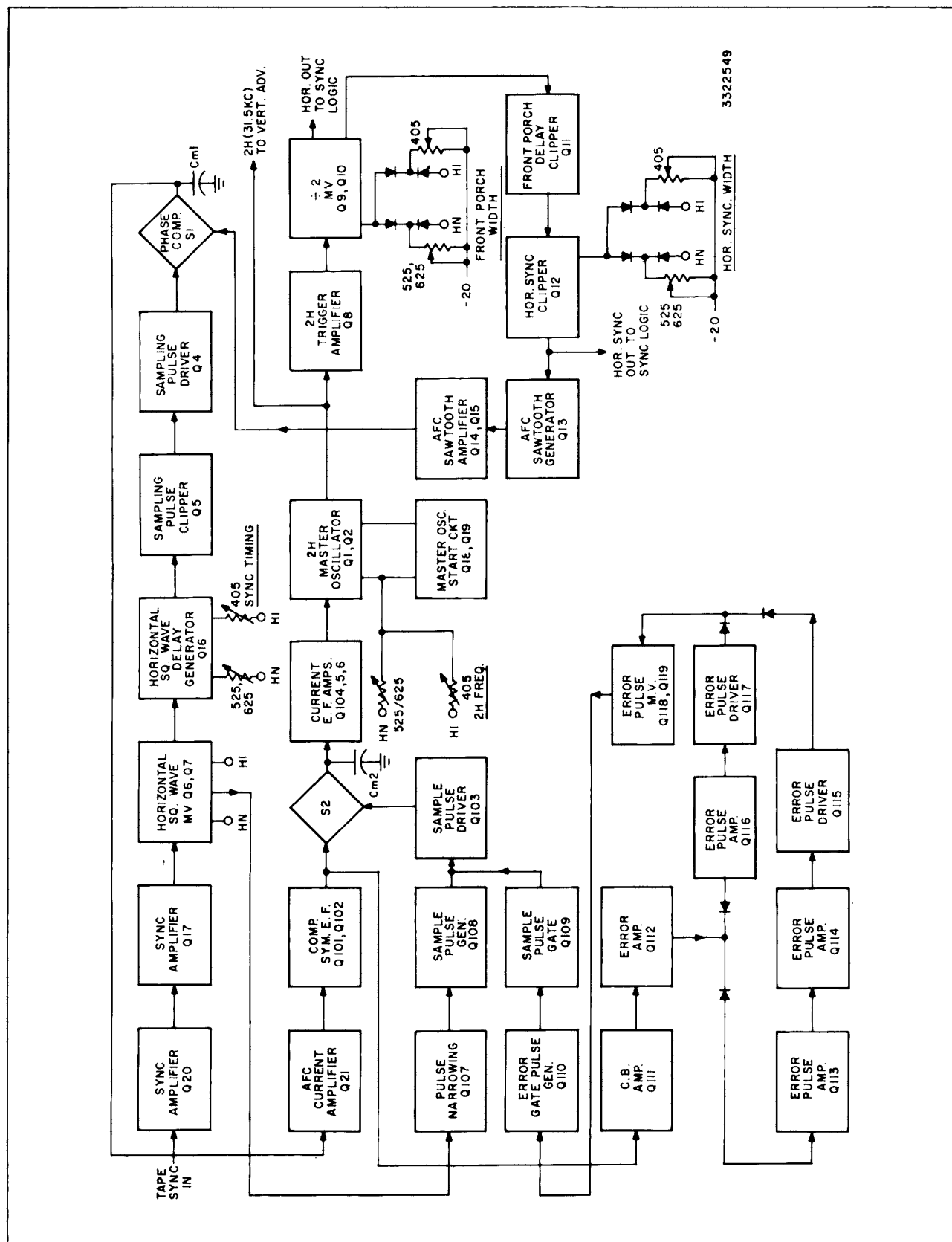


Figure 129—Block Diagram, Horizontal AFC Module

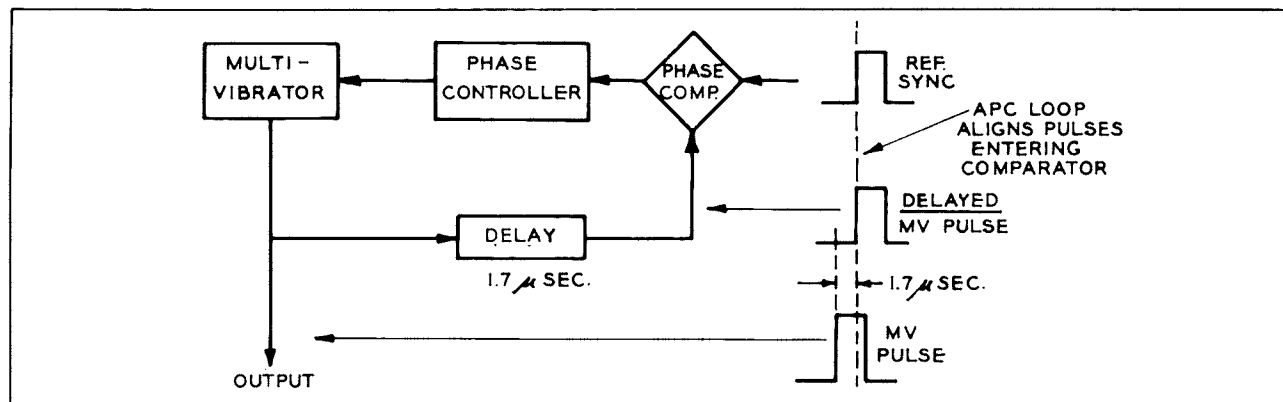


Figure 130—Block Diagram of Pulse Advance Circuit

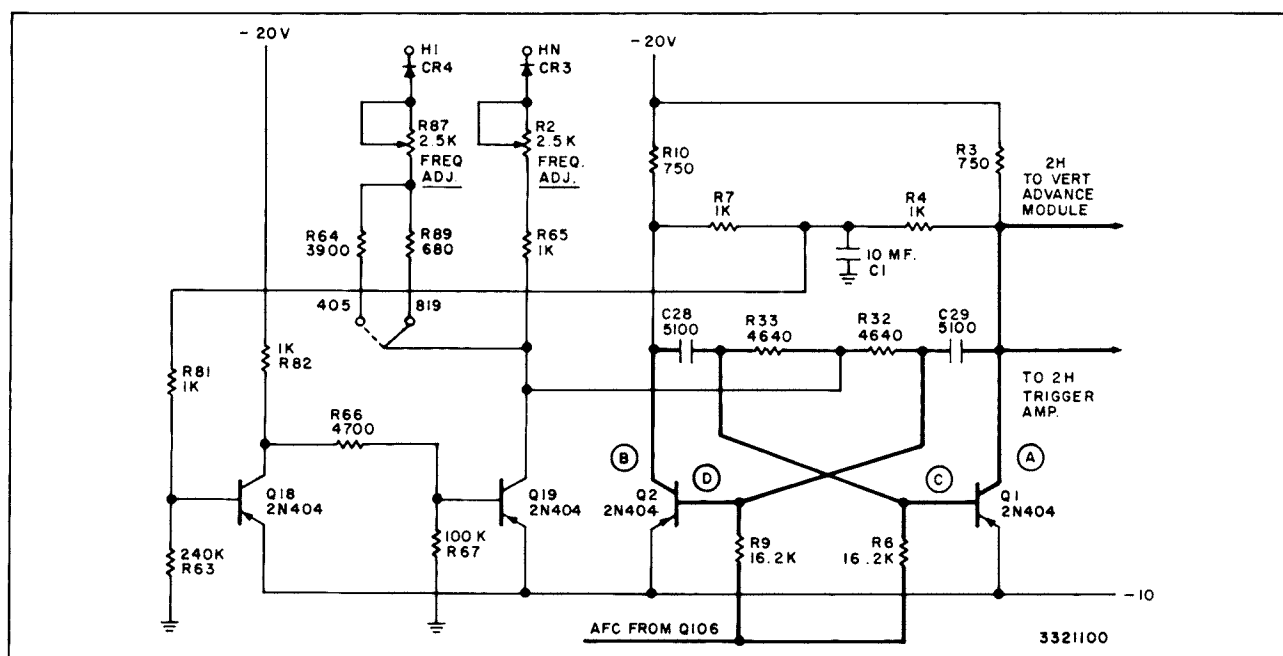


Figure 131—2H Master Oscillator

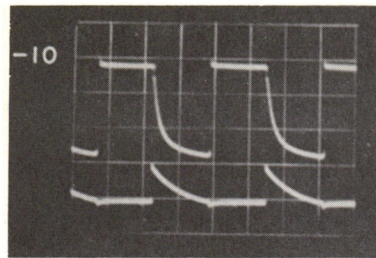
balance between the components of each half of the multivibrator, one side of the 2H master oscillator will begin to conduct before the other. Thus one transistor is driven into saturation and the other is cut off.

At the same time, the states of Q18 and Q19 are reversed. Now Q19 is cut off, and current from the HI or HN bus is allowed to flow into the base of the saturated transistor. Transistor Q18 is turned on by the bias on the base, which is now more negative than the voltage on the emitter. The bias is obtained from the -20 volt supply and is developed across the divider network formed by R63, R81, and the 1000 and the 750 ohm resistors in the collector circuit of the transistor that is cut off.

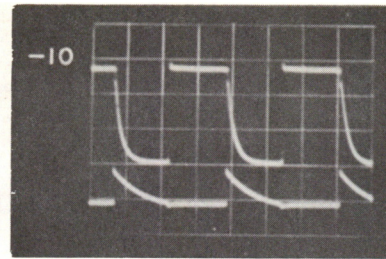
The time constant components are the same for both 525- and 625-line standards. For 405- or 819-line standards, different time constant components are switched into the circuits by means of the HN and HI busses. The TV STANDARDS switch used to select the desired line standard is located on the front panel of the Vertical Advance (module 228A). On 525- and 625-line standards, the HN bus is at -20 volts and the isolation diodes in the related time constant circuits are forward biased. Conversely, the HI bus is at ground potential and the isolation diodes associated with time constant components connected to this bus are reverse biased or cut off.

NOTE

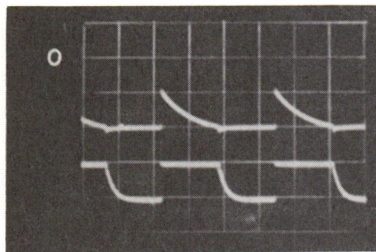
New time constants are switched into the circuits of the following stages on 405- or 819-line standards for the reasons stated:



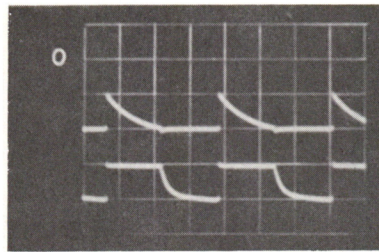
**A. Top: Q1 collector, 10 μ s/cm, 2v/cm
Bottom: Q1 base, 10 μ s/cm, 5v/cm**



**B. Top: Q2 collector, 10 μ s/cm, 2v/cm
Bottom: Q2 base, 10 μ s/cm, 5v/cm**



**C. Top: Q1 base, 10 μ s/cm, 5v/cm
Bottom: Q2 collector, 10 μ s/cm, 5v/cm**



**D. Top: Q2 base, 10 μ s/cm, 5v/cm
Bottom: Q1 collector, 10 μ s/cm, 5v/cm**

Figure 132—Typical Waveforms, 2H Master Oscillator (525 lines)

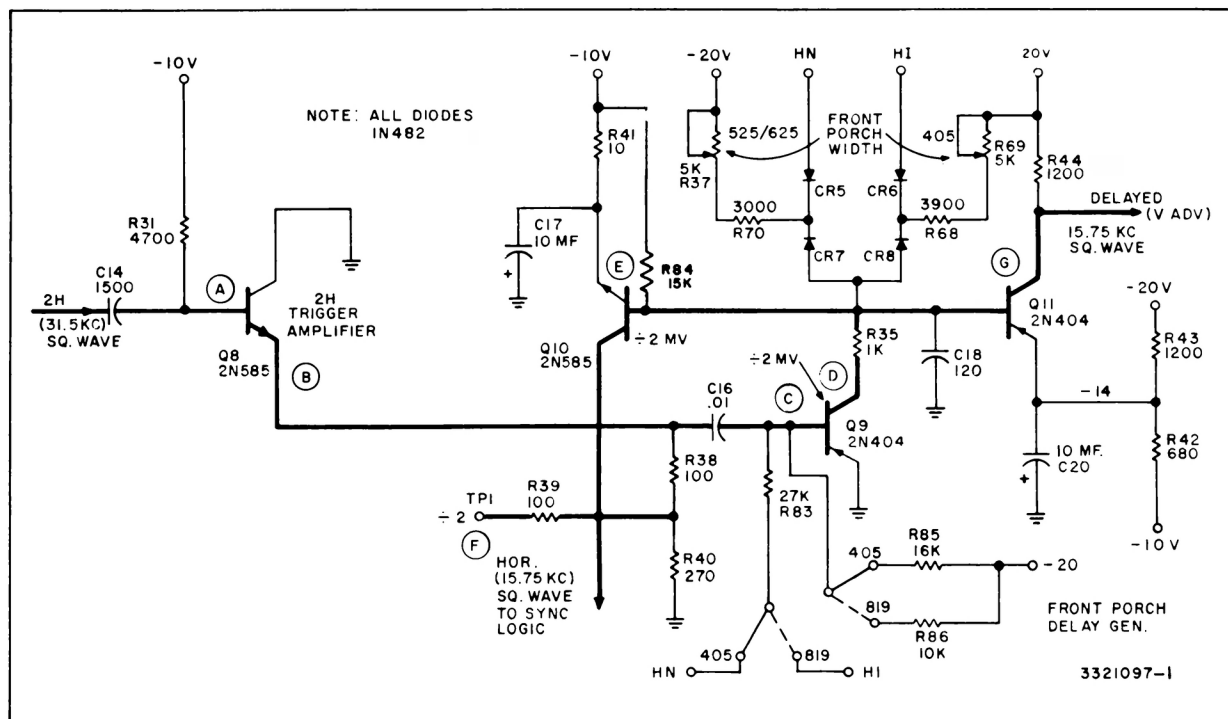


Figure 133—2H Trigger Amplifier $\div$ 2 Multivibrator and Front Porch Delay Clipper Circuits

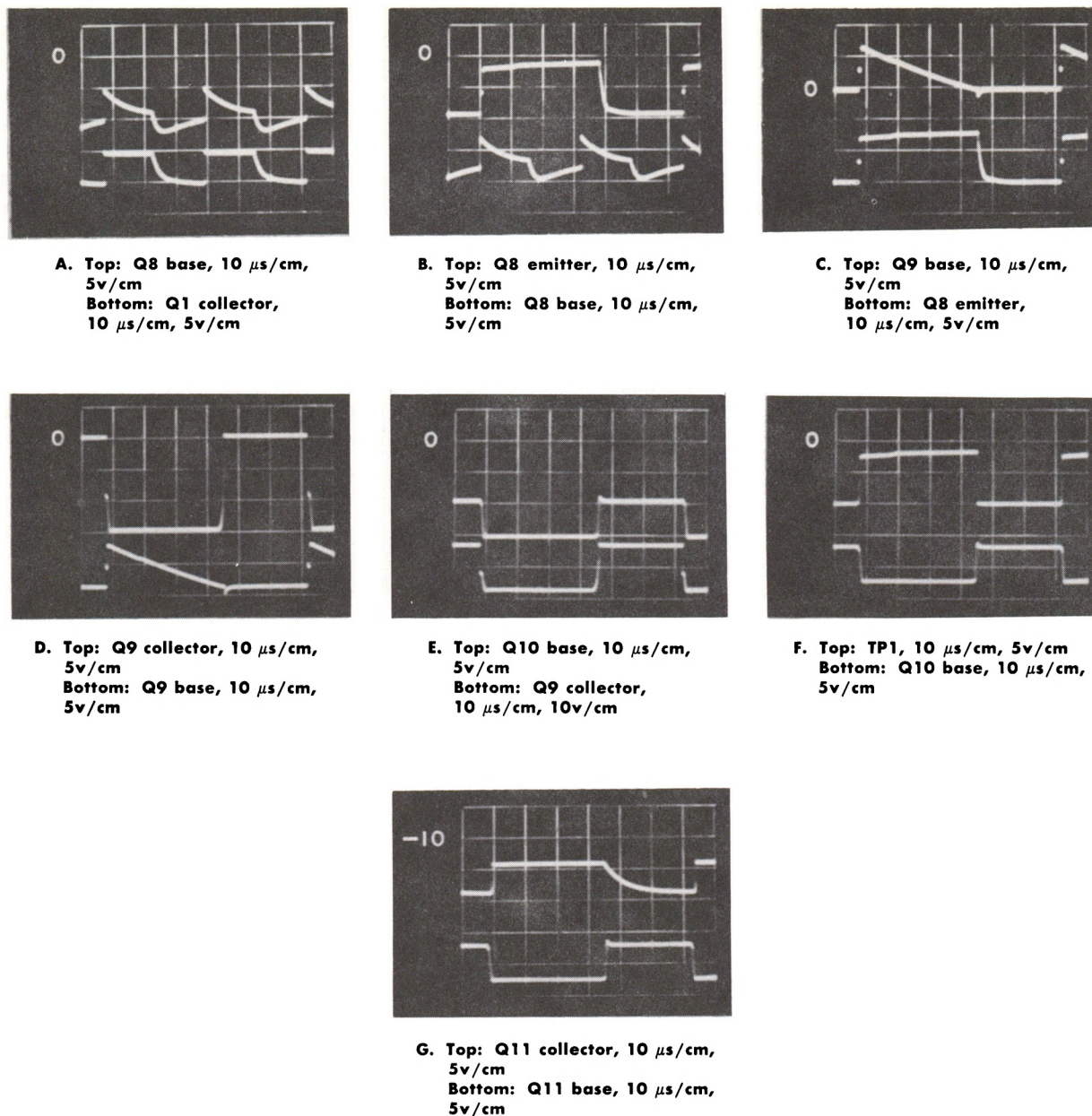


Figure 134—Typical Waveforms; 2H Trigger Amplifier $\div 2$ Multivibrator and Front Porch Delay Clipper Circuits

1. Horizontal Square Wave Multivibrator (Q6, Q7) for setting the horizontal frequency to the proper duty cycle.

2. $\div 2$ Multivibrator (Q9, Q10) for proper timing of the front porch interval.

3. Horizontal Sync Clipper (C12) for setting the width of regenerated sync.

4. Horizontal Square Wave Delay Generator (Q16) for correct timing of regenerated sync with respect to reference sync.

Both transistors of the $\div 2$ multivibrator (refer to figure 133) are saturated in the stable state and

driven to cutoff by a positive trigger pulse from Q8. The time constant of C16, R83 and R85, determines the duration of the cutoff period which is slightly greater than the period of the 31.5-kc trigger pulse. Both transistors then revert to the saturated state until the next trigger pulse comes along.

A gating action is accomplished by dc connecting the emitter of Q8 through R38 to the collector of Q10. (Refer to figure 133.) When Q10 is in the saturated or stable state, the Q10 collector and Q8 emit-

ter are at -10v . Since the collector of Q8 is at zero potential, the transistor is capable of passing a trigger pulse applied to its base. The output from the emitter of Q8 is a positive going trigger pulse that is applied through C16 to the base of Q9. This pulse cuts off Q9 which simultaneously cuts off Q10. When Q10 is cut off, the voltage at its collector and at the emitter of Q8 rises to 0 volts making it impossible for Q8 to pass trigger pulses, since the trigger pulses on the base of Q8 do not exceed 0 volts in the positive direction. Amplifier Q8 is biased so that it does not pass the negative going pulses applied to the base.

A 15.75-kc square wave from the collector of Q9 is fed to the base of the front porch delay clipper, Q11. The shunt capacitor, C18, at the base of Q11 slows down the rise time of the square wave. Transistor Q11 does not conduct until the potential in the base falls to approximately the fixed emitter potential (-14v) formed by voltage divider R42, R43. The time taken to reach this potential is the delay time. In conduction, the Q11 circuit produces, at the collector, a fast-rise-time square wave whose leading edge is delayed from that of the input square wave. The delay in the conduction of Q11 is determined by the rise time of the input square wave, which is controlled by the setting of the FRONT PORCH WIDTH potentiometer, R37.

Regenerated Sync and AFC Sawtooth

As shown in figure 135, this delayed 15.75-kc square wave output is coupled to the base of Q12, the horizontal sync clipper, which is a pulse narrowing circuit. The width of the pulse is determined by the time constant of C19, R74, R75, R72 and R45, the last being the HOR SYNC WIDTH potentiometer. Regenerated horizontal sync for the Sync Logic module is taken from the collector of Q12.

The horizontal sync pulse is also coupled to the base of the afc sawtooth generator, Q13. The integrating network of R48 and C15 slows the rise time of the sync pulse enough to permit a slight delay in the time of conduction for Q13. This delay contributes to the total advance in timing of the 31.5-kc square wave relative to tape sync; however, it does not affect the front porch width since that width is determined only by the delay between the 15.75-kc square wave (used to generate horizontal blanking) and the leading edge of regenerated horizontal sync. The SYNC TIMING control, R56, allows adjustment of the total delay of horizontal sync over a small range so that the leading edge of regenerated horizontal sync may be made coincident with the leading

edge of incoming tape sync. Therefore, when regenerated horizontal sync is combined with the vertical interval of tape sync in the Sync Logic module, the equalizing pulses and the vertical sync pulses are correctly timed with respect to the horizontal sync pulses.

The afc sawtooth generator, Q13, conducts when the integrated sync pulse on its base drops to approximately the voltage (-4v) on the emitter, which is fixed by voltage divider R49, R50 and R91. When Q13 conducts, it provides a low impedance discharge path for capacitor C25. Then, when Q13 is cut off by the decay of the input sync pulse, C25 charges slowly through R52 and R53, generating a sawtooth voltage. The sawtooth voltage at the collector is direct-coupled to the bases of the sawtooth or complementary symmetry (bootstrap) amplifier, Q14 and Q15. This bootstrap circuit increases the linearity of the sawtooth waveform; the complementary symmetry arrangement provides sufficient current gain and a very low impedance to drive the phase comparator (figure 137). The output is taken from the emitters of Q14 and Q15.

During the vertical interval, equalizing pulses and vertical sync serrations occur at twice the rate (31.5 kc) of the horizontal sync pulses. If this "double frequency" (half-line) information is permitted to trigger the sampling pulse clipper, Q5, (figure 137) the phase comparator would be keyed on during the wrong part of the sawtooth voltage cycle and thus provide wrong afc information to the 2H master oscillator. The circuitry as shown in figure 139 provides only 15.75-kc pulses for the sampling pulse clipper, Q5. Tape sync is fed to Q20, the first sync amplifier, an emitter follower used for isolation, with essentially unity gain. This couples to Q17 which in conjunction with C31 and R60 differentiates and amplifies the negative sync signal. The amplified differentiated sync signal appears on the collector of Q17. The leading edge of sync or negative pulse triggers the horizontal square wave multivibrator, Q6, Q7. The time constant of the multivibrator is such that the triggering is effective only at the horizontal frequency rate of composite sync. Q6, Q7 is designed as a monostable multivibrator.

With no signal, Q7 is normally in its stable or cut-off state, and Q6 is in its stable or saturation state. The collector of Q7 is nominally at -10 volts and that of Q6 is 0 volts. The negative sync pulse from the collector of Q17 forward biases Q7. This drives Q7 into saturation thereby generating a positive pulse on the collector. This positive pulse is applied to the base of Q6 through R25 and C11. With the positive

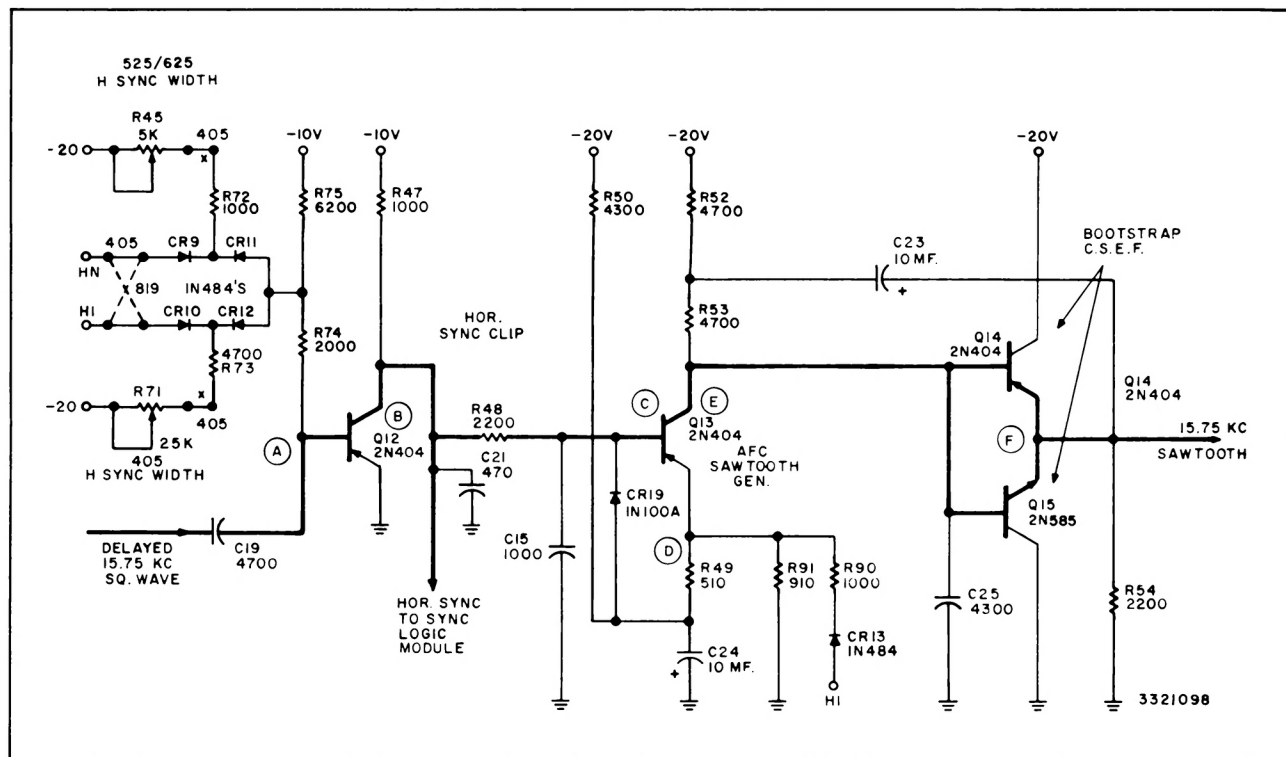


Figure 135—Horizontal Sync Clipper, AFC Sawtooth Generator and Complementary Symmetry Circuits

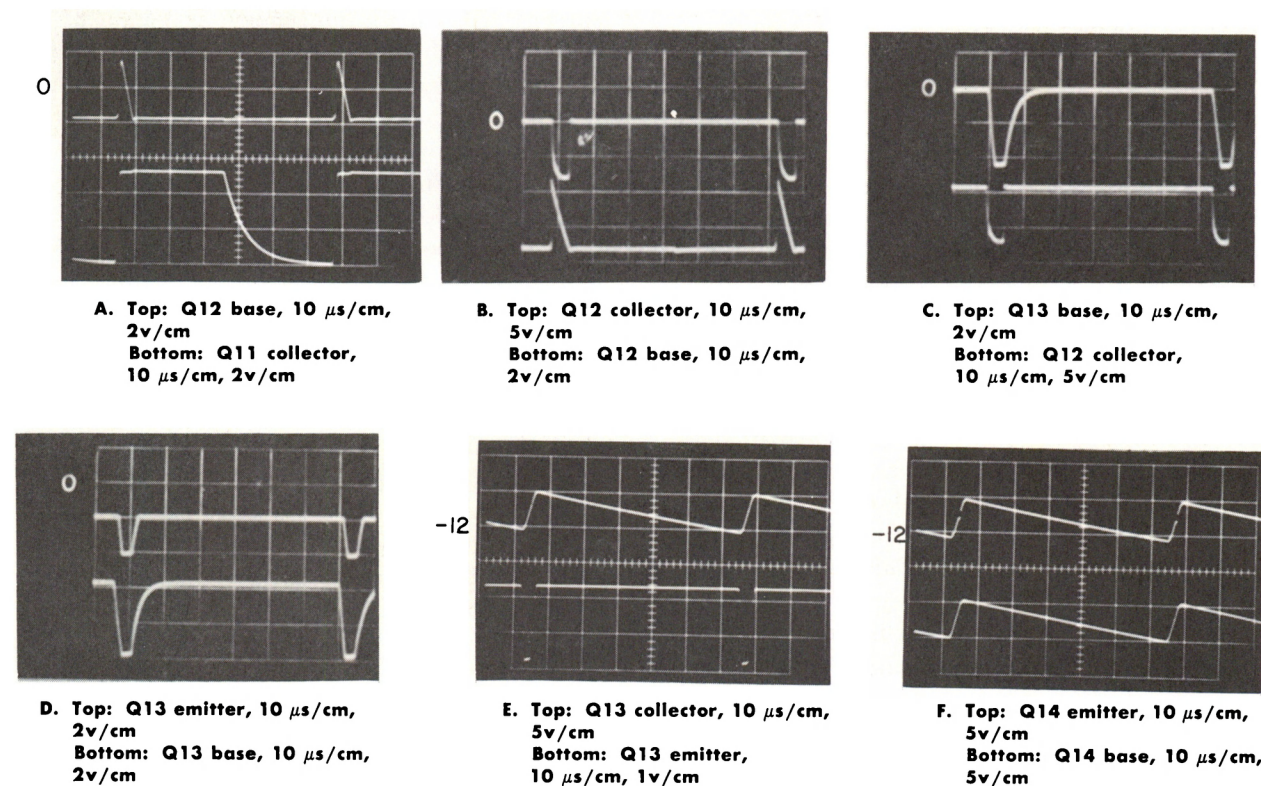


Figure 136—Typical Waveforms; Horizontal Sync Clipper, AFC Sawtooth Generator and Complementary Symmetry Circuits

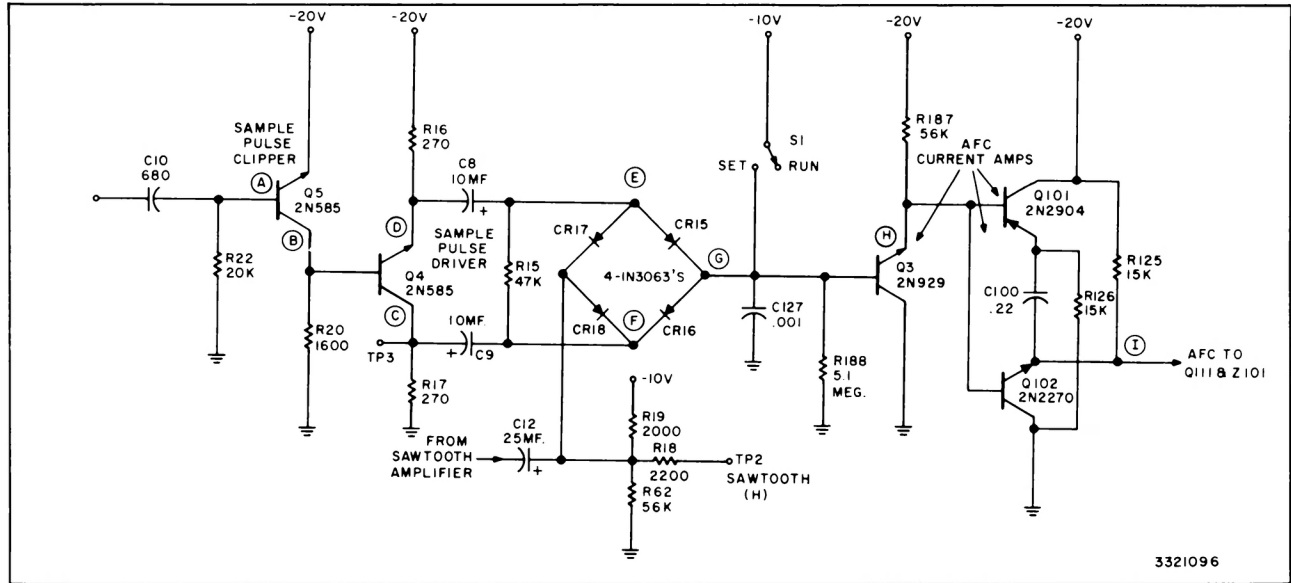


Figure 137—Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier Circuits

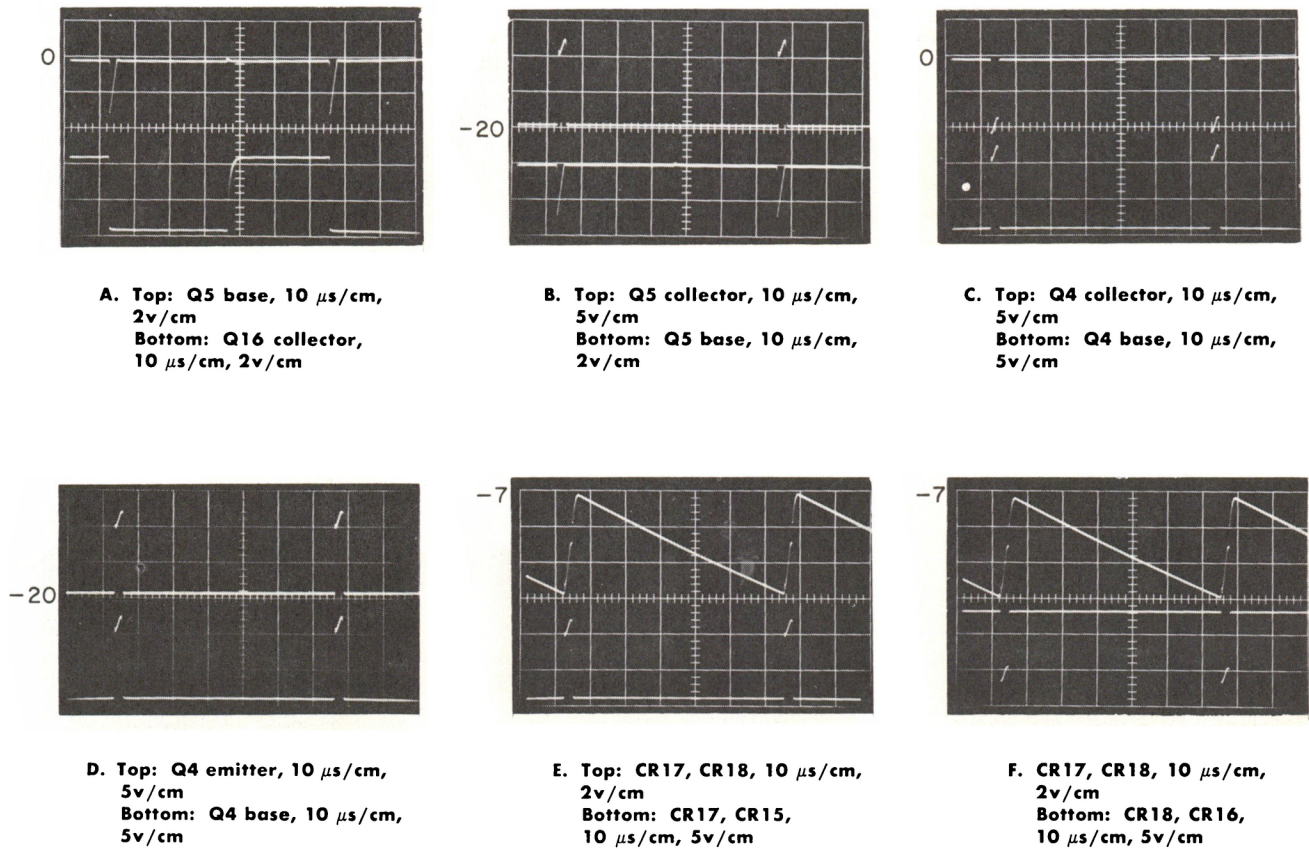


Figure 138—Typical Waveforms; Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier Circuits

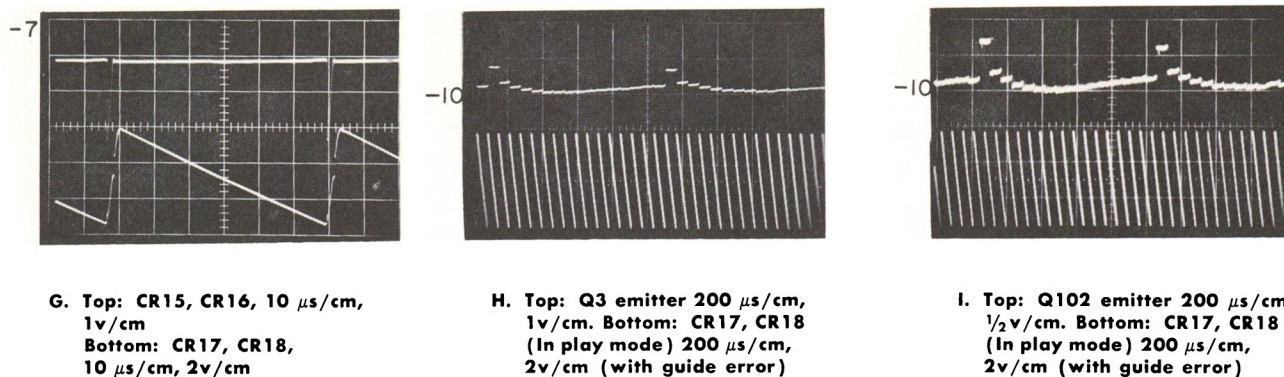


Figure 138—Typical Waveforms; Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier Circuits (Continued)

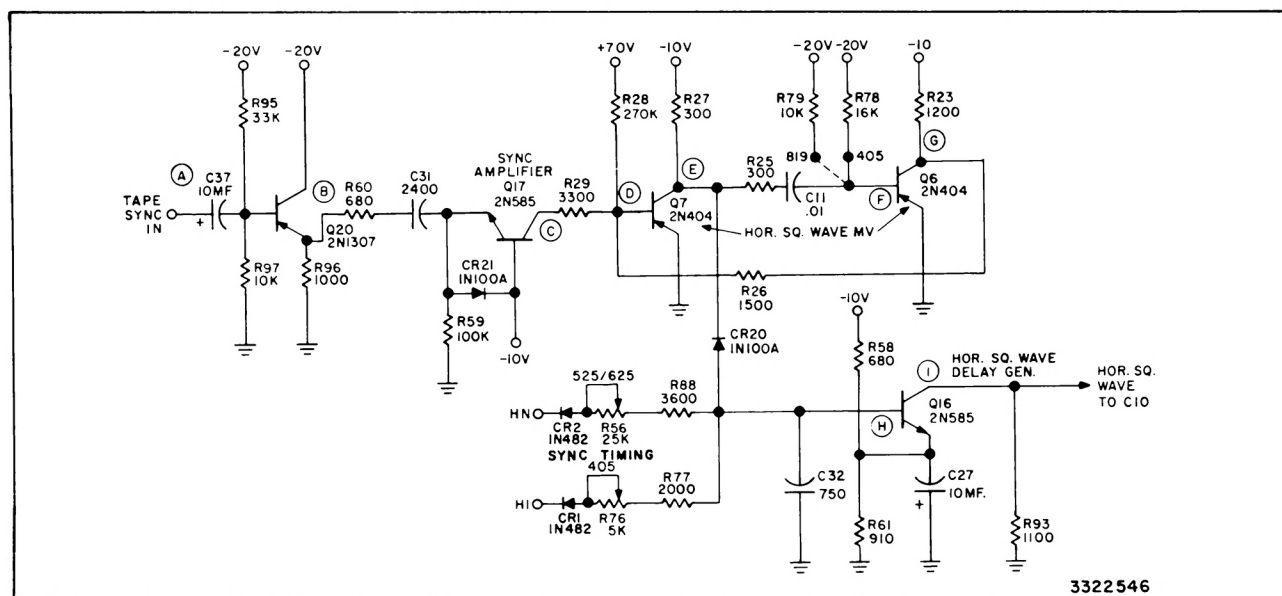


Figure 139—Sync Amplifiers, Horizontal Square Wave Multivibrator and Horizontal Square Wave Delay Generator Circuits

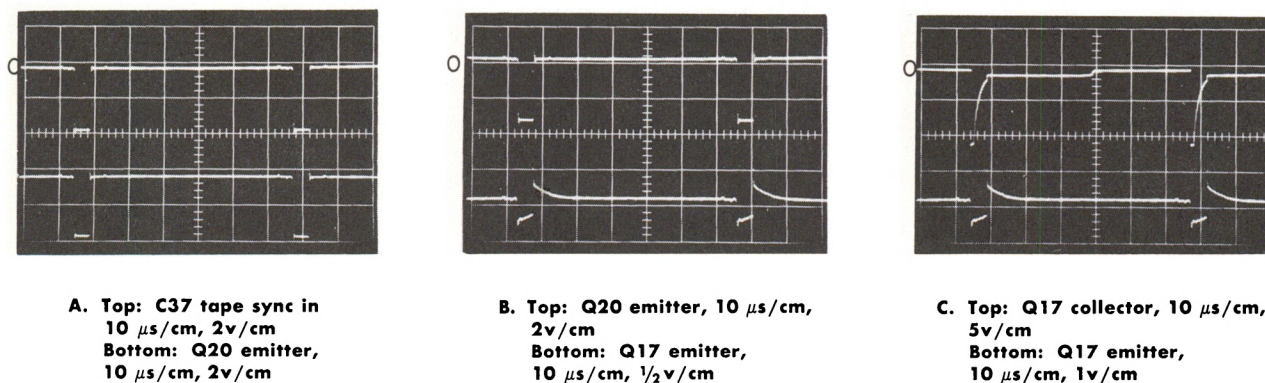


Figure 140—Typical Waveforms; Sync Amplifiers, Horizontal Square Wave Multivibrator and Horizontal Square Wave Delay Generator Circuits

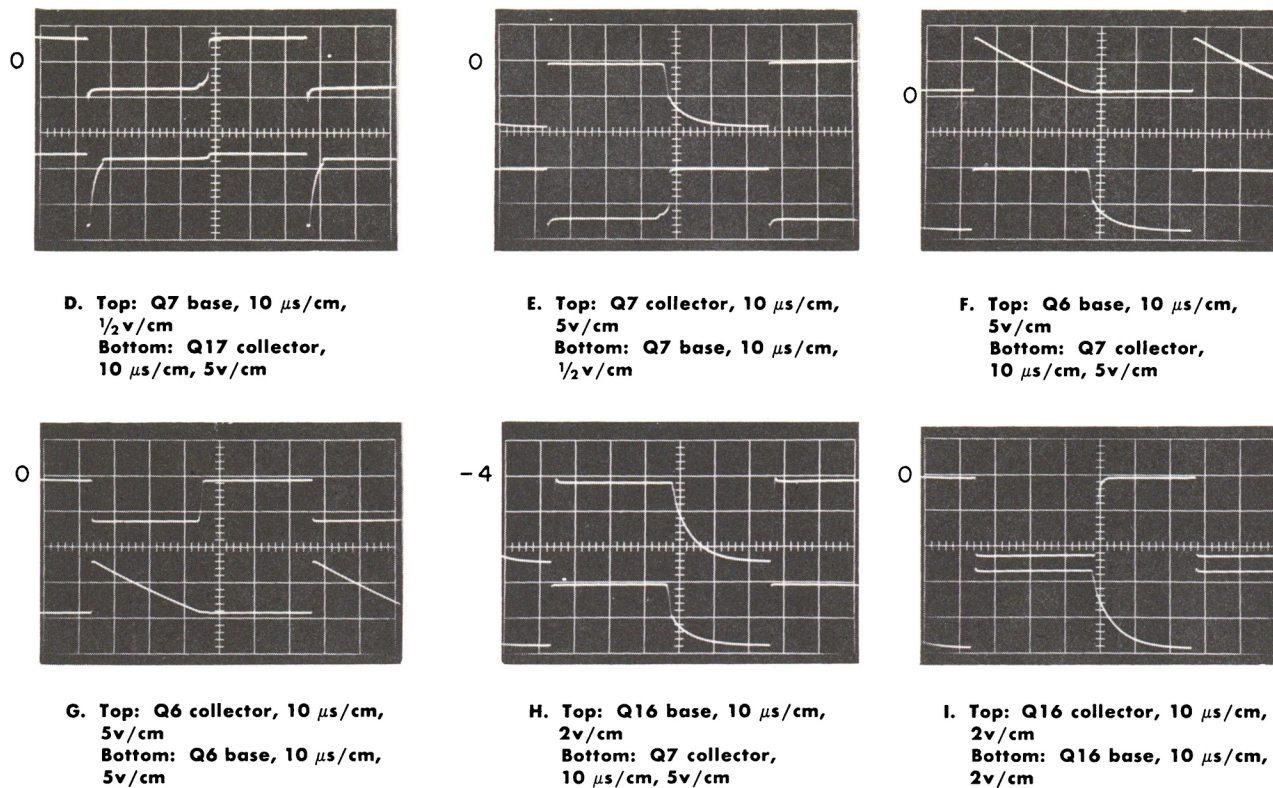


Figure 140—Typical Waveforms; Sync Amplifiers, Horizontal Square Wave Multivibrator and Horizontal Square Wave Delay Generator Circuits (Continued)

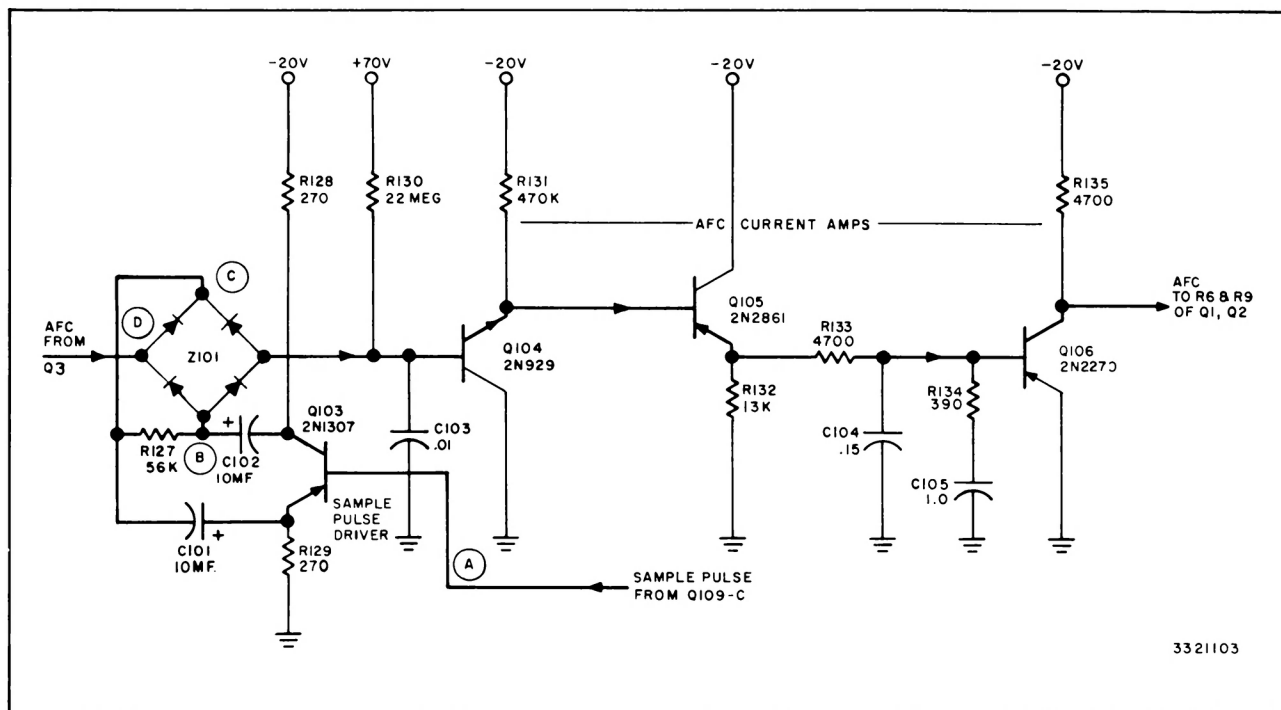


Figure 141—AFC Current Amplifiers

pulse on its base, Q6 is cut off. C11 is charged to -10 volts through R27 and R25 and the base-emitter junction of Q6 during the quiescent state of Q7. C11 discharges through R78, R25 and the saturation resistance of Q7. The voltage on the base of Q6 becomes less positive and Q6 begins to conduct. As Q6 goes toward saturation, the voltage on the collector decreases negatively, and is coupled through R26 to the base of Q7, driving it into cutoff.

By applying a succession of negative pulses to the base of Q7, the multivibrator generates a train of positive sync pulses or horizontal square waves at the collector of Q7. The width or frequency of the horizontal square waves is determined by the time constant of R25, C11, and R78. Through the use of the horizontal square wave multivibrator, any half line (31.5 kc) information during vertical blanking is eliminated.

The positive-going square wave from the collector of Q7 is direct-coupled to the base of Q16, the horizontal square wave delay generator. The capacitor, C26, on the base of Q16 delays the square wave. The amount of delay can be varied by the SYNC TIMING

control, R56. (Refer to *Adjustment Procedures* for this module.)

NOTE

The composite video output signal can be observed by connecting an oscilloscope to any one of the five test points on the Video Output module. In the same manner, the sync on the video input signal can be observed at test point one on the Video Control module.

The emitter of Q16 is set to a small negative voltage ($-2v$) at which level the signal into the base is being clipped. Q16 also inverts the signal. When this inversion takes place, the positive-going pulse in the collector is limited at zero volts, so that there is a 2-volt square wave appearing on the collector. This signal drives the differentiating network C10 and R22.

As shown in figure 137, the 15.75-kc signal from the collector of Q16 is coupled through the timing capacitor, C10, to the sampling pulse clipper, Q5. Transistor Q5 is a boxcar circuit which generates a narrow pulse; the leading edge of this pulse corresponds in time to the leading edge of sync. The positive-going portion of the differentiated signal is

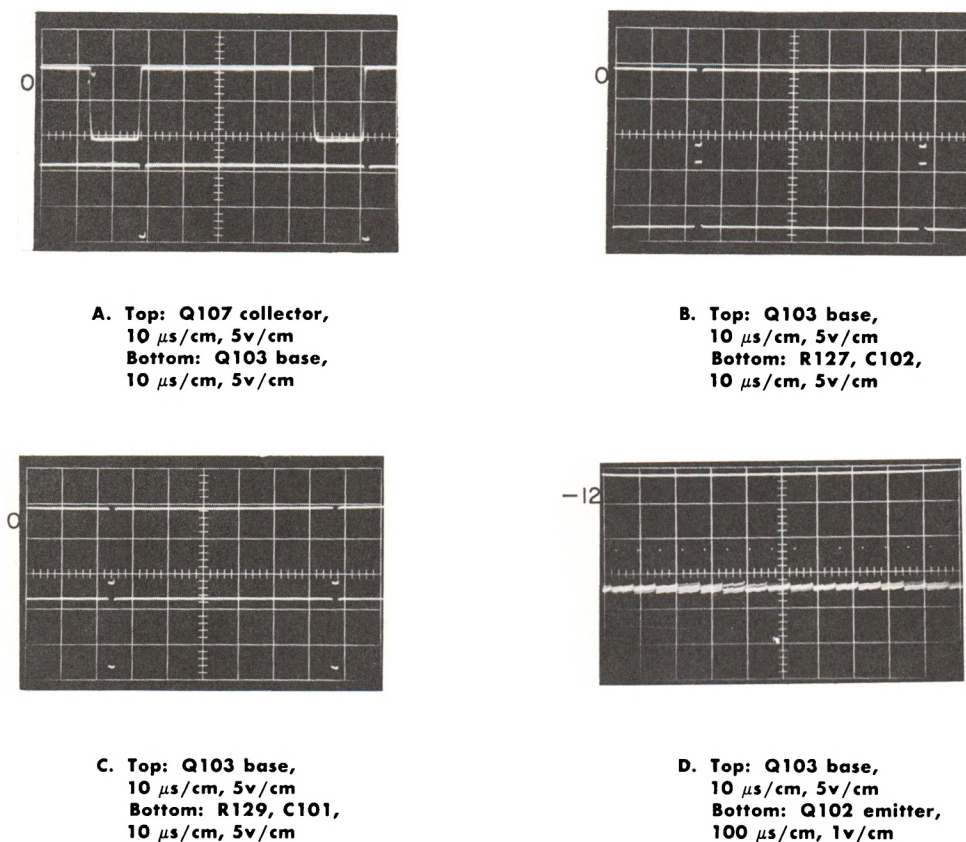


Figure 142—Typical Waveforms, AFC Current Amplifiers

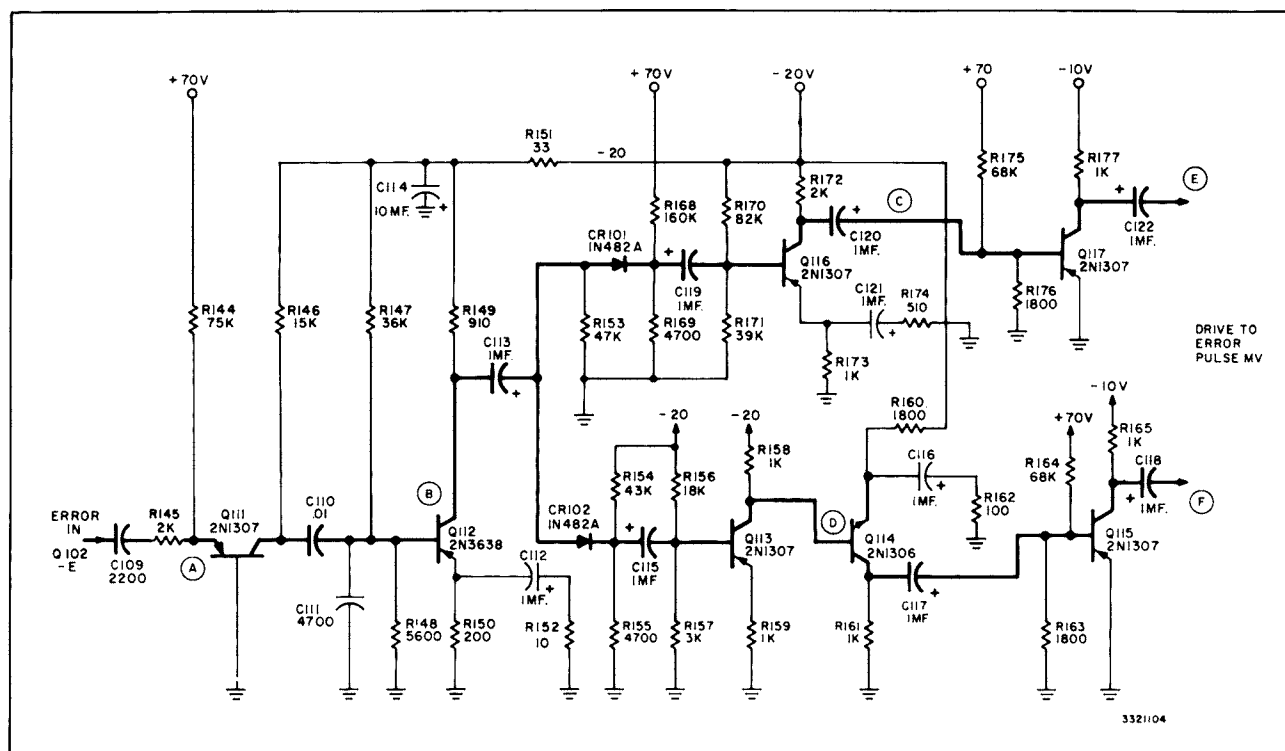


Figure 143—Error Pulse Amplifiers

clipped by the diode action of the base-to-emitter junction of Q5. The remaining negative pulse triggers the boxcar action of Q5. The positive pulse at the collector of Q5 is direct-coupled to the base of the sampling pulse driver, Q4.

In the sampling pulse driver circuit, a negative pulse from the collector and a positive pulse from the emitter of Q4 apply forward bias to all four diodes simultaneously. At the tips of the pulses, the diodes conduct momentarily connecting the sawtooth voltage to capacitor C127 which acts as a memory device, storing the instantaneous voltage of the sawtooth at the moment of connection. During the remainder of the horizontal period, the diodes are reverse biased and C7 remains at the clamped voltage which sets the operating point for the afc current amplifier, Q3, which drives the afc current amplifier Q101, Q102 a complementary symmetry emitter follower.

After processing by sampling quad Z101, and additional current amplification stages Q104, Q105, and Q106 (refer to figure 141) the afc error signal is fed to the 2H master oscillator Q1, Q2. If the incoming tape sync signal changes frequency or phase slightly, the sampling pulse derived from it occurs at slightly different time relative to the sawtooth voltage applied to the phase comparator. Therefore, there is a change

in the instantaneous voltage to which C7 charges. This change causes the afc current to change the frequency and phase of the master oscillator to correspond to that of the incoming signal. When the afc loop is operating properly, sampling of the sawtooth voltage takes place on the fast positive-going portion of the sawtooth.

Switching Transient Suppression

In conjunction with the 2H master oscillator circuitry just discussed another loop of circuits is involved. These are best described as protection or disabling circuits. The reason these come into action is in the playback of certain types of tapes known as "RF dubs". In some cases these tapes may have transients known as switching pulses actually recorded on the tape. In the situation where these pulses occur just prior to every 16th horizontal sync pulse, difficulty in the form of line pulling for three or four lines could develop.

The sync separating circuits cannot distinguish between these transients and the normal horizontal sync. As a result of this, improper correction signals would be fed to the AFC system. In addition, once disturbed in this fashion the disturbance would continue for several lines while the AFC feedback loop goes through its recovery cycle.

To prevent improper control a second sampling system is used. (Refer to block diagram figure 129). The voltage stored on memory capacitor CM1 is not passed immediately to control the oscillator but is instead forced to await a second sampling "inspection". In normal sampling, each sample produces nearly the same voltage on CM1 as did the previous sample. This voltage is continuously monitored by a differentiator, and amplifier Q111 (refer to figure 143). This amplifier and subsequent error amplifiers respond only to changes in voltage. If the voltage at CM1 stays constant, within predetermined limits; a second sampler, S2, transfers the voltage on CM1 to CM2, where it is applied to the controlled oscillator Q1, Q2. However, if the differentiator detects a large change from the preceding sample, it sends an inhibit signal by the ten-line monostable multivibrator Q118, Q119 on to the sample pulse gate, Q109; through

which the sample pulse passes to actuate S2 (refer to figure 145). With this gate inhibited, no sample pulse passes to S2; hence, the voltage on CM1 is not transferred to CM2, and the oscillator is not disturbed by the bad sample.

The previous voltage on CM2 holds the oscillator on the right frequency and phase until a proper sample is passed by S1. This sampled voltage is then passed on to CM2, and the normal functioning of the circuit resumes.

During the lockup cycle, each sample differs considerably from the preceding one. This system, applied in its simplest form, would inhibit every sample, and would prevent lockup from ever taking place. The ten-line multivibrator Q118, Q119 allows inhibiting action only on every tenth sample; the 9 intermediate samples are passed without regard to the differentiator's evaluation of them. This assures lockup.

PLAY MODE — MACHINE ADJUSTED FOR FRONT PORCH SWITCHING

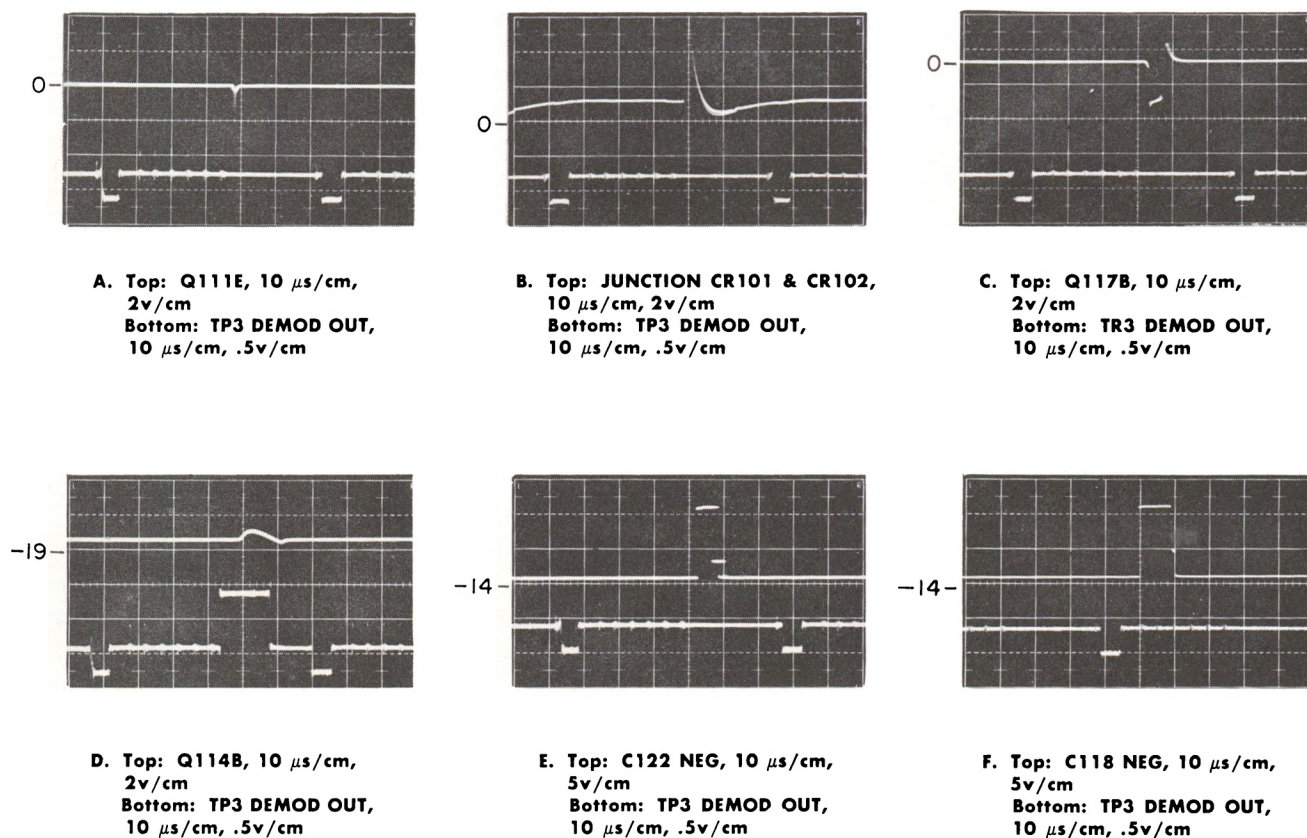


Figure 144—Typical Waveforms, Error Pulse Amplifiers

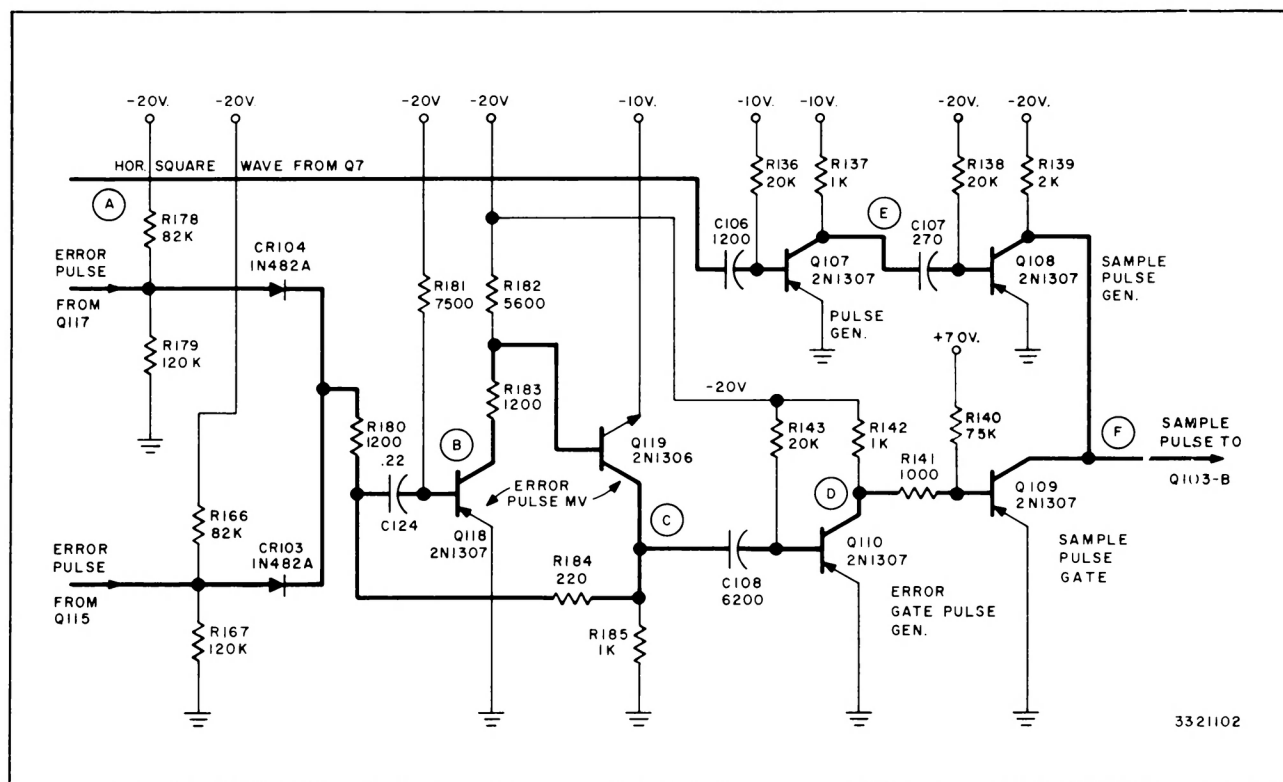
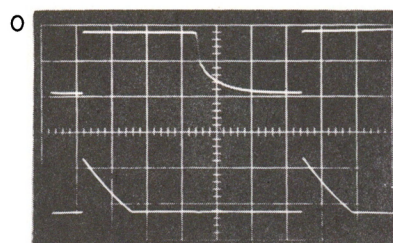
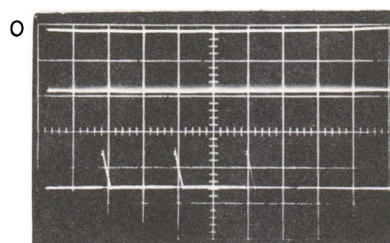


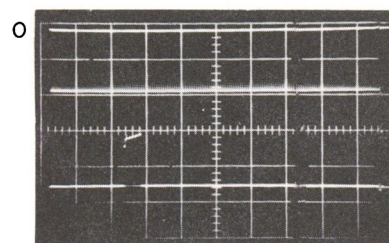
Figure 145—Error Pulse MV and Sample Pulse Generator



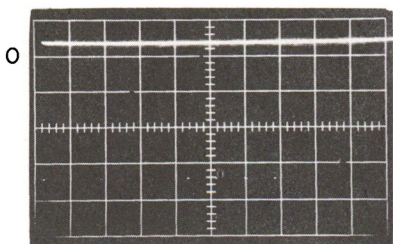
**A. Top: Q7 collector, 10 μ s/cm, 5v/cm
Bottom: Q107 base, 10 μ s/cm, 2v/cm**



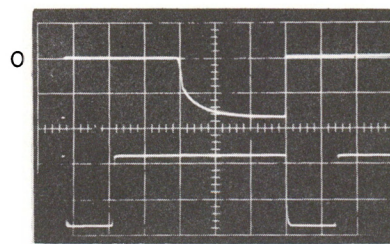
**B. Top: Q7 collector, 2 ms/cm, 5v/cm
Bottom: Q118 base, 2 ms/cm, 2v/cm**



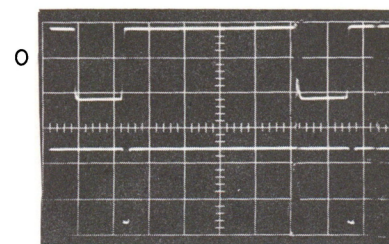
C. Top: Q7 collector, 2 ms/cm, 5v/cm. Bottom: Q119 collector (Adj. switching pulse to leading edge of sync) 2 ms/cm, 5v/cm



D. Q110 collector, 5 ms/cm, 2v/cm



**E. Top: Q7 collector, 2 μ s/cm, 5v/cm
Bottom: Q107 collector, 10 μ s/cm, 5v/cm**



**F. Top: Q107 collector, 10 μ s/cm, 5v/cm
Bottom: Q109 collector, 10 μ s/cm, 5v/cm**

Figure 146—Typical Waveforms; Error Pulse MV and Sample Pulse Generator

Since transients can be either negative or positive in direction two error pulse paths are provided. One via Q116, Q117; the other via Q113, Q114, Q115. The extra stage in the latter path inverts the signal so that the output pulses at Q117 and Q115 are always of positive polarity for triggering the error pulse multi-vibrator.

ADJUSTMENTS

Select line standard desired on the Vertical Advance Module.

2H Master Oscillator Adjustment

The oscilloscope or the picture monitor triggered with external sync, can be used to adjust the center frequency of the master oscillator.

Using Oscilloscope

1. Observe the video output on the CRO by pressing VID OUT on the CRO switcher.
2. Press the CRO HOR button and EXT SYNC, on the CRO switcher.
3. With the switch on the Play panel in MOD-DEMOD position, and an incoming video signal of the desired line standard the outgoing signal should be observed on the CRO.
4. Press and hold the AFC OFF pushbutton (switch S1) on the front of the Horizontal AFC module. Adjust the appropriate 2H FREQ control, until the pattern on the CRO is as nearly stationary as possible. The upper control on the module is for 525/625 and the lower control 405 or 819 lines. Release the pushbutton.

Using Picture Monitor

1. Observe the video output on the picture monitor by pressing VID OUT on the monitor switcher.
2. Repeat step 4 above but observe the picture monitor while making the adjustment.

NOTE

To make the remaining internal adjustments, the Horizontal AFC module should be mounted in the extender. In addition, the adjustments require the use of an external oscilloscope such as the Tektronix 535A. Dual trace is at times desirable. Refer to the chart below for various widths for different standards. Individual minor changes due to local requirements can be made.

	<i>Line Standard</i>		
Pulse Widths	405	525	625
Hor. Sync	9.25	4.75	4.9
Hor. Blanking	18.0	11.0	11.85
Front Porch	1.56	1.5	1.4
Vert. Blanking	1425	1250	1290
(Times are in microseconds)			

Front Porch Width Adjustment

1. Connect the oscilloscope to one of the five VID test jacks (TP1, TP2, TP3, TP4, TP5) on the front of the Video Output module.
2. Trigger the scope with REF HOR (TP-2) on the Reference Generator module. Adjust the scope to display a horizontal blanking interval.
3. Adjust the FRONT PORCH WIDTH control (R37 for 525/625, R69 for 405) to the proper width as shown on the chart above.

Horizontal Sync Width Adjustment

1. Same conditions as steps 1 and 2 in Front Porch Width Adjustment.
2. Adjust the HOR SYNC WIDTH control (R45 for 525/625, R71 for 405) for proper width as shown in the chart.

Sync Timing Adjustment

Place the picture monitor switch for raster display in the P.C. (Pulse Cross) position. Play back a tape of the required standard and adjust the sync timing control (R56 for 525/625, R76 for 405) so that the horizontal sync during the vertical interval is lined up with the main portion of the picture information.

Replace module in the machine.

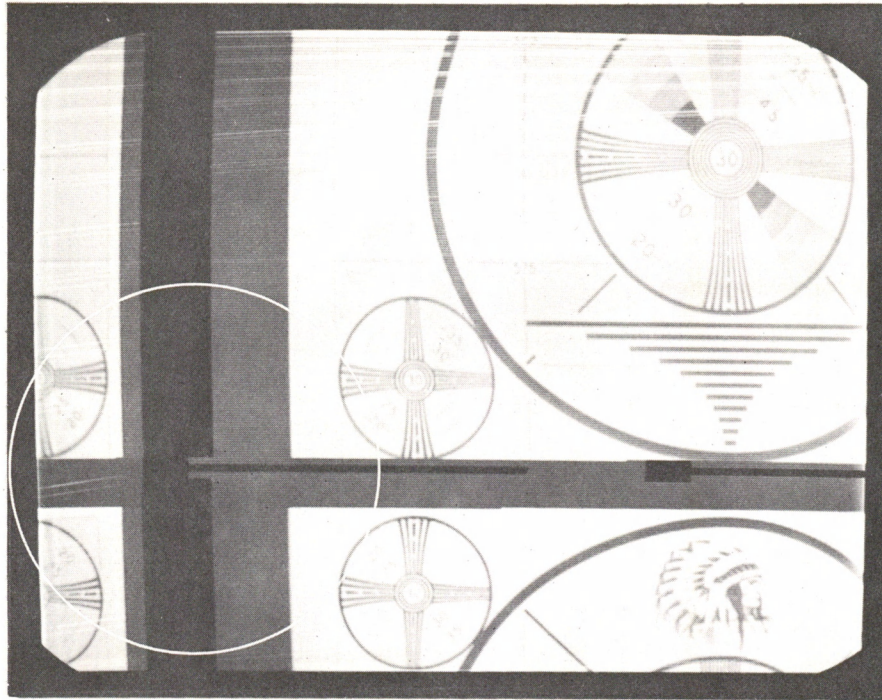
VERTICAL ADVANCE (Module 228)

(Refer to Block Diagram Figure 148)

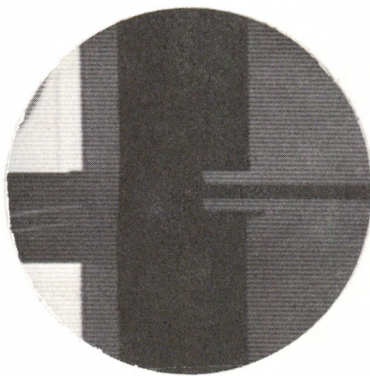
NOTE

In the following discussion the 525 line system is considered basic, with appropriate notes for the other systems being added where applicable. In the discussion, the 9H pulse changes to 7.5H for 625 lines and 4H for 405 lines. The 3.5H vertical advance pulse in the 525 line system, changes to 3.0H in 625 lines. In the 405 system the vertical advance is 1.5H.

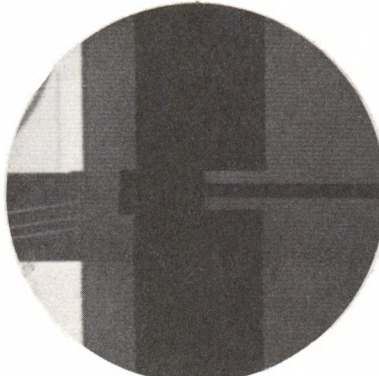
PULSE CROSS PRESENTATION



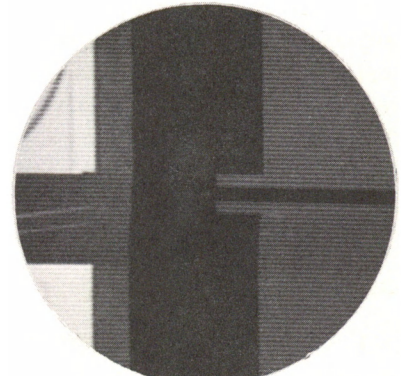
a. Normal Test Pattern (Picture Monitor)



b. Misadjusted Sync Gate Width Control, R-32 (Sync Logic Module 230B)



c. Misadjusted Sync Timing Adjustment Control, R-56 (Horizontal AFC Module 227B)



d. Normal Sync Timing

Figure 147—Adjustment of Sync Forming Circuits (Picture Monitor)

The Vertical Advance module is required to produce the timing edge which determines the leading edge of vertical blanking and the 9H gating pulse. The method of vertical pulse advance used must regenerate the vertical blanking edge, which precedes the vertical sync signal by 3H. The technique used to obtain vertical advance is that of counting horizontal pulses between adjacent vertical intervals. The counters designed to follow any change in basic sync frequency and automatically readjust the position of vertical blanking. Moreover, they recover quickly from transient disturbances in the recording system.

Separate time constant components are used for all standards in the first two counter stages, Q3, Q10, and Q5, Q11, respectively. In the third and fourth counters, Q6, Q12 and Q7, Q13, respectively, the time constants for the 405- and the 625-line standards are combined and the 525-time constants are separate. All time constants are selected by means of rotary switch S2, which is located on this module. This switch also supplies the international switching busses (HI, HN, and VI, VN) with the proper dc operating levels. The switch control, designated TV STANDARDS, is mounted on the front panel of the module.

In addition to time constant components, the timing of the vertical advance pulse (3.5H) is changed to accommodate the 405- and the 625-line standards. Since there are five equalizing pulses in the 625-line system, the vertical advance must be 3H wide; however, the width of the first $\div 5$ count cycle is only 2.5H wide. Therefore, in order to produce a 3H pulse from the 2.5H count, a miscount pulse amplifier, Q15, and associated circuitry has been incorporated (see figures 154 and 155).

MISCOUNT PULSE AMPLIFIER

The operation of this circuit will be discussed later.

Timing Chart

In the 525-line timing chart, figure 149, the relative positions of the vertical blanking edge, equalizing pulses and vertical sync interval are shown. The leading edge of the second vertical sync pulse is the earliest possible time for detecting accurately the position in the vertical sync. Although the timing difference

NOTE

ON refers to active counting time; OFF refers to resting time of counters. Conducting state of transistors (ON-OFF) is opposite to that of the counters.

between the beginning of vertical blanking and vertical sync is 3H, observe on the timing chart that the

difference between the two edges (vertical blanking and the second vertical sync pulse position) is actually 3.5H. This timing distance of 3.5H must be maintained to produce vertical blanking from vertical sync. The timing distance of 3.5H is exactly the period of a $\div 7$ MV counter running from a 31.5 kc master oscillator. The vertical advance circuits must, therefore, select that one period of the $\div 7$ MV (one out of the 75 periods which occur in each field) which is so phased that the beginning of the period falls on the leading edge of vertical blanking and the end of the period falls 3.5H later in vertical sync. As shown in figure 148, the 31.5 kc pulses supplied through the 2H amplifier, Q1, and the trigger eliminator, Q2, activate a string of counters. The count is initiated by the start pulse which is generated from the vertical sync in the Sync Logic module. The counters count for 259 lines then shut off due to the coincidence of the last three counters ($\div 5$, $\div 5$, $\div 3$) and normally remain shut off for a period of (3.5H). This period of 3.5H added to 259H equals 262.5 lines or one field. The next cycle is started by the generation of another START pulse in the Sync Logic module. Under unusual operating conditions due to a non-synchronous switch or a bad splice in the tape, the vertical sync period of the tape sync signal may arrive at a much later time. In this event, the counters remain off until a new start pulse is generated when vertical sync does arrive.

Gating Circuits

As shown in the simplified schematic, figure 150, the 2H input pulses from the Horizontal AFC module are applied to the base of Q1 through the differentiating network C1 and R1. The 2H amplifier, Q1, is an emitter follower which clips the negative spike from the differentiated pulse. The trigger pulses from the emitter of Q1 are coupled to the counter chain through the isolation diode, CR2.

The (31.5 kc) pulses are gated by Q2, the trigger eliminator, which is driven to saturation during the (3.5H) interval, shorting out the pulses. At all other times, Q2 is biased off, allowing the pulses to pass to the counter chain. The (3.5H) pulse driving Q2 is coupled to its base from the collector of Q8, the start pulse amplifier. Transistor Q8 is also normally biased off because its base is held to approximately 0 volts, the potential on the anode of CR6. During the (3.5H) pulse interval the anode voltage of CR6 drops to -10 volts, allowing the base of Q8 to fall to the potential determined by the bias network of R31, R32, and R34. In this state, Q8 conducts and drives Q2 to satu-

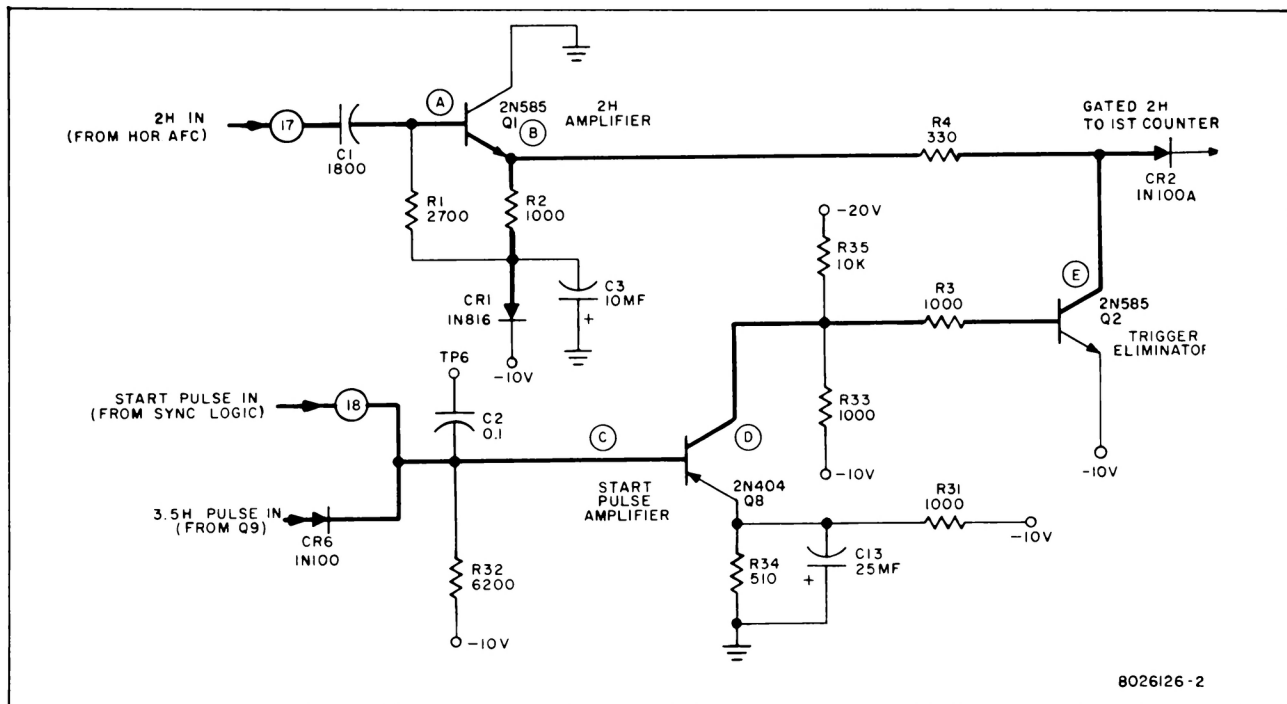
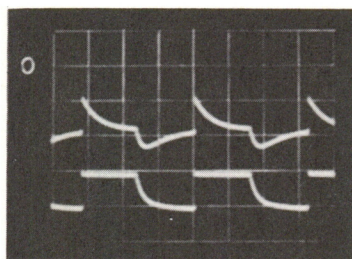
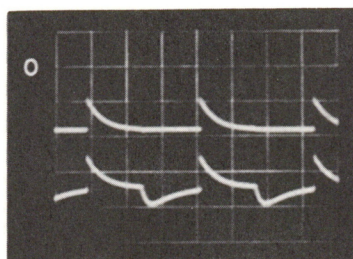


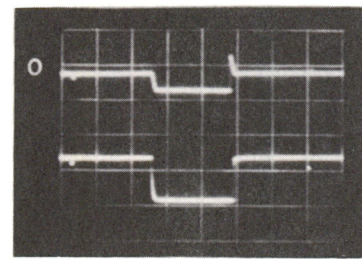
Figure 150—2H Amplifier, Trigger Eliminator and Start Pulse Amplifier Circuits



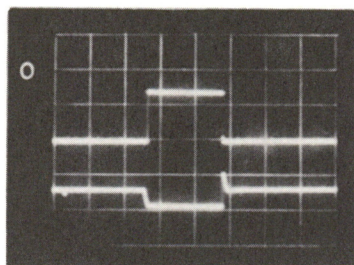
**A. Top: Q1 base, 10 μ s/cm, 5v/cm
Bottom: C1 input, 10 μ s/cm, 5v/cm**



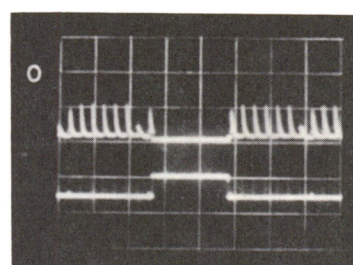
**B. Top: Q1 emitter, 10 μ s/cm, 5v/cm
Bottom: Q1 base, 10 μ s/cm, 5v/cm**



**C. Top: Q8 base, 100 μ s/cm, 5v/cm
Bottom: CR6 input, 100 μ s/cm, 5v/cm**



**D. Top: Q8 collector, 100 μ s/cm, 5v/cm
Bottom: Q8 base, 100 μ s/cm, 5v/cm**



**E. Top: Q2 collector, 100 μ s/cm, 5v/cm
Bottom: Q2 base, 100 μ s/cm, 2v/cm**

Figure 151—Typical Waveforms; 2H Amplifier, Trigger Eliminator and Start Pulse Amplifier Circuits (525 Lines)

ration. Transistors Q8 and Q2 remain conducting until a positive start pulse drives Q8 off which, in turn, drives Q2 off. This allows a 2H trigger pulse to pass, starting the counters and thereby terminating the (3.5H) pulse. The base of Q8 is again held to 0 volts and does not conduct. (See figure 151.)

Counters

With S2 in the 525 line position as shown in figure 152, the first counter, is a $\div 7$ MV, a monostable multivibrator consisting of Q3 and Q10. It is similar in design to the $\div 2$ MV in the Horizontal AFC module. Both transistors, Q3 and Q10, conduct in the stable state. When the base is driven positive by the first pulse, Q3 is driven to cutoff (also cutting off Q10). Time constant C4, R6, and R7 determine the length of time the multivibrator is cut off. The transistor must return to the stable conducting state just after the seventh pulse.

The operation of the 2nd counter (Q5, Q11) is similar to that of the 1st counter. However, the conducting time of the transistors is not entirely dependent on the time constant of C9, R19, and R20. Variations in component values and transistor characteristics cause slight variations in timing. Since one of the conduction times of the multivibrator is the 3.5H

pulse, precise timing is essential for both on and off transitions. This is accomplished by using the triggers not only to start but also to stop the timing cycle.

The positive and negative trigger pulses required to start and stop the 2nd counter are generated by the bidirectional trigger, Q4, in conjunction with diodes CR3 and CR4. As shown in figure 152, the collector of Q4 is dc connected through CR4 and R17 to the junction of R44 and R45 in the collector circuit of Q11. In the stable state of the multivibrator, when Q11 is conducting, the voltage at the junction of R44 and R45 is almost -10 volts, and Q4 does not conduct since the emitter and collector of Q4 are at the same potential. However, a positive spike resulting from the differentiation of the $\div 7$ pulse is passed by CR3 through C9 to the base of Q5. The positive spike cuts off Q5 and Q11, and the voltage at R44 and R45 rises to 0 volts. In this condition, CR3 is reverse-biased and does not pass the positive spikes. Now, however, the collector-to-emitter voltage of Q4 is sufficient to provide amplification of the positive spikes fed to its base. The resulting negative trigger pulses at the collector of Q4 are passed through CR4 and C9 to the base of Q5. On the fifth count, Q5 and Q11 are driven into conduction, and the cycle repeats. Switch S2 changes standards and counters as shown in the chart on figure 148.

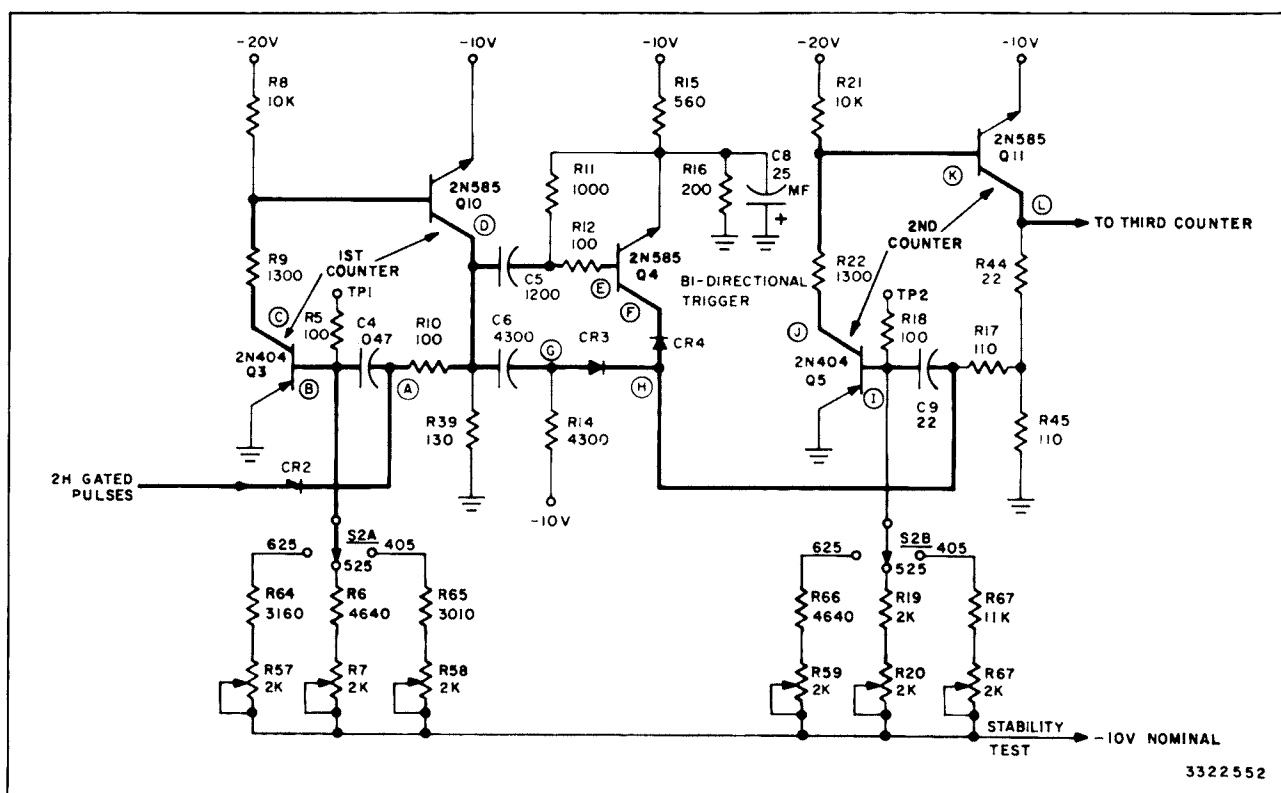


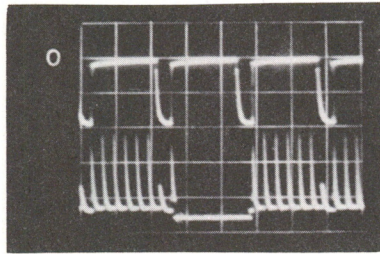
Figure 152—First Counter, Bi-Directional Trigger and Second Counter Circuits

As shown in figure 152, the final two counters, the $\div 5$ MV (Q6, Q12) and the $\div 3$ MV (Q7, Q13) are identical in operation to the $\div 7$ MV (Q3, Q10). Each multivibrator conducts in the stable state; each is cut off by the positive spike resulting from the differentiation of the trailing edge of the preceding pulse

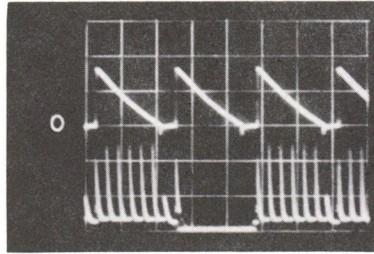
output. The trailing edge of the $\div 3$ counter pulse is used as an emergency trigger for the vertical blanking generator multivibrator in the Sync Logic module.

Coincidence Gate

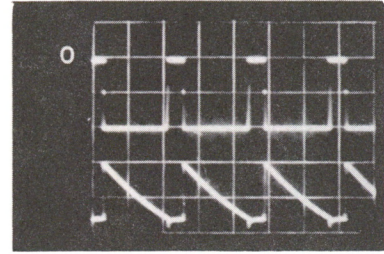
The coincidence gate consists of three diodes, CR7,



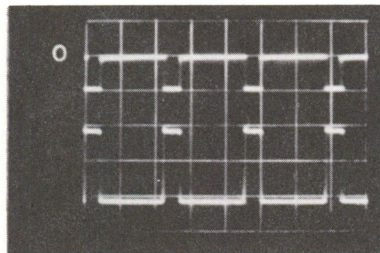
A. Top: C4, R10, CR2,
100 μ s/cm, 5v/cm
Bottom: gated 31.5 kc (Q2
collector, 100 μ s/cm, 2v/cm)



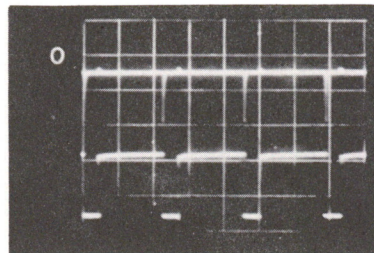
B. Top: Q3 base, 100 μ s/cm,
5v/cm
Bottom: gated 31.5 kc (Q2
collector, 100 μ s/cm, 2v/cm)



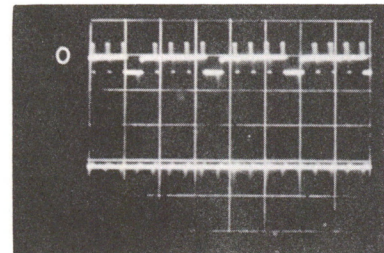
C. Top: Q3 collector, 100 μ s/cm,
10v/cm
Bottom: Q3 base, 100 μ s/cm,
5v/cm



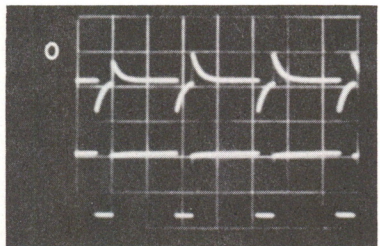
D. Top: Q10 collector, 10 μ s/cm,
10v/cm
Bottom: Q10 base, 100 μ s/cm,
5v/cm



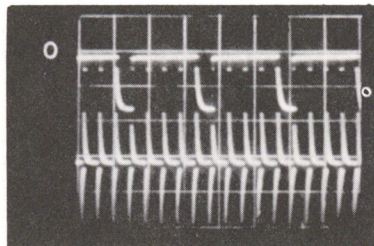
E. Top: Q4 base, 100 μ s/cm,
5v/cm
Bottom: Q10 collector,
100 μ s/cm, 5v/cm



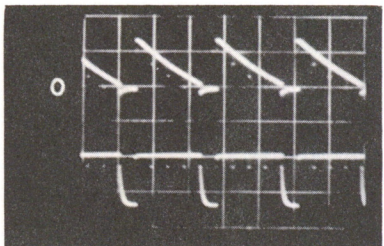
F. Top: Q4 collector, 500 μ s/cm,
5v/cm
Bottom: Q4 base, 500 μ s/cm,
5v/cm



G. Top: C6, CR3, R14, 100 μ s/cm,
10v/cm
Bottom: Q10 collector,
100 μ s/cm, 5v/cm

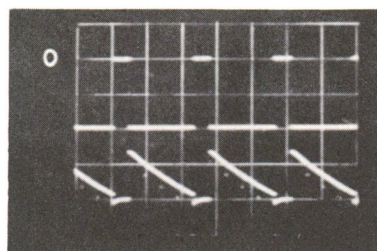


H. Top: CR3, CR4, 500 μ s/cm,
5v/cm
Bottom: C6, CR3, R14,
500 μ s/cm, 5v/cm

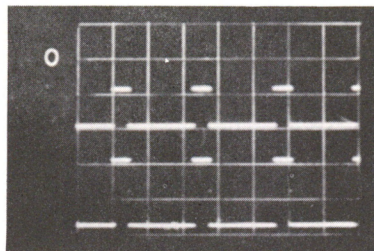


I. Top: Q5 base, 500 μ s/cm,
5v/cm
Bottom: C9, R17, 500 μ s/cm,
5v/cm

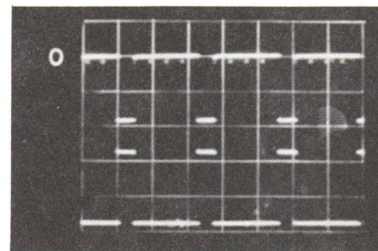
Figure 153—Typical Waveforms; First Counter, Bi-Directional Trigger and Second Counter Circuits



**J. Top: Q5 collector, 500 μ s/cm, 10v/cm
Bottom: Q5 base, 500 μ s/cm, 5v/cm**



**K. Top: Q11 base, 500 μ s/cm, 10v/cm
Bottom: Q5 collector, 500 μ s/cm, 10v/cm**



**L. Top: Q11 collector, 500 μ s/cm, 5v/cm
Bottom: Q11 base, 500 μ s/cm, 5v/cm**

Figure 153—Typical Waveforms; First Counter, Bi-Directional Trigger and Second Counter Circuits (Continued)

CR9, CR10. The cathode of each diode is connected to -10 v through resistor R36. The anode of each diode is connected to the collector of the output transistor of each of the last three counter multivibrators, $\div 5$ MV, $\div 5$ MV, and $\div 3$ MV. When any one of these multivibrators is in the non-conducting (counting) state, its collector is at 0 volts, and the corresponding diode connected to its collector conducts, holding the base of the vertical advance pulse (3.5H) and amplifier, Q9, close to 0 volts, causing the amplifier to conduct. However, if none of these multivibrators is counting, a condition which occurs 259H from the start of the counter cycle, none of the diodes conduct. The base of Q9 then drops to -10 volts and the transistor is cut off. The emitter of Q9 is normally at 0 volts when the transistor is conducting, providing the holding voltage for the anode of CR6 of the trigger gating circuits. During the (3.5H) period of coincidence, this voltage drops to -10 volts. Switch S2 changes the counters as shown on the chart of figure 148.

MISCOUNT PULSE AMPLIFIER (See figure 154)

The output of the four counters (Q7, Q13) is a 50-cycle signal, the leading or positive-going edge of which is used to trigger the miscount amplifier, Q15. The latter is a pulse narrowing or "boxcar" circuit. The output of Q15 is a negative pulse, approximately 50 microseconds wide, that begins with the leading edge of the second vertical sync pulse. This pulse is applied to the first counter, Q3, Q10, through the timing network of C4 and R70.

During the duration of the miscount pulse, C4 dis-

charges at a faster rate than when the pulse is absent so that it is discharged before the fifth trigger arrives, and then the counter can return to its resting state. This allows the fifth trigger to start the counter for the next count, thereby shortening the time cycle of the previous count (see figure 156). Additional energy is supplied from the miscount amplifier, Q15, to the second counter, Q5, Q11, through R73 during the miscount period. At the end of the miscount pulse period, the counter reverts to its normal counting ($\div 5$) rate. It continues to count at this rate until the next to the last count before the next field period.

The last count starts in the usual manner, and C4 discharges before the sixth trigger. However, at this time all of the counters are in the off or non-counting state, and the train of triggers from the 2H amplifier, Q1, are gated out by the trigger eliminator, Q2. During this time, there is no trigger to start the first counter before the sixth count is enclosed. After the sixth count, the start pulse arrives, gating on the trigger eliminator which, in turn, allows the 2H pulses to pass and trigger the first counter. The first trigger appears simultaneously with the start pulse and thus the counting cycle starts over again.

In the 405-line system there are no equalizing pulses and the vertical interval begins with the leading edge of the first vertical sync pulse. The start pulse is timed to occur with the leading edge of the third vertical sync pulse (see figure 157) therefore the vertical advance pulse is 1.5H wide. Since the first counter is a $\div 3$ multivibrator, the output is a 1.5H signal, and this is exactly the width of the vertical advance pulse. Therefore the count during one

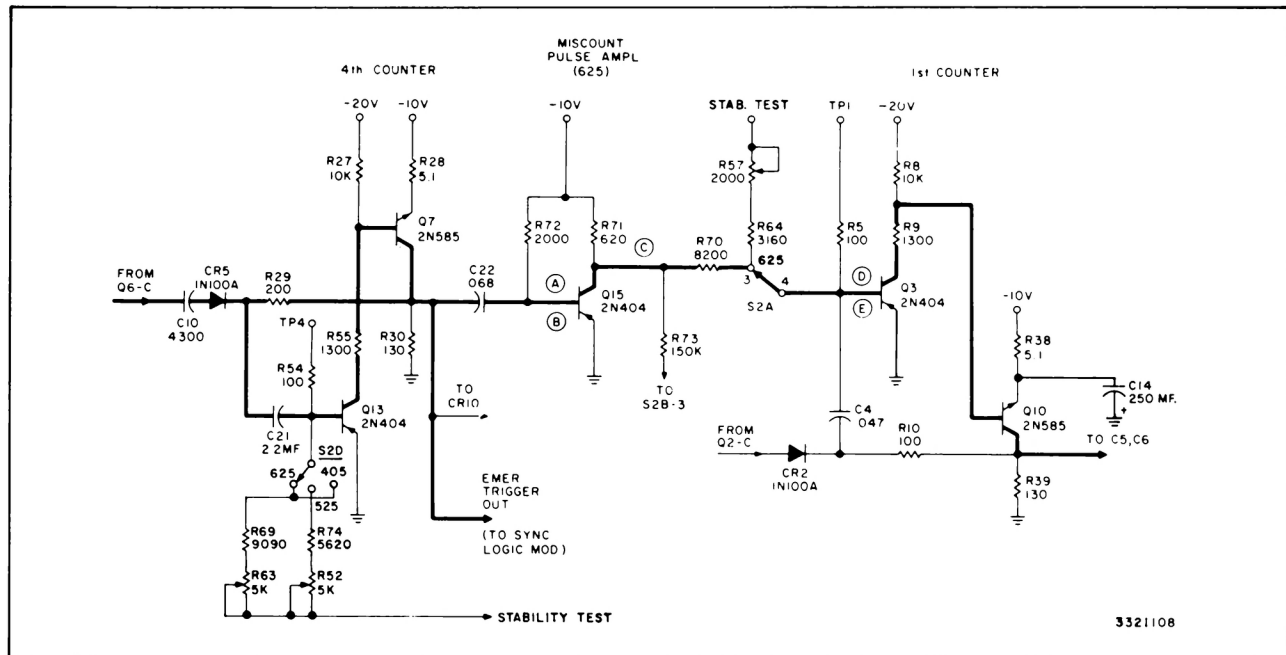
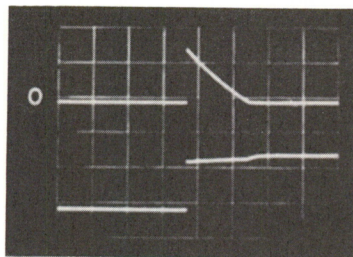
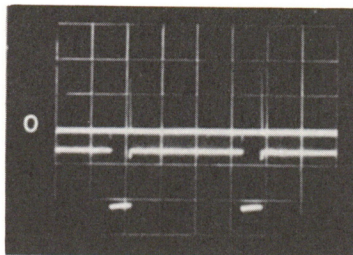


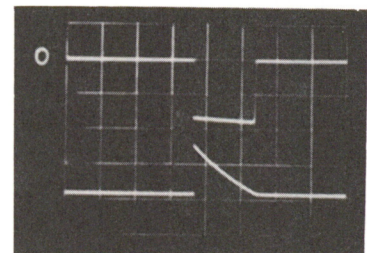
Figure 154—Fourth Counter, Miscount Pulse Amplifier and First Counter Circuits



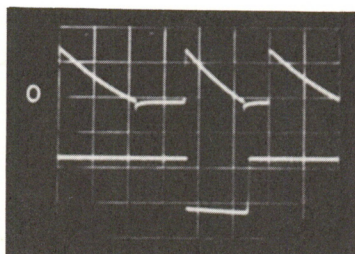
**A. Top: Q15 base, 50 μ s/cm, 5v/cm
Bottom: Q7 collector, 50 μ s/cm, 5v/cm**



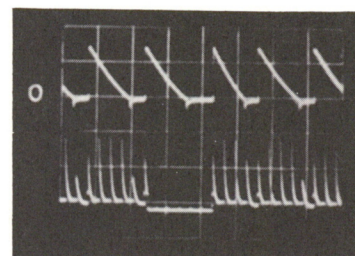
**B. Top: Q15 base, 5000 μ s/cm, 5v/cm
Bottom: Q7 collector, 5000 μ s/cm, 5v/cm**



**C. Top: Q15 collector, 50 μ s/cm, 5v/cm
Bottom: Q15 base, 50 μ s/cm, 5v/cm**



**D. Top: Q3 base, 50 μ s/cm, 5v/cm
Bottom: Q15 collector, 50 μ s/cm, 5v/cm**



**E. Top: Q3 base, 100 μ s/cm, 2v/cm
Bottom: Q2 collector, 100 μ s/cm, 2v/cm**

Figure 155—Typical Waveforms; Fourth Counter, Miscount Pulse Amplifier and First Counter Circuits

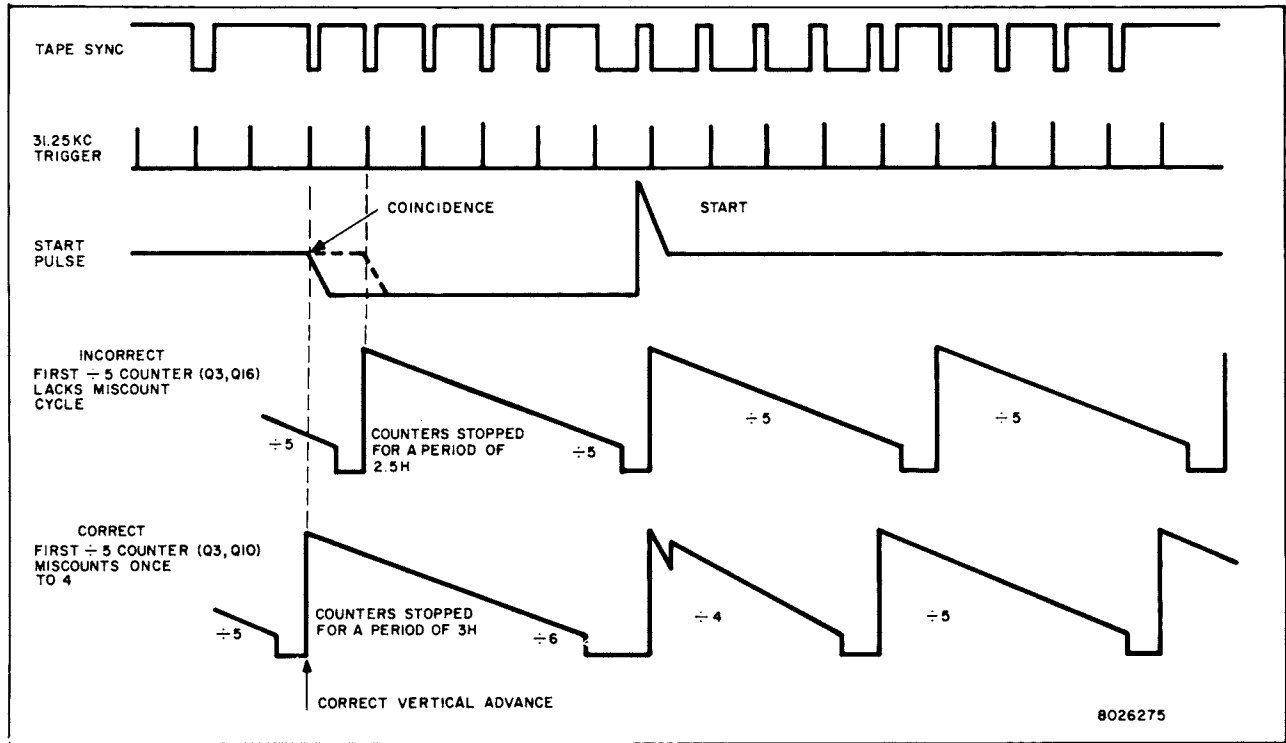


Figure 156—3.0H Vertical Advance for 625-Line Standard

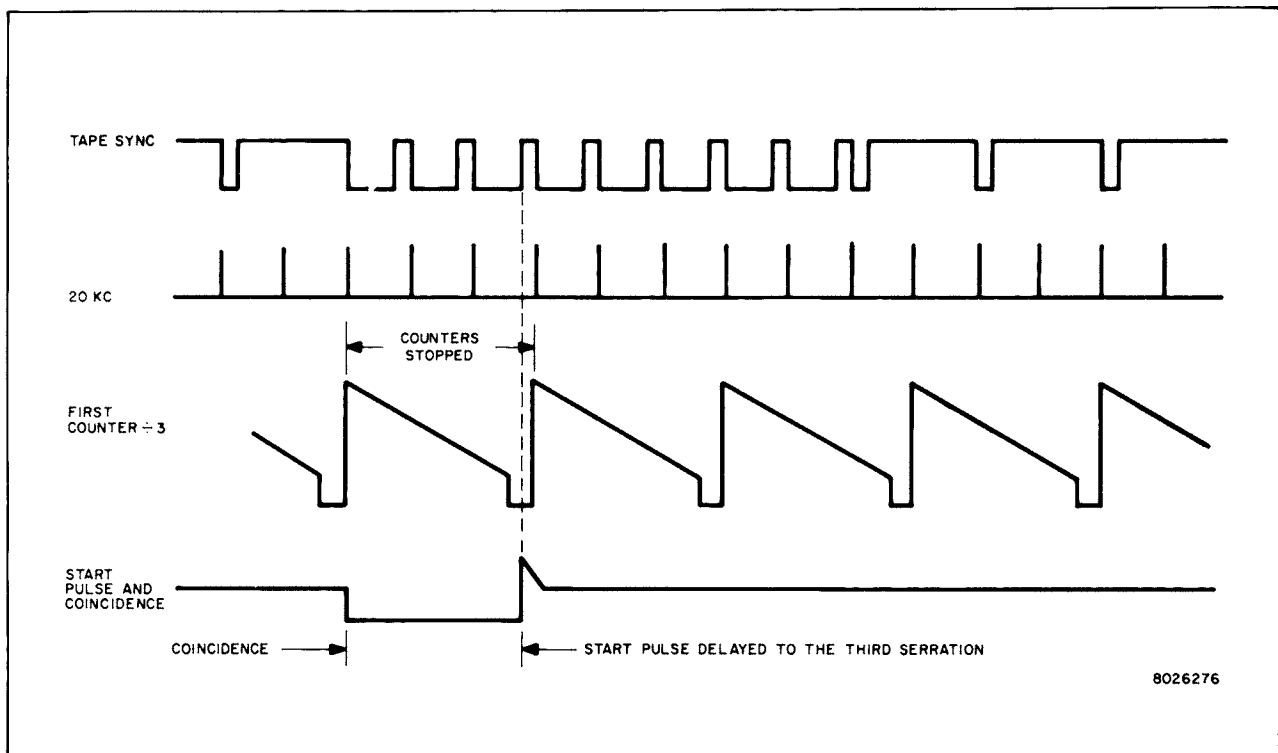


Figure 157—1.5H Vertical Advance for 405-Line Standard

field comes out evenly and the last count is $1.5H$ wide. The next $2H$ trigger arrives simultaneously with the start pulse to begin a new counting cycle.

The stability test circuit, shown in figure 158 provides a temporary variation in the power supply voltage to ensure that the counters have been set approximately in the middle of the range in which they provide the proper count. If one or more of the counters has been set too near the edge of its range, it will miscount when the STABILITY TEST button is pressed and the STABILITY RANGE potentiometer, R41, is varied. (The procedure for adjusting the counters is given at the end of this description, under Adjustments.)

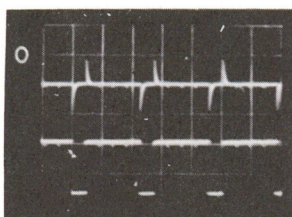
1. Place the tape recorder in the MOD state by

pressing the DEMOD mode selection pushbutton, PLAY-MOD.

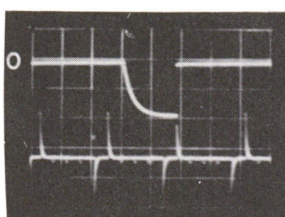
2. Connect an oscilloscope to the VERT ADV test point (TP5) on the front of the module.

3. Set the oscilloscope sweep time to vertical rate and expand the trace to observe the 3.5H pulse. (1.5H on 405 standards.)

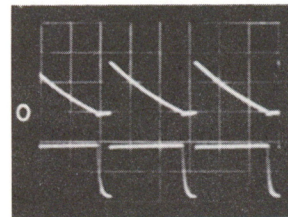
4. Press and hold the STABILITY TEST push-



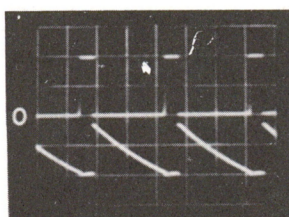
**A. Top: C16, CR8, R46,
500 μ s/cm, 10v/cm
Bottom: Q11 collector,
500 μ s/cm, 5v/cm**



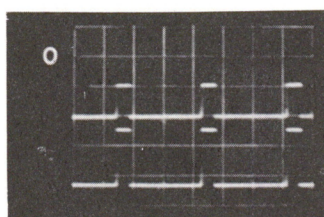
**B. Top: C17, CR8, R51,
500 μ s/cm, 5v/cm
Bottom: C16, CR8, R46,
500 μ s/cm, 5v/cm**



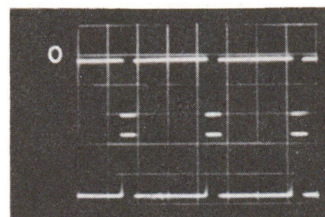
**C. Top: Q12 base, 2 ms/cm,
5v/cm
Bottom: C17, CR8, R51,
2 ms/cm, 5v/cm**



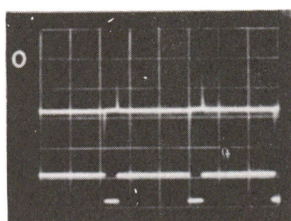
**D. Top: Q12 collector, 2 ms/cm,
10v/cm
Bottom: Q12 base, 2 ms/cm,
5v/cm**



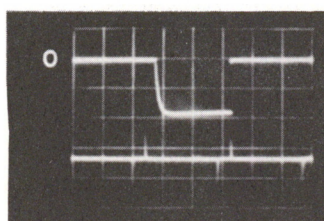
**E. Top: Q6 base, 2 ms/cm,
10v/cm
Bottom: Q12 collector,
2 ms/cm, 10v/cm**



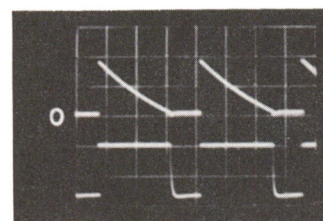
**F. Top: Q6 collector, 2 ms/cm,
5v/cm
Bottom: Q6 base, 2 ms/cm,
5v/cm**



**G. Top: C10, CR5, R26, 2 ms/cm,
5v/cm
Bottom: Q6 collector,
2 ms/cm, 10v/cm**

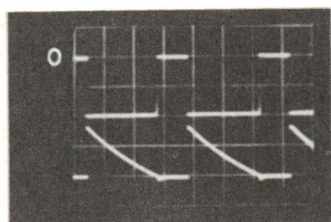


**H. Top: C18, CR5, R29, 2 ms/cm,
5v/cm
Bottom: C10, CR5, R26,
2 ms/cm, 10v/cm**

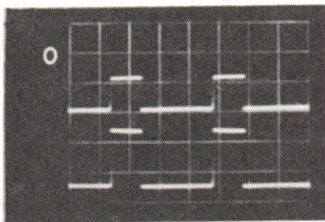


**I. Top: Q13 base, 5 ms/cm,
5v/cm
Bottom: C18, CR5, R29,
5 ms/cm, 5v/cm**

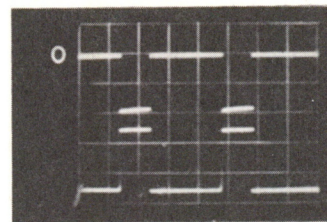
Figure 159—Typical Waveforms, Third Counter, Fourth Counter and Coincidence Detector Circuits



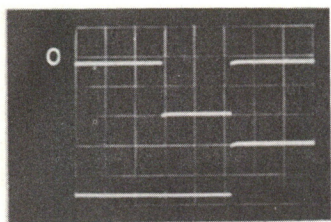
**J. Top: Q13 collector, 5 ms/cm, 10v/cm
Bottom: Q13 base, 5 ms/cm, 5v/cm**



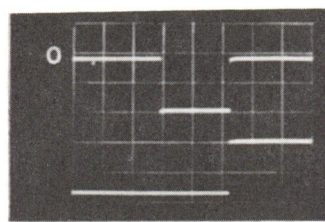
**K. Top: Q7 base, 5 ms/cm, 10v/cm
Bottom: Q13 collector, 5 ms/cm, 10v/cm**



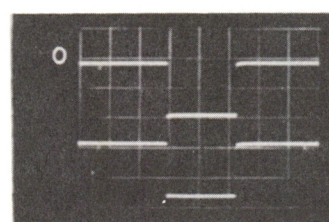
**L. Top: Q7 collector, 5 ms/cm, 5v/cm
Bottom: Q7 base, 5 ms/cm, 5v/cm**



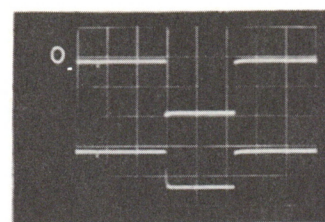
**M. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q7 collector, 100 μs/cm, 5v/cm**



**N. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q6 collector, 100 μs/cm, 5v/cm**



**O. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q11 collector, 100 μs/cm, 5v/cm**



**P. Top: Q9 emitter, 100 μs/cm, 5v/cm
Bottom: TP5, 100 μs/cm, 5v/cm**

Figure 159—Typical Waveforms, Third Counter, Fourth Counter and Coincidence Detector Circuits (Continued)

button; then rotate the STABILITY TEST control through its entire range. The pulse width and amplitude should not change in any respect. Minor disturbances appearing on the base line do not indicate improper operation. If the pulse width or amplitude change while the control is being rotated, the counters must be readjusted.

ADJUSTMENT OF COUNTERS (525)

The counters, the 3.5H pulse, and the start pulse in the Vertical Advance module form a continuous loop which makes it difficult, when a marginal counter is indicated, to determine which counter is at fault. The following procedure provides a method for identifying and correcting a marginal or defective counter.

Use of a single trace oscilloscope is assumed in the following procedure, therefore it is necessary to change the sweep of the oscilloscope as indicated in the following in order to maintain the various counter signals within the 10-cm display of the CRO. However, with a dual trace oscilloscope, inspection of the signals is somewhat simplified, since the output of each counter may be compared directly to the output of the preceding stage. This makes it unnecessary to set the sweep at an arbitrary 10 cm.

The adjustment described in step 1 (below) is a precautionary measure. This step may be omitted provided it is ascertained that the Horizontal AFC module is functioning properly.

To perform the following adjustments, the module under test must be mounted in an extender.

Horizontal AFC/Vertical Advance Modules

1. Set the oscilloscope on internal trigger. Place the probe on the emitter of Q8. (This is the source of 31.5 kc pulses from the master oscillator, Q1, to the $\div 2$ multivibrator, Q9, Q10.) Adjust the oscilloscope sweep so that two 31.5 kc pulses cover 10 cm on the oscilloscope. Then move the probe to the $\div 2$ test point, TP1. One cycle of the $\div 2$ MV should be 10-cm wide; if not, a failure in the Horizontal AFC module is indicated. This must be corrected before adjusting the counter in the Vertical Advance module. The width of the $\div 2$ waveform should not change at any position of the knob. The $\div 2$ counter must pass this test before the counters in the Vertical Advance module can be adjusted.

2. Disconnect the collector lead of Q2 from the terminal at the junction of CR2 and R4; leave the jumper and CR2 connected to the terminal. (This opens the loop and allows the counters to run freely.)

3. Set the oscilloscope on internal trigger. Locate C1 which is connected to the base of Q1 and place the probe on the input side of C1. The CRO display will show the 31.5 kc input signal.

4. Adjust the sweep so that seven 31.5-kc pulses cover 10 cm on the oscilloscope. Then move the probe to the No. 1 counter test point, TP1. One cycle of the $\div 7$ MV should be 10 cm (seven 31.5 kc pulses) wide. If it is not, adjust R7, the $\div 7$ MV "trim-pot", until the cycle measures 10 cm.

5. Press and hold the STABILITY TEST push-button, and rotate the STABILITY TEST control through its range. The width of the $\div 7$ cycle should not change.

6. Set the oscilloscope sweep so that five $\div 7$ pulses cover 10 cm on the oscilloscope. Place the probe on the No. 2 counter test point, TP2. One cycle of the first $\div 5$ MV (Q5, Q11) should be 10 cm (five $\div 7$ pulses) wide. To obtain this it may be necessary to adjust the $\div 5$ "trim-pot", R20. If so, repeat step 5, this time observing the width of the $\div 5$ cycle, which should not vary.

7. Change the oscilloscope sweep so that five $\div 5$ pulses cover 10 cm on the oscilloscope. Place the probe on the No. 3 counter test point, TP3. One cycle of the third MV (Q6, Q12) should be 10-cm wide (the width of five of the second counter pulses). If it is not, adjust the "trim-pot", R49, then repeat the Stability Test in order to determine the stability of the third counter.

8. Change the oscilloscope sweep so that three of the No. 3 counter pulses cover 10 cm on the oscilloscope. Place the probe on the No. 4 counter test point, TP4. One cycle of the fourth MV (Q7, Q13) should be 10 cm wide (the width of three of the third counter pulses). If not, adjust the "trim-pot", R52, and again perform the Stability Test to determine the stability of the fourth counter.

9. Reconnect the collector of Q2 to the terminal, and replace the module in the tape recorder.

10. Refer to the first section of this procedure, Stability Test of Counter Multivibrators, and re-check the stability of the counters according to the instructions in steps 1 through 5.

ADJUSTMENT OF COUNTERS (625)

Put switch on the vertical advance module in the 625 position. Refer to the 525 line system Horizontal AFC module. In step one the 31.5-kc pulse is now a 31.25-kc pulse. The rest of the checkout procedure is the same.

Vertical Advance Module

1. Perform steps 2 and 3 listed in the 525 line system. The 31.5-kc signal now becomes 31.25 kc. (The module must be on an extender.)

2. Adjust the sweep so that five 31.25 kc pulses cover 10 cm on the oscilloscope. Replace module. Then place the probe on the No. 1 counter test point, TP1. One cycle of the first counter should be 10 cm (five 31.25 kc pulses) wide. If it is not, place the vertical advance modules on the extender and adjust R57, the active 1st counter "trim-pot", until the cycle measures 10 cm.

3. Press and hold the STABILITY TEST push-button, and rotate the STABILITY TEST control through its range. The width of the cycle should not change.

4. Set the oscilloscope sweep so that five of the TP1 pulses cover 10 cm on the oscilloscope. Move the probe to TP2 the second counter test point. One cycle of the second counter (Q5, Q11) should be 10 cm (five of previous $\div 5$ pulses) wide. To obtain this it may be necessary to adjust the "trim-pot", R59. If so, repeat step 3, this time observe the width of the second counter, which should not vary.

5. Again change the oscilloscope sweep so that five of the $\div 5$ pulses cover 10 cm on the CRO. Place the probe on the No. 3 counter test point, TP3. One cycle of the third counter (Q6, Q12) should be 10 cm wide (the width of five of the second counter pulses). If it is not, adjust the now active "trim-pot", R62, then repeat the stability test in order to determine the stability of the third counter.

6. Change the CRO sweep so that five of the No. 3 counter pulses cover 10 cm on the screen. Place the probe on the No. 4 counter test point, TP4. One cycle of the TP4 pulses, from (Q7, Q13) should be 10 cm wide. If not adjust the "trim-pot", R63, and again perform the stability test. If this checks reconnect the collector of Q2.

7. Refer to the first section of this procedure, Stability Test of Counter Multivibrators, steps 1 to 4. If performance is correct replace module in the machine.

ADJUSTMENT OF COUNTERS (405)

Place the standards switch on the vertical advance module in the 405 position and place the horizontal AFC module on an extender. Perform steps 1, 2, and 3 as for the 525 line system. In place of the 31.5 kc (2H) pulse in the 405 system the 2H pulse becomes 20.25 kc.

1. Adjust the sweep so that three 20.25 kc pulses cover 10 cm on the oscilloscope. Replace the module in the machine and place the vertical advance module on the extender. Place the probe on No. 1 counter test point, TP1. One cycle of the 1st counter signal should be 10 cm wide. If not, adjust R58, "trim-pot", until the cycle measures 10 cm.

2. Press and hold the STABILITY TEST push-button, and rotate the STABILITY TEST control through its range. The width of the $\div 3$ cycle should not change.

3. Set the oscilloscope sweep so that nine of the first counter pulses cover 10 cm on the oscilloscope. Place the probe on the No. 2 counter test point, TP2. One cycle of the TP2 signal (from Q5, Q11) should be 10 cm wide. To obtain this it may be necessary to adjust "trim-pot", R60. If so, repeat step 2, this time observing the width of the TP2 signal, which should not vary.

4. Change the CRO sweep so that 3 of the $\div 9$ pulses cover 10 cm on the oscilloscope. Move the probe to the No. 3 counter test point, TP3. One cycle of the third counter signal should be 10 cm wide. If not, adjust "trim-pot", R62, and again perform the stability test for this counter.

5. Change the sweep so that 5 of the $\div 3$ pulses cover 10 cm on the CRO. Place the probe on the No. 4 counter test point, TP4. One cycle of the fourth counter should occupy 10 cm on the scope. If not, adjust the "trim-pot", R63, and perform the stability test.

6. Reconnect the collector of Q2 and perform the Stability Test of Counter Multivibrator as in first part of this section. If test results are good replace the module in the machine.

ADJUSTMENT OF COUNTERS (819)

The machine must be modified to work on 819 lines instead of 405 lines. The procedure for 819 lines is the same as for 405 but the counter numbers are different. Refer to the chart on the block diagram of the vertical advance module figure 152.

NOTES

1. Proper counter operation is necessary, but not sufficient, to insure proper vertical advance. In some cases proper counting may be obtained with the collector of Q2 disconnected; however, when the loop is closed again by reconnecting Q2, improper advance is obtained. This condition results from improper off-time width of one of the counters, usually the third counter (Q6, Q12). To detect the offending counter, locate the leading edge of the 3.5H pulse (which will be much wider than normal). The leading edge lines up with the turn-off edge of the offending counter. When the counter has been located, readjust its timing so as to lengthen its period. A point will be found where the counting chain jumps suddenly into proper operation. Continue to lengthen its period until the counter-chain holds to proper count throughout the entire range of the STABILITY TEST control.
2. A condition may occur in the Vertical Advance module in which a blanking bar is generated only on alternate fields, instead of on every field. This

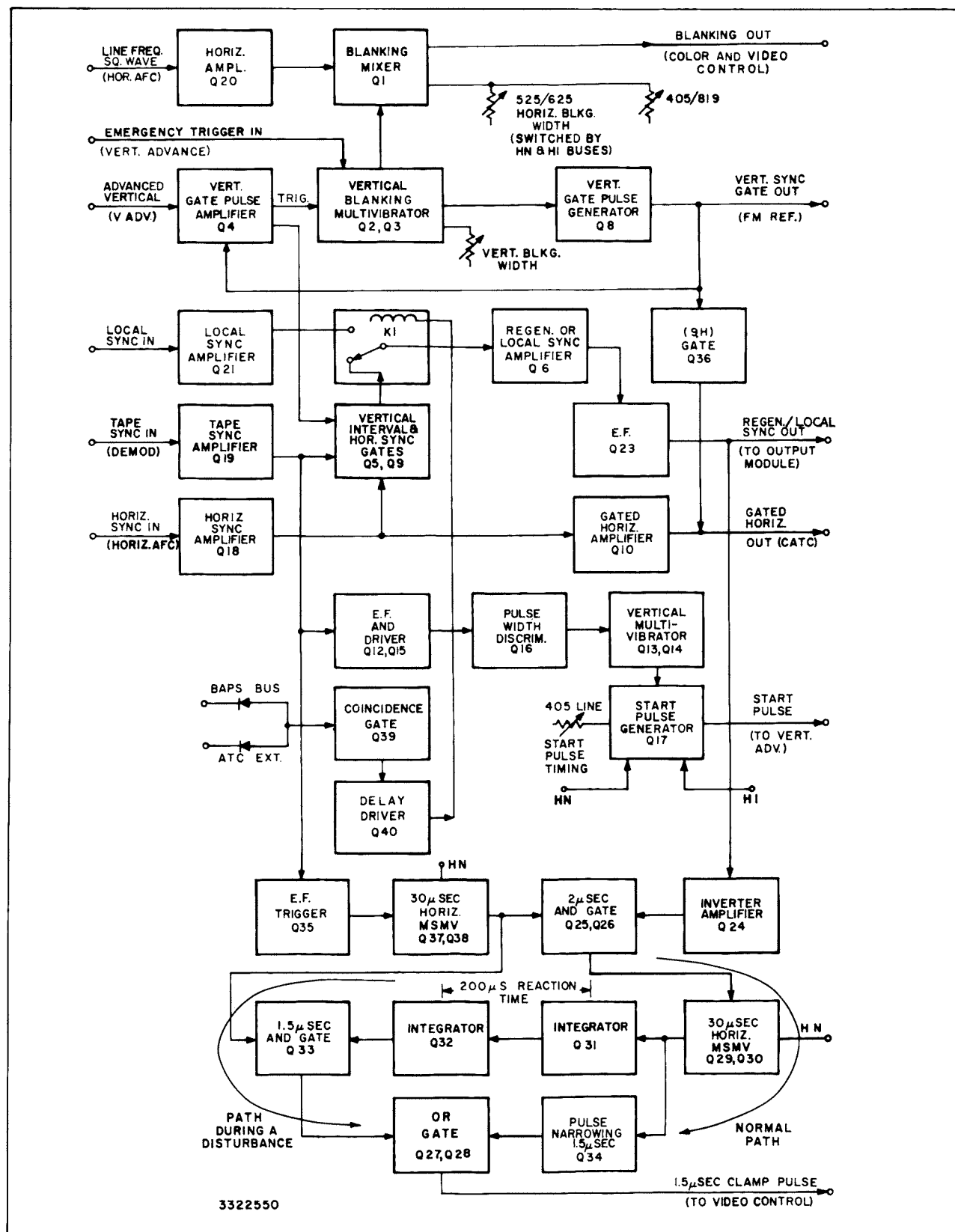


Figure 160—Block Diagram, Sync Logic Module

results from having the fourth counter adjusted for an excessively long time constant. The multivibrator cannot recover in time to be retriggered by the start pulse; therefore, it waits for one entire field before being retriggered. To eliminate this condition, simply readjust the fourth counter "trim-pot", (R52) to shorten the time constant, then check the final setting to be certain that the counter passes the STABILITY TEST.

3. Sometimes a condition occurs in which the Horizontal AFC module produces regenerated sync at 31.5 kc, instead of 15.75 kc. A common cause of this fault is a shorted regulator transistor (Q14) in the Vertical Advance module. A quick check for this fault can be made by measuring the -10 volt bus in the Vertical Advance module. If transistor Q14 is shorted, the bus is at a more negative potential than -10 volts.

SYNC LOGIC (Module 230)

In the following discussion the 525 line system will be discussed with appropriate notes or comments added to cover the 405, 625, and 819 line systems as required. The numbers in parentheses in the 525 line discussion indicate that these values will probably change for the other line standards, a few examples are given in the chart below and figure 160.

	525	405	625
Vert. Advance	3.5H	1.5H	3.0H
Vert. Gate	9.0H	4.0H	7.5H
Vert. Blanking	21H	15H	25H
2H	31.5KC	20.25KC	31.25KC

The Sync Logic module provides signals for the operation of the Vertical Advance module, as well as signals for the Video Control, Video Output and Color Modules. When triggered by the leading edge of the (3.5H) pulse, which is generated in the Vertical Advance module, the Sync Logic module regenerates the vertical blanking and reinserts the tape vertical sync interval. The signals supplied by this module include mixed blanking for the Video Control and the Color Processor module if the machine is equipped for color. A vertical sync gate pulse is supplied to the FM reference module for keying in crystal markers. Gated horizontal is supplied for use in color ATC. Regenerated or local sync is available for the Output module. (Local Sync is used only in Pixlock selected by relay K1.)

A start pulse is generated in this module for the Vertical Advance module, and a clamp pulse of 1.5 microseconds duration is generated which is used in the video control module (131).

Circuitry is provided in this module, shown in the lower part of the diagram, to ensure clamp pulses being produced during circuit disturbances. A disturbance can cause lack of coincidence in "And" gate Q25, Q26. If the trigger pulse from Q25, Q26 is not sufficient to drive MSMV Q29, Q30 the output will be taken from the monostable multivibrator Q37, Q38.

If coincidence is lost in "And" gate Q25, Q26 after 200 microseconds, signal is derived from "And" gate Q33. This signal then supplies a 1.5-microsecond pulse to "Or" gate Q27, Q28 which then passes clamp signal derived from tape sync to the Video Control module (131B). When the signal returns to normal, the path reverts to Q29, Q30 multivibrator, and Q34 "boxcar" pulse narrowing circuit.

The HN bus switching of the two monostable multivibrators Q29, Q30 and Q37, Q38 changes the 30-microsecond time to 50 microseconds for the 405 line system.

Vertical Blanking Generator

As shown in figure 161, the vertical blanking multivibrator, Q2, Q3, is a monostable multivibrator with Q2 on, Q3 off in the stable state. The multivibrator changes state by applying a positive trigger pulse to the base of Q2 through the isolation diode, CR3, from Q4 collector. The normal trigger for the vertical blanking multivibrator is the leading edge of (3.5H) pulse. Transistor Q2 remains off and Q3 on for the length of time determined by the charging time of capacitor C3 through resistors R7 and R52. The vertical blanking pulse width at the collector of Q3 is set to (21H) by adjustment of R7, the VERT BLKG WIDTH control.

The output of Q3 is coupled to the blanking mixer, Q1, through the isolation diode, CR2, and to the vertical gate pulse (9H) generator through R34 and C16. The (9H) generator, Q8, is a pulse-narrowing circuit. The (9H) pulse output from the collector of Q8 is coupled through the isolation diode, CR9, and combined with the (3.5H) pulse input signal. The combined pulses are then passed through R157 and C69 to the (9H) gate amplifier, Q36, and through R17 and C6 to the base of the vertical gate pulse (9H) amplifier, Q4. An output to the vertical interval gate, Q5, is taken from the emitter of Q4. (9H) gate E. F. Q36 feeds the horizontal sync gate, Q9 via R37 and C17.

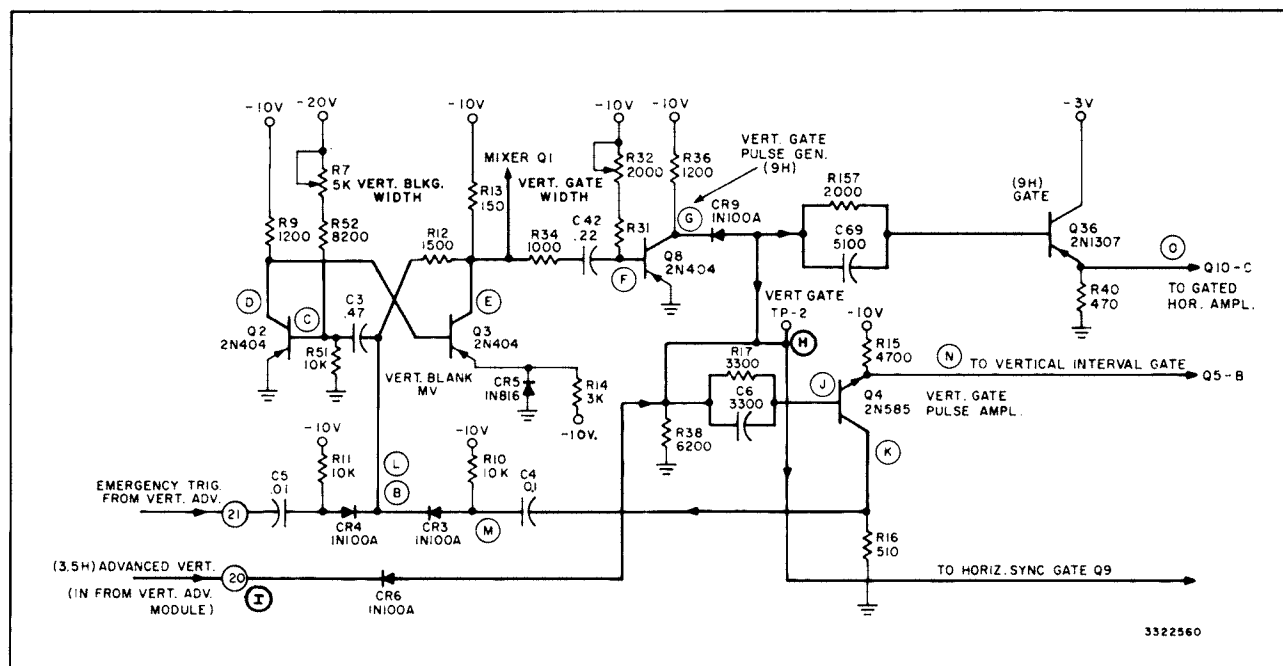


Figure 161—Vertical Blanking Multivibrator, Vertical Gate Pulse Generator and Vertical Gate Pulse Amplifier Circuits

Emergency Trigger

The normal trigger pulse for the vertical blanking multivibrator (Q2, Q3) is the leading edge of the (3.5H) pulse which is coupled to the base of Q2 through CR3 from the collector of the vertical gate pulse (9H) amplifier, Q4. The emergency trigger pulse is a positive going signal taken from the (÷3) multivibrator in the Vertical Advance module and appears simultaneously with the negative going edge (trailing edge) of the (3.5H) pulse at the base of Q2. During normal conditions of operation, this pulse has no effect on the vertical blanking multivibrator which has already been triggered by the leading edge of the (3.5H) pulse and remains in that state for (21H). However, under unusual operating conditions due to a non-synchronous switch or a bad splice in the tape, the vertical sync period of the tape sync signal may arrive at a much later time. As explained in the description of the Vertical Advance module, the leading edge of the (3.5H) pulse is generated exactly (259H) after the previous pulse, even though the vertical sync has been delayed. The trailing edge of the (3.5H) pulse is coincident with the second vertical sync pulse but since the second vertical sync pulse is delayed, the trailing edge of (3.5H) will be delayed. Therefore, the (3.5H) pulse will be much longer than (3.5H). This lengthened (3.5H) pulse holds the vertical interval gate, Q5, open, (figure 163) allowing tape sync to pass. When the vertical

sync does arrive, a start pulse is generated at the leading edge of the second vertical sync pulse, resulting in the termination of the lengthened (3.5H) pulse. This trailing edge of the lengthened pulse is negative going and does not trigger the vertical blanking multivibrator (Q2, Q3) which has returned to its stable state (21H) after the leading edge of the (3.5H) pulse.

If there were no emergency trigger, the vertical interval gate, Q5, would close, cutting off the remainder of the vertical interval. However, the positive going emergency trigger coincident with the trailing edge of the lengthened (3.5H) pulse does trigger the vertical blanking multivibrator which in turn triggers the vertical gate pulse (9H) generator, Q8. The (9H) pulse holds the vertical interval gate open for the remainder of the vertical interval, minimizing the "roll" in the picture.

Sync Reassembly

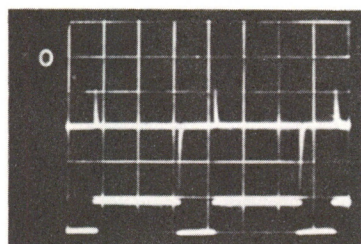
In the reassembly of sync, the (3.5H) pulse (which originates in the Vertical Advance module) is added to the (9H) pulse at both the output of the vertical gate pulse generator, Q8, and at the input to the vertical gate pulse amplifier, Q4 (see figure 161).

The (3.5H) and (9H) combined signal appearing at the junction of CR9, C69, and R157 is fed to the horizontal sync gate, Q9, and the similarly combined

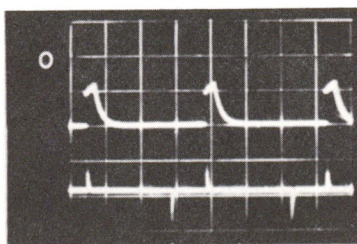
signal from the emitter of Q4 is fed to Q5, the vertical interval gate (see figure 163).

Normally, transistor Q5 is biased to saturation, shorting out the tape sync pulses which appear at its collector while transistor Q9 is biased to cut off. In this state, the regenerated horizontal sync pulses appearing at the collector of Q9 are applied to the base

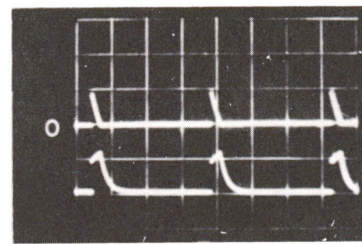
of the regenerated sync amplifier, Q6, through isolation diode CR10, and relay K1. During the vertical interval, the (9H) pulse applied to the base of Q5 drives it to cutoff, which permits the tape sync pulses to pass through the isolation diode, CR7, to the base of Q6. Diode CR14 sets the positive going excursion of the tape sync signal at $-3V$. Capacitor C37 is a



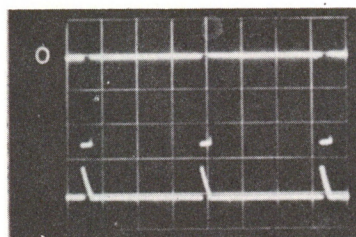
A. Top: R11, C5, CR4, 5 ms/cm, 5v/cm
Bottom: C5 input, 5 ms/cm, 10v/cm



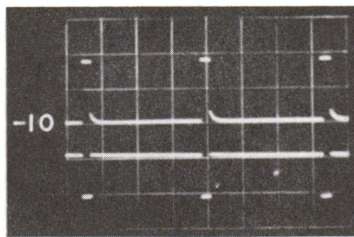
B. Top: CR4, CR3, C3, R12, 5 ms/cm, 5v/cm
Bottom: R11, C5, CR4, 5 ms/cm, 10v/cm



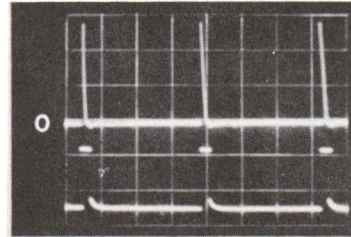
C. Top: Q2 base, 5 ms/cm, 5v/cm
Bottom: CR4, CR3, C3, R12, 5 ms/cm, 5v/cm



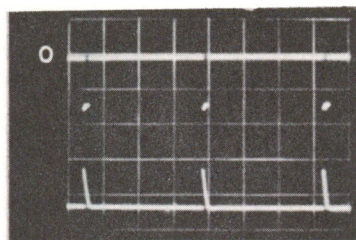
D. Top: Q2 collector, 5 ms/cm, .5v/cm
Bottom: Q2 base, 5 ms/cm, 5v/cm



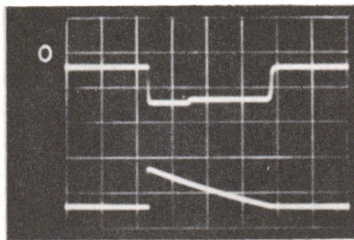
E. Top: Q3 collector, 5 ms/cm, 5v/cm
Bottom: Q3 base, 5 ms/cm, 1v/cm



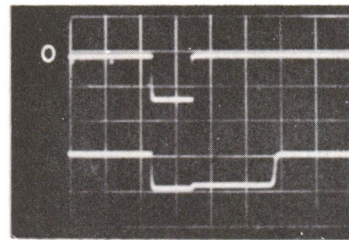
F. Top: Q8 base, 5 ms/cm, 2v/cm
Bottom: Q3 collector, 5 ms/cm, 5v/cm



G. Top: Q28 collector, 5 ms/cm, 5v/cm
Bottom: Q8 base, 5 ms/cm, 5v/cm



H. Top: TP2, 200 μ s/cm, 5v/cm
Bottom: Q8 base, 200 μ s/cm, 5v/cm



I. Top: CR6 input, 200 μ s/cm, 5v/cm
Bottom: TP2, 200 μ s/cm, 5v/cm

Figure 162—Typical Waveforms; Vertical Blanking Multivibrator, Vertical Gate Pulse Generator and Vertical Gate Pulse Amplifier Circuits

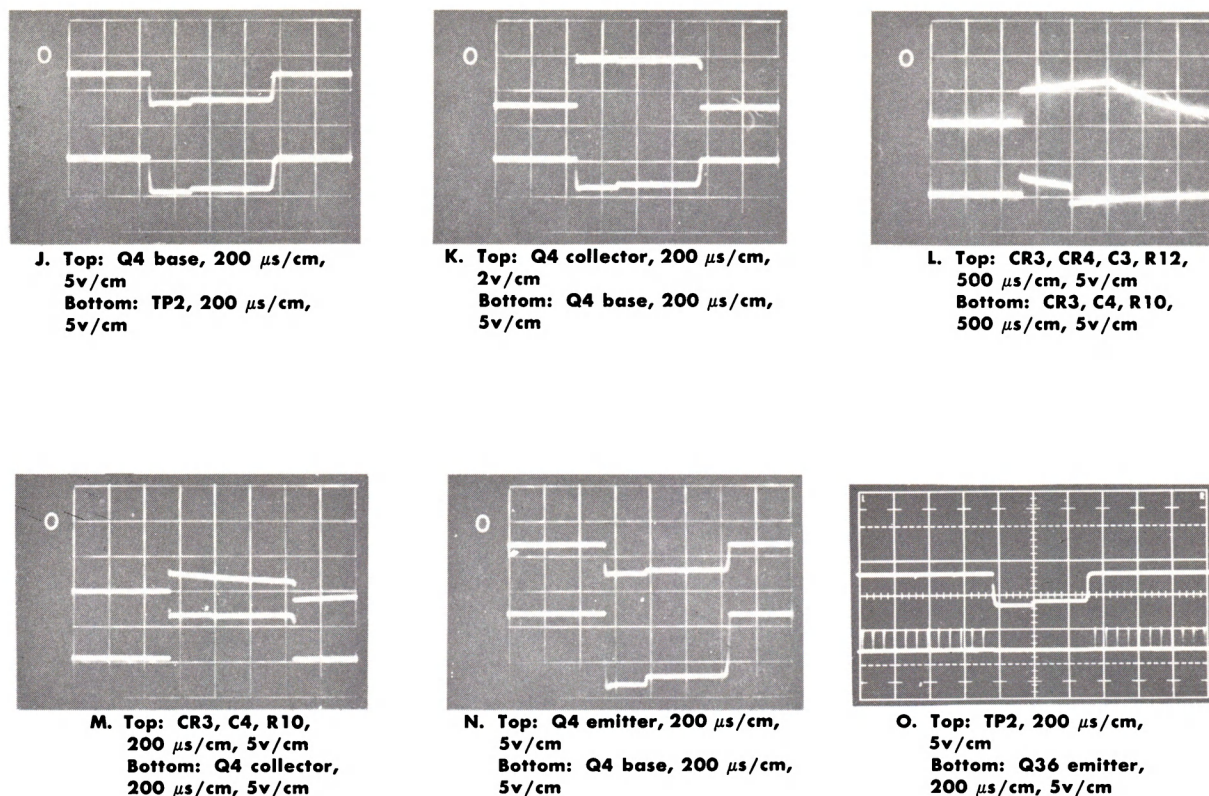


Figure 162—Typical Waveforms; Vertical Blanking Multivibrator, Vertical Gate Pulse Generator and Vertical Gate Pulse Amplifier Circuits (Continued)

“speedup” capacitor for making faster rise times or steeper edges of the pulses. The (9H) pulse applied to the base of Q9 drives it into saturation and shorts out the regenerated horizontal pulses. During the vertical sync interval, the pulses at the base of Q6 are tape sync and during the rest of the period, regenerated horizontal sync pulses. These pulses are amplified by transistor Q6 and isolation is provided by Q23, emitter follower to provide regenerated sync for the Video Output module and for the integrator driver, Q7. Diode CR8 together with R22, R94, and C11 prevents transistor Q6 from being driven into saturation. A divider R28, R29 provides a -3 volt bias which insures that Q6 will be cut off in the absence of a pulse input. Regenerated horizontal sync pulses from the horizontal sync clipper Q12 in the horizontal AFC module are fed to the base of Q18. Q18 is an emitter follower horizontal sync amplifier, the output of which goes to two places. One of these feeds, Q10, gated horizontal amplifier. The output at collector of Q10 is clamped by the (9H) vertical sig-

nal fed from Q36 emitter. This eliminates horizontals during the (9H) period. The output of Q10 collector is supplied to the color processor module, if used, and is required for burst gating.

The other portion of the Q18 output goes to the collector of Q9. Diode CR34, like diode CR14, sets the positive excursion of the signal at $-3V$. The negative part of the signal goes to -10 volts. The network of R20, CR35, R68 and C10 is used as a pulse widening circuit. Capacitor C10 is effectively switched into the circuit for “speed up” on the leading edge by diode CR35 but it disconnects C10 for the trailing edge. This produces a waveform with a slope on the trailing edge which widens the pulse. This is used to effect an advance of the gated regenerated sync. The advance is required because of the 0.55 microsecond delay in the monochrome path in the video output module (233B), and the color requirement to adjust the “breezeway” between horizontal sync and burst. With this arrangement by

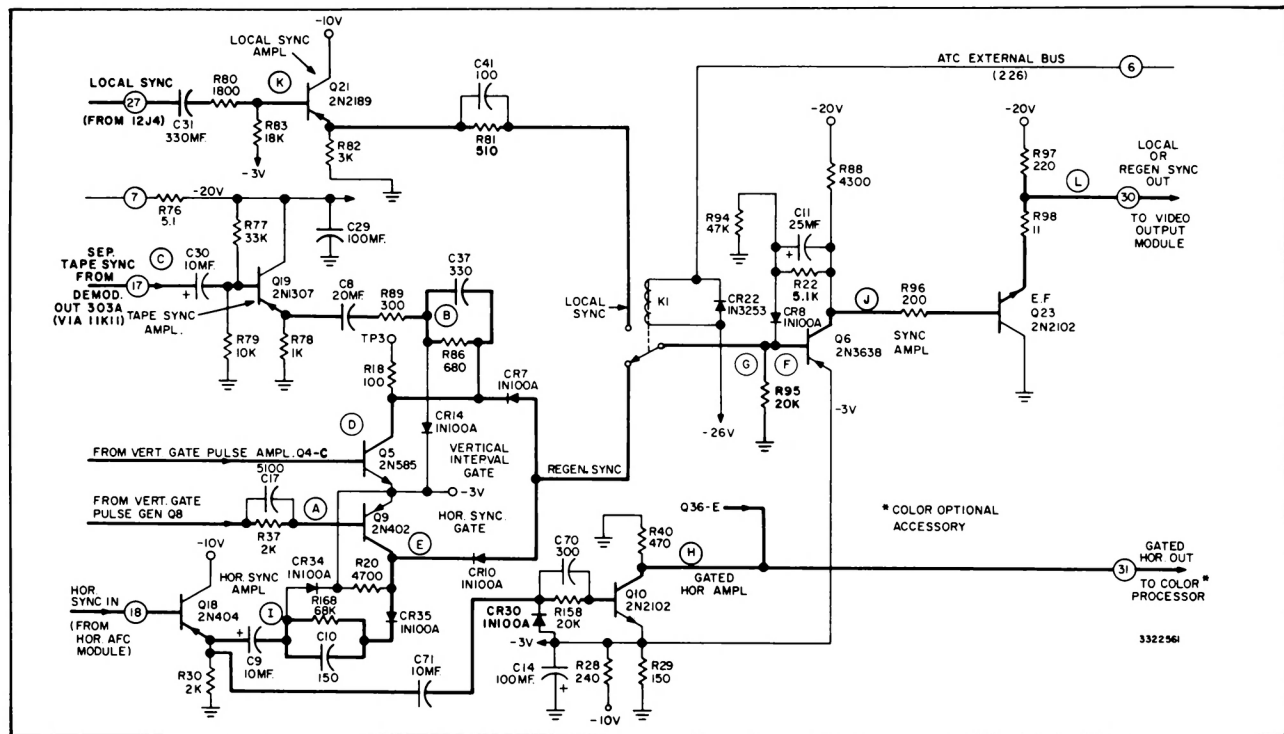


Figure 163—Vertical Interval Gate, Horizontal Sync Amplifier, Horizontal Sync Gate, Regenerated Sync Amplifier and Gated Horizontal Amplifier Circuits

proper adjustment of horizontal sync width, the "breezeway" can be reduced to zero although it normally is not set at this point.

Start Pulse

Incoming tape sync from the Horizontal AFC module is used to generate the start pulse (see figure 165). The input is a 4-volt peak-to-peak negative signal which is applied to the base of Q12, an emitter fol-

lower. The latter is used as a unity gain amplifier for isolation purposes. The output appearing on the emitter of Q12 is the same polarity as the input, therefore the signal fed to the base of Q15, the driver, is negative also.

Transistor Q12 is normally cut off and Q15 is normally saturated so that C21 returns to -10 volts through the emitter-base junction of Q15. When there is no signal present on the emitter of Q12, the

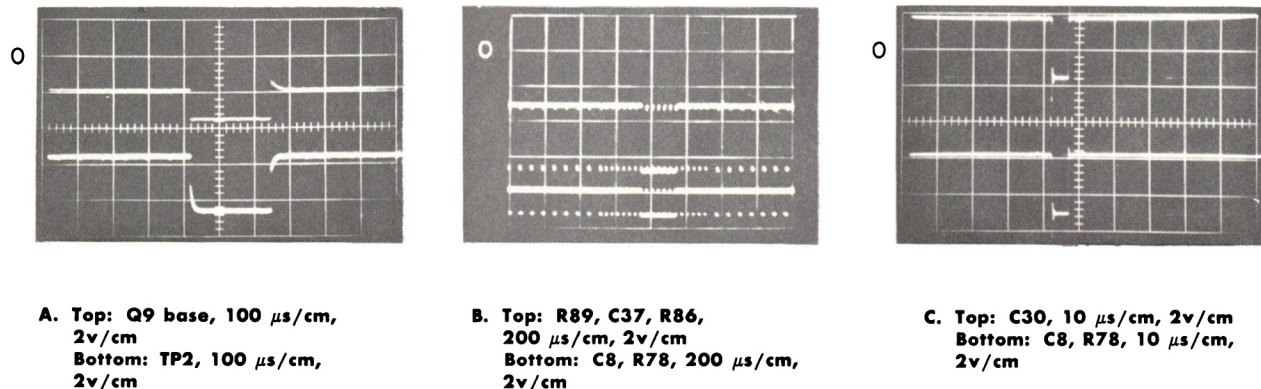


Figure 164—Typical Waveforms; Vertical Interval Gate, Horizontal Sync Amplifier, Horizontal Sync Gate, Regenerated Sync Amplifier and Gated Horizontal Amplifier Circuits

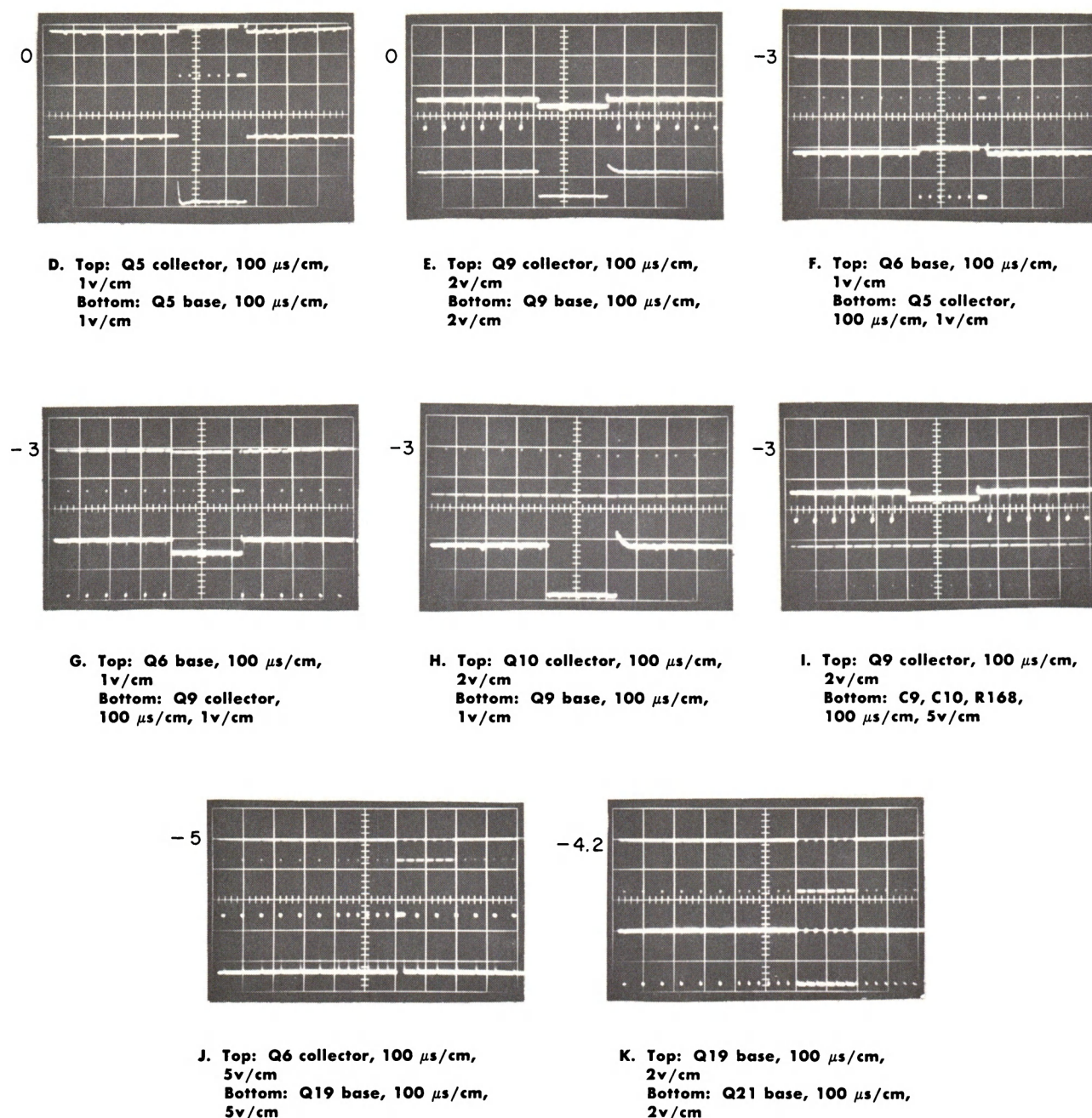


Figure 164—Typical Waveforms; Vertical Intergal Gate, Horizontal Sync Amplifier, Horizontal Sync Gate, Regenerated Sync Amplifier and Gated Horizontal Amplifier Circuits (Continued)

capacitor is charged to -10 volts through R55. The time constant of C21 and R55 is such that C21 will discharge completely when there is a negative pulse on the emitter of Q12. During the horizontal sync and the equalizing pulse intervals there is ample time between successive pulses for C21 to return to its fully charged state. However, during vertical sync, the time between successive pulses is very short and C21 is not able to recover from its discharged state before

the next negative pulse arrives. After the second negative pulse, C21 recharges to a lower level than after the first negative pulse. The recharging of C21 after successive negative pulses continues to become progressively less so that the recovery pulses (serrations) become progressively smaller. This signal appears on the base of Q15, where the dc level now is shifted to -10 volts; otherwise the signal is not altered. The negative pulses arriving on the base of Q15 cut off

this transistor, while simultaneously generating positive pulses on the collector.

The positive sync output from the collector of Q15 goes simultaneously to the emitter and the base of Q16, the pulse width discriminator. The input to the emitter is direct coupled; the input to the base is passed through the differentiating network, C24, R57, R58.

The RC time constant of the differentiator in the base of Q16 is such that the duration of the capacitor discharge is longer during the horizontal and the equalizing pulse intervals than the duration of these pulses on the emitter. Therefore the pulses on the base keep Q16 cut off. Compared to the duration of the vertical sync pulses, however, the time constant of the differentiator is short. Therefore, when vertical sync arrives, the capacitor discharges before the end of the pulse, but the emitter still sees the trailing edge of the positive pulse. Thus the emitter is more positive than the base during the remainder of the pulse and the transistor conducts. Simultaneously on the collector of Q16 several positive pulses are generated to correspond to the first few vertical sync pulses.

This positive vertical output signal is passed through a differentiator, and then applied to the base of Q13. Transistor Q13 in conjunction with Q14 forms the vertical multivibrator which is the monostable type. The RC time constant of the differentiator permits only the differentiated trailing (negative) edge of the first pulse to trigger the vertical multivibrator. The vertical multivibrator generates a positive output pulse which is fed through a differentiator comprised of C25, R33 and variable resistor R100 and then applied to the base of Q17, the start pulse generator.

A bilateral transistor, which serves as either a pulse narrowing amplifier (boxcar) or an emitter follower, is used for the start pulse generator. The configuration it assumes depends upon the potential applied to the HI and HN busses and this, in turn, is determined by the standards selector switch. On 525- and 625-line standards, Q17 is an emitter follower. On 405-line standards, Q17 is a pulse narrowing amplifier or boxcar, and the potentials on the HI and HN busses are reversed.

Variable resistor R100 in the differentiator in the

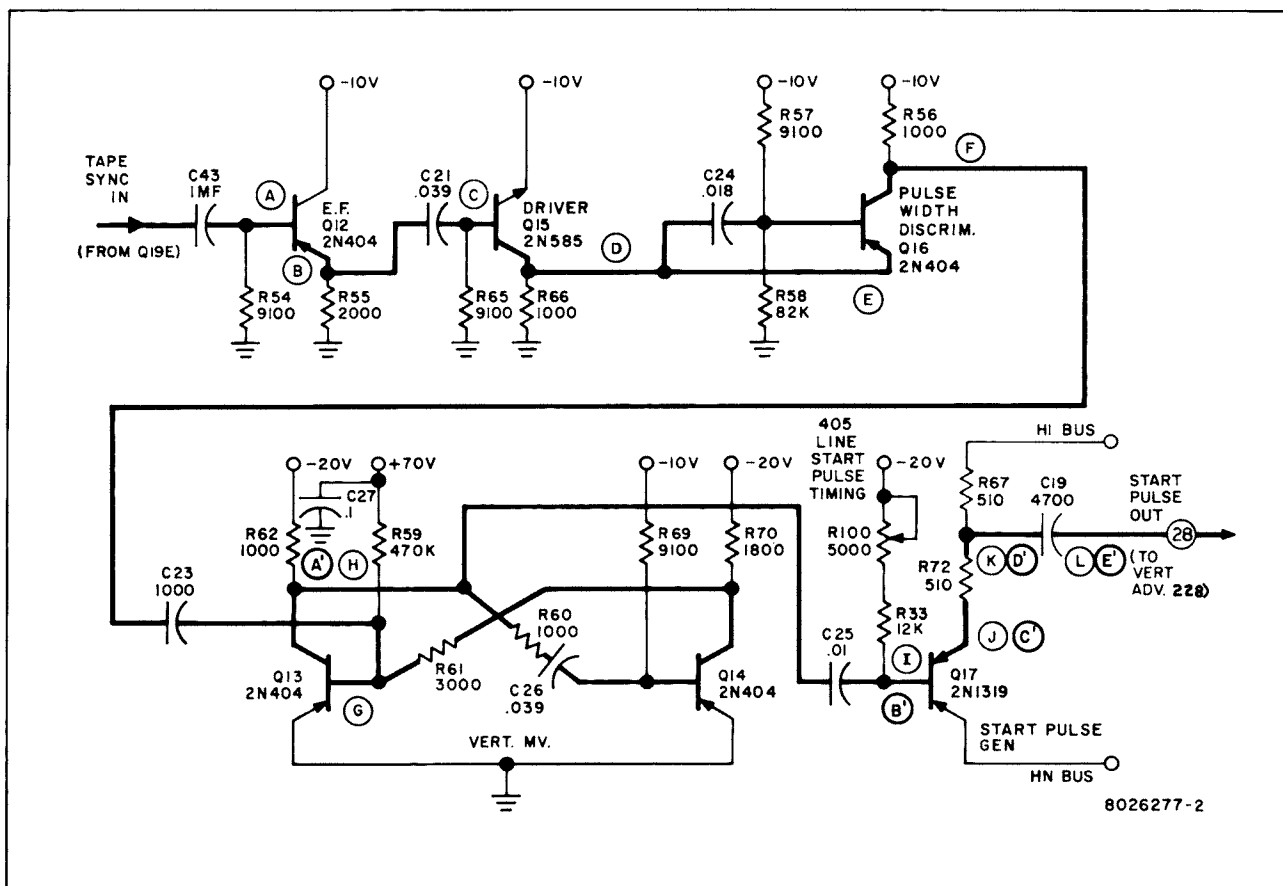
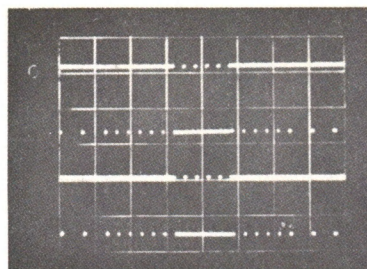
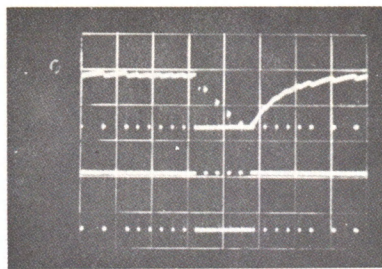


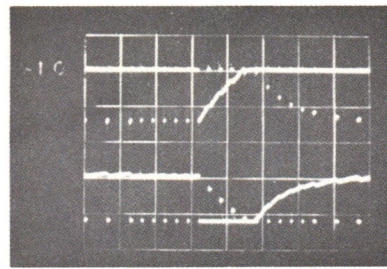
Figure 165—405- and 625-Line Standards Start Pulse Generator Circuits



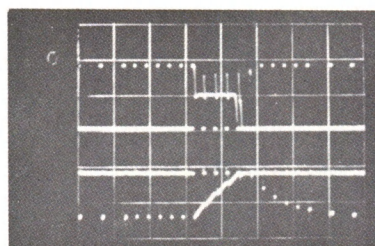
A. Top: Q12 base, 100 μ s/cm, 2v/cm. Bottom: tape sync in, 100 μ s/cm, 2v/cm



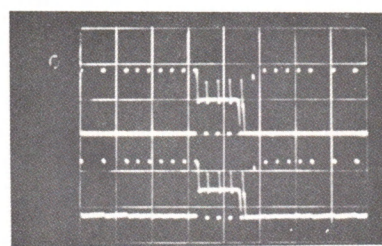
B. Top: Q12 emitter, 100 μ s/cm, 2v/cm. Bottom: Q12 base, 100 μ s/cm, 2v/cm



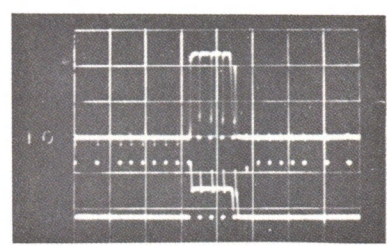
C. Top: Q15 base, 100 μ s/cm, 2v/cm. Bottom: Q12 emitter, 100 μ s/cm, 2v/cm



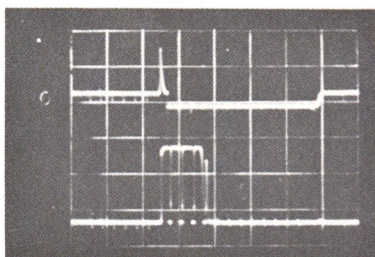
D. Top: Q15 collector/Q16 emitter, 100 μ s/cm, 5v/cm. Bottom: Q15 base, 100 μ s/cm, 2v/cm



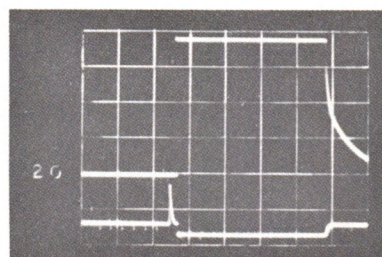
E. Top: Q16 emitter, 100 μ s/cm, 5v/cm. Bottom: Q16 base, 100 μ s/cm, 5v/cm



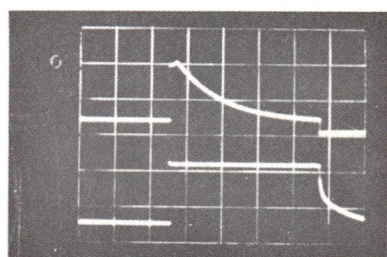
F. Top: Q16 collector, 100 μ s/cm, 2v/cm. Bottom: Q16 emitter, 100 μ s/cm, 5v/cm



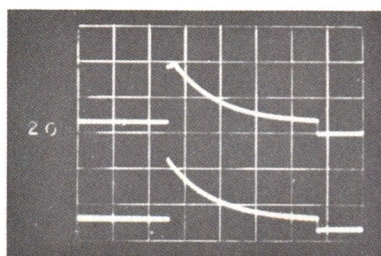
G. Top: Q13 base, 100 μ s/cm, 2v/cm. Bottom: Q16 collector, 100 μ s/cm, 2v/cm



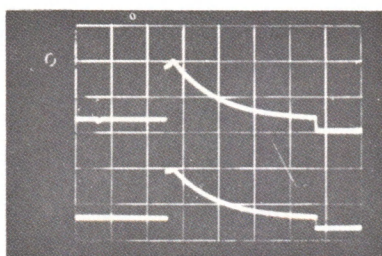
H. Top: Q13 collector, 100 μ s/cm, 5v/cm. Bottom: Q13 base, 100 μ s/cm, 2v/cm



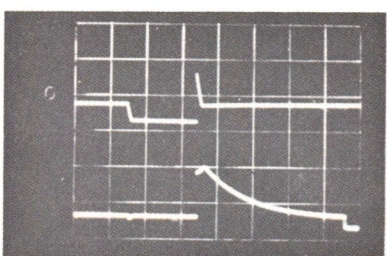
I. Top: Q17 base, 100 μ s/cm, 10v/cm. Bottom: Q13 collector, 100 μ s/cm, 10v/cm



J. Top: Q17 emitter, 100 μ s/cm, 10v/cm. Bottom: Q17 base, 100 μ s/cm, 10v/cm

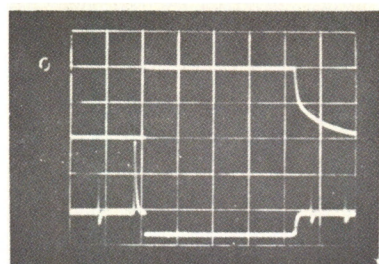


K. Top: R67, R72, 100 μ s/cm, 5v/cm. Bottom: Q17 emitter, 100 μ s/cm, 10v/cm

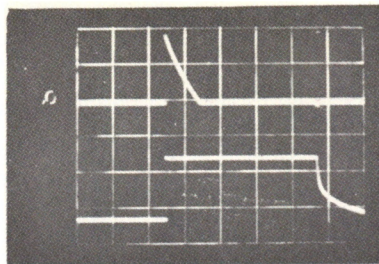


L. Top: Start pulse out, 100 μ s/cm, 5v/cm. Bottom: R67, R72, 100 μ s/cm, 5v/cm

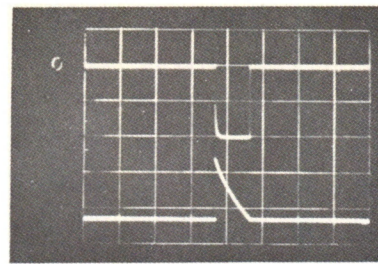
Figure 166—Typical Waveforms; 405- and 625-Line Standards Start Pulse Generator Circuits



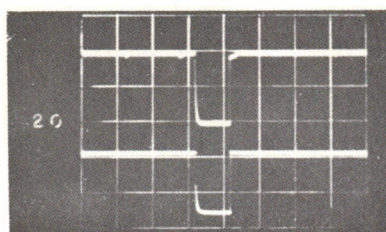
A.¹ Top: Q13 collector,
100 μ s/cm, 10v/cm
Bottom: Q13 base,
100 μ s/cm, 1v/cm



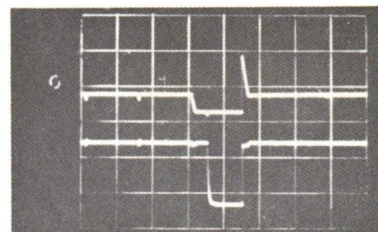
B.¹ Top: Q17 base,
100 μ s/cm, 10v/cm
Bottom: Q13 collector,
100 μ s/cm, 10v/cm



C.¹ Top: Q17 emitter,
100 μ s/cm, 10v/cm
Bottom: Q17 base,
100 μ s/cm, 10v/cm



D.¹ Top: R67, R72,
100 μ s/cm, 5v/cm
Bottom: Q17 emitter,
100 μ s/cm, 10v/cm



E.¹ Top: Start pulse out,
100 μ s/cm, 5v/cm
Bottom: R67, R72,
100 μ s/cm, 5v/cm

**Figure 166—Typical Waveforms; 405- and 625-Line Standards
Start Pulse Generator Circuits (Continued)**

base of Q17 is used to fix the timing of the trailing edge of the 405-line start pulse. Since there are no equalizing pulses in the 405-line signal, this resistor is adjusted to set the RC time constant so that the positive going leading edge of the 405-line start pulse occurs during the third vertical serration interval. Resistor R100 has no influence on the RC time constant in producing the 525/625 line start pulse, since on this line standard it is the positive going leading edge that is used as the trigger. The timing of the start pulses is illustrated in figure 168.

The output of the start pulse generator is differentiated, and the resulting positive pulse is fed to the base of Q8, the start pulse amplifier in the Vertical Advance module 228A. Here, on the base of Q8, the start pulse and the output of the vertical advance pulse amplifier, Q9, are combined as the input to the start pulse amplifier.

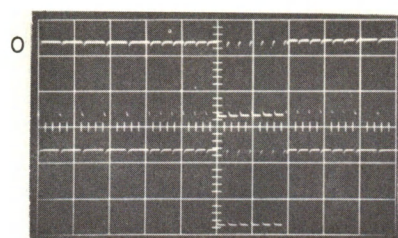
Blanking Mixer

Another output provided by this module is blank-

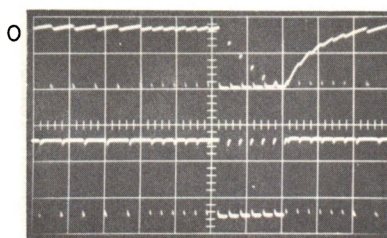
ing. As shown in the simplified schematic, figure 169 and waveforms diagram figure 170, the 15.75 kc square wave input from the Horizontal AFC module is coupled through the isolation emitter follower Q20, to the blanking mixer, Q1. The Q1 circuit is the pulse narrowing type.

The HN-HI switchable time constant of C20, R49, R50, etc., in the base circuit of the blanking mixer, Q1, is adjustable and is set to provide horizontal blanking pulses of approximately eleven microsecond-duration by the HOR BLKG WIDTH control, on 525- or 625-lines, or 18 microseconds on 405. The vertical blanking pulse from the multivibrator, Q2, Q3, is coupled directly to the base of Q1 through the isolation diode, CR2. During the (21H) vertical blanking period, Q1 is cut off, thereby generating the vertical blanking pulse and presenting the generation of horizontal blanking pulses. The output at the collector of Q1 is a composite horizontal and vertical blanking signal.

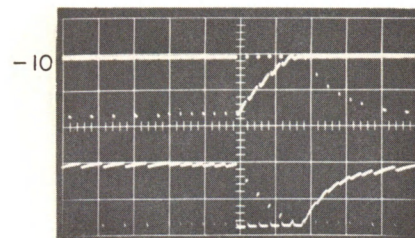
In the horizontal blanking circuit the time con-



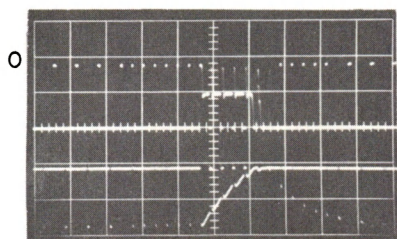
**A. Top: Q12 base, 100 μ s/cm, 2v/cm
Bottom: tape sync in, 100 μ s/cm, 2v/cm**



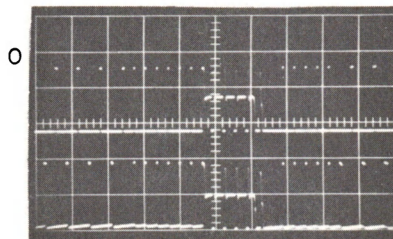
**B. Top: Q15 base, 100 μ s/cm, 2v/cm
Bottom: Q12 base, 100 μ s/cm, 2v/cm**



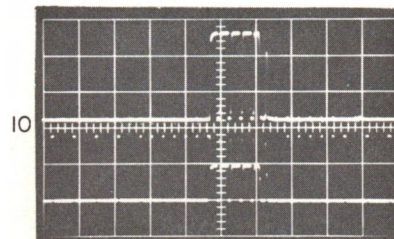
**C. Top: Q15 base, 100 μ s/cm, 2v/cm
Bottom: Q12 emitter, 100 μ s/cm, 2v/cm**



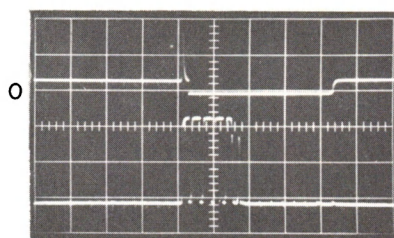
**D. Top: Q15 collector/Q16 emitter, 100 μ s/cm, 5v/cm
Bottom: Q15 base, 100 μ s/cm, 2v/cm**



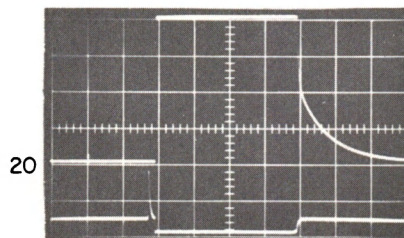
**E. Top: Q16 emitter, 100 μ s/cm, 5v/cm
Bottom: Q16 base, 100 μ s/cm, 5v/cm**



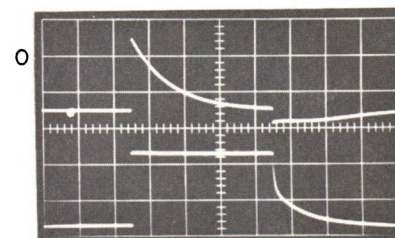
**F. Top: Q16 collector, 100 μ s/cm, 2v/cm
Bottom: Q16 emitter, 100 μ s/cm, 5v/cm**



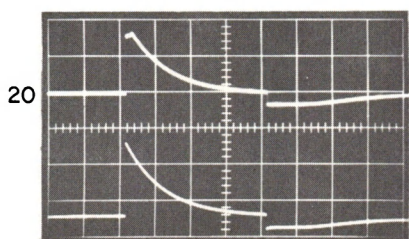
**G. Top: Q13 base, 100 μ s/cm, 2v/cm
Bottom: Q16 collector, 100 μ s/cm, 2v/cm**



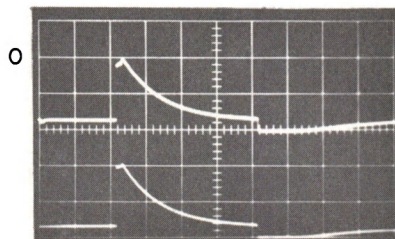
**H. Top: Q13 collector, 100 μ s/cm, 5v/cm
Bottom: Q13 base, 100 μ s/cm, 2v/cm**



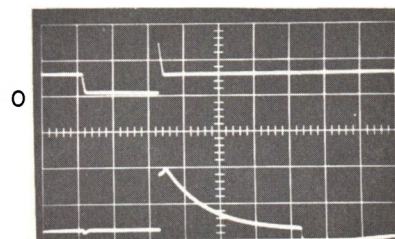
**I. Top: Q17 base, 100 μ s/cm, 10v/cm
Bottom: Q13 collector, 100 μ s/cm, 10v/cm**



**J. Top: Q17 emitter, 100 μ s/cm, 10v/cm
Bottom: Q17 base, 100 μ s/cm, 10v/cm**



**K. Top: R67, R72, 100 μ s/cm, 5v/cm
Bottom: Q17 emitter, 100 μ s/cm, 10v/cm**



**L. Top: Start pulse out, 100 μ s/cm, 5v/cm
Bottom: R67, R72, 100 μ s/cm, 5v/cm**

Figure 167—Typical Waveforms; 525-Line Standards Start Pulse Generator Circuits

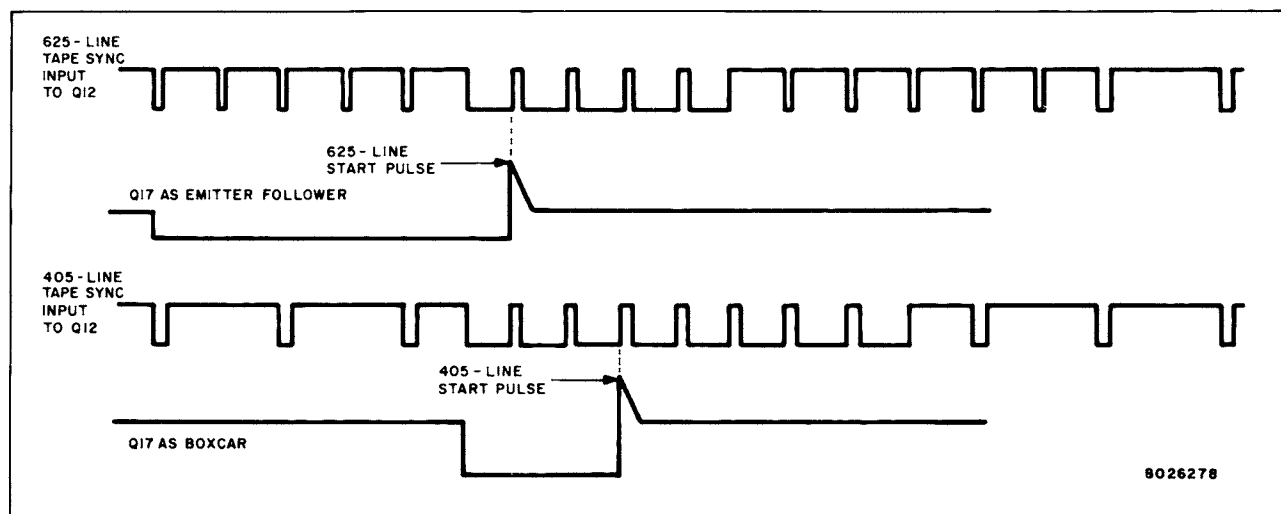


Figure 168—Timing of 405- and 625-Line Start Pulse

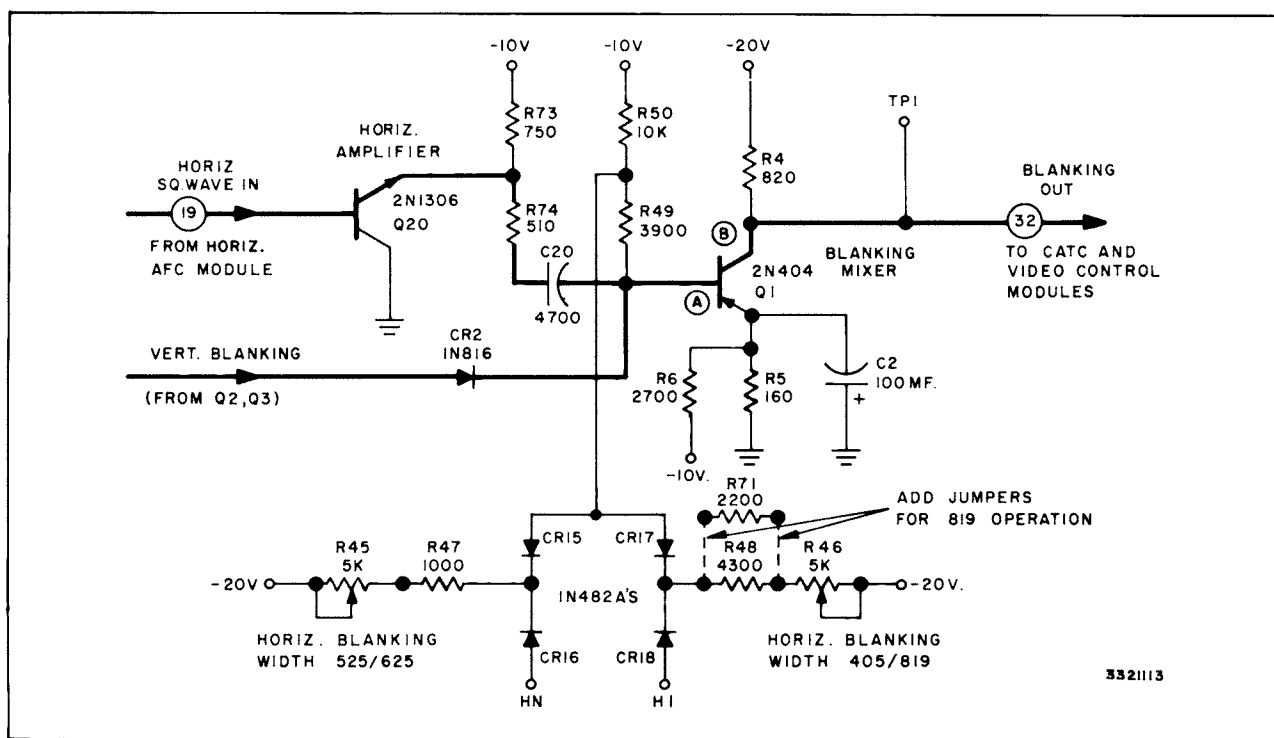


Figure 169—Blanking Mixer Circuit

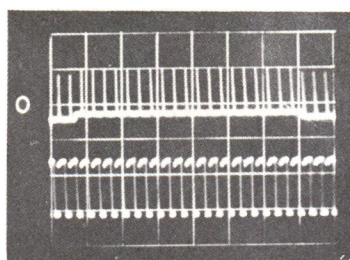
stants are switchable. The 525- and 625-line standards use the same time constants, but separate components accommodate the 405-line standard, since it requires a different RC time constant. The time constants are electronically switched into the circuit through the HN and HI busses. The desired standard is selected by means of the TV STANDARDS switch, which is located on the Vertical Advance module, (228A).

In 525- or 625-lines, the HN bus activates the additional path through R47 and R45. In the case of 405

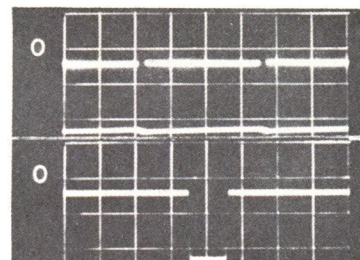
or 819 lines the HI bus goes to -20V , selecting R48 (R71) and R46 for the active control.

CLAMP PULSE GENERATING CIRCUITS

The purpose of the clamp pulse generating circuits is to select during normal operation the regenerated sync pulse (from the Horizontal AFC module 227B) for generating the video clamp pulse; or during time of signal disturbances to select the tape sync pulse for generating the video clamp pulse, and when the



**A. Top: Q1 base, 200 μ s/cm,
5v/cm
Bottom: Q20 base, 200 μ s/cm,
5v/cm**



**B. Top: Q1 collector,
500 μ s/cm, 5v/cm, vert rate
Bottom: Q1 collector,
10 μ s/cm, 5v/cm, hor. rate**

Figure 170—Typical Waveforms; Blanking Mixer Circuit

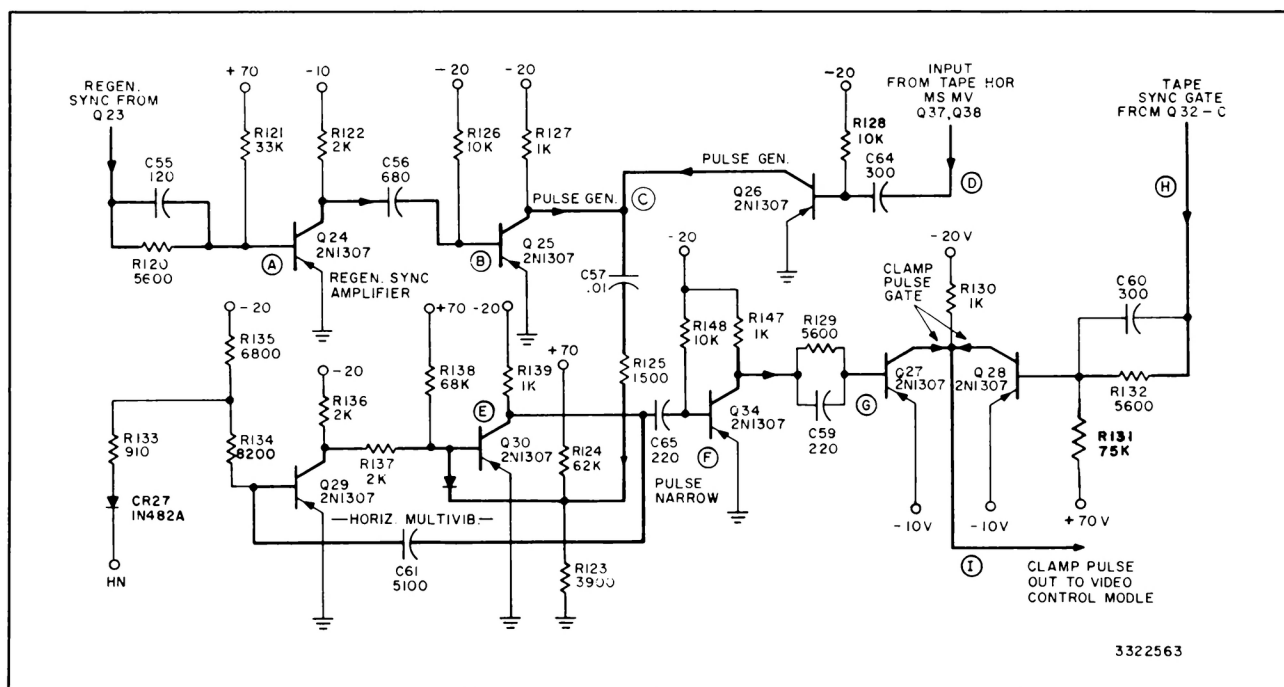


Figure 171—Clamp Pulse Generating Circuits, Regenerated Sync Clamp Pulse Generator and Horizontal MV

disturbance ends, to revert back to the regenerated sync pulse.

Since any signal disturbances present will also be present on the tape sync signal, any change in clamping level will be eliminated.

Under normal operation the regenerated sync signal is applied to the base of inverter-amplifier Q24. Refer to figures 160 and 171. The output signal of Q24 is applied to the base of Q25 which forms part of a 2 μ sec coincidence AND gate. The tape sync sig-

nal from Horiz MSMV Q37 and Q38 is applied to the base of Q26, also part of the 2 μ sec AND gate. When both sync signals are time-coincident (within 2 μ sec) AND gate Q25 and Q26 is enabled, thus triggering MSMV Q29 and Q30. The output from MSMV Q29 and Q30 is divided into two paths; one path is to integrator Q31, and the other is to a pulse-narrowing circuit composed of Q34, C65, R148 and fed via C59 and R129 to the base of Q27. Q27 and Q28 form an OR gate circuit which couples the regenerated sync to the video control module 131B.

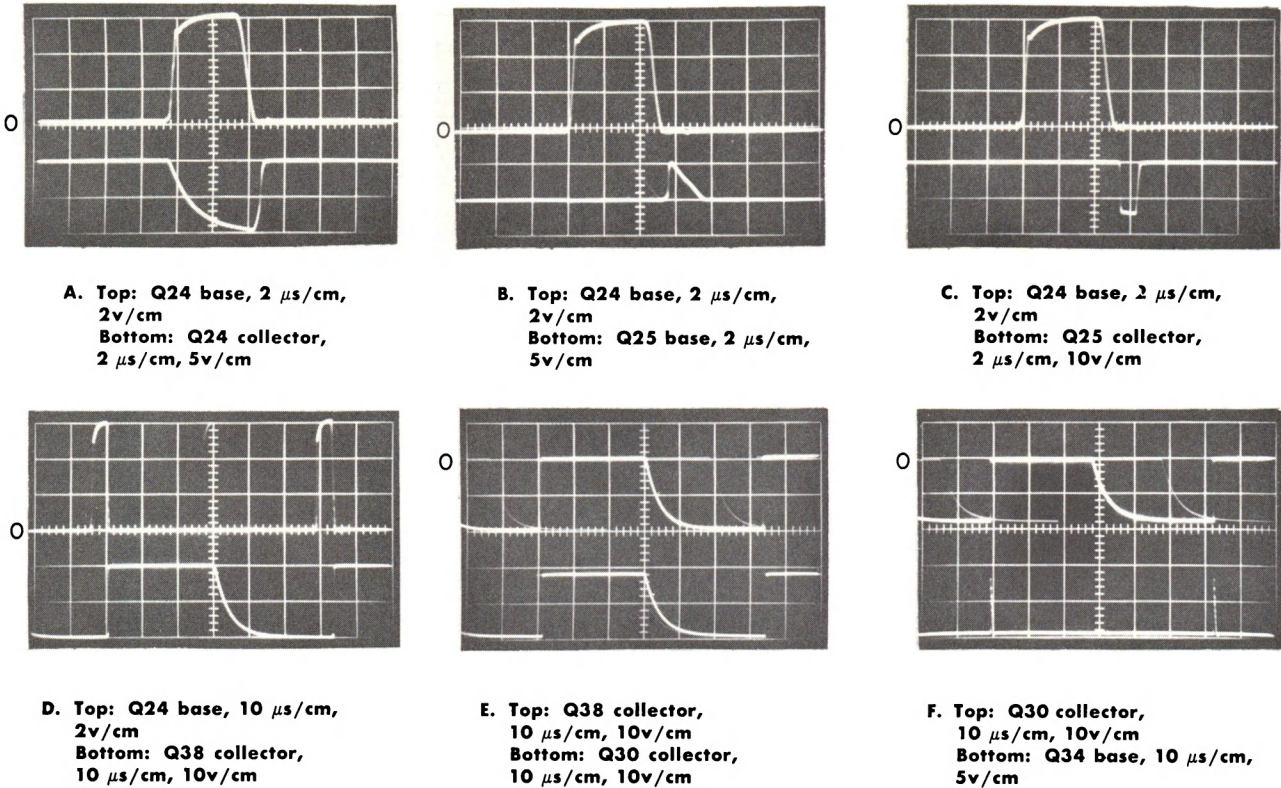


Figure 172—Typical Waveforms; Clamp Pulse Generating Circuits, Regenerated Sync Clamp Pulse Generator and Horizontal MV

When a signal disturbance is encountered and no signal coincidence occurs at AND gate Q25 and Q26, MSMV Q28 and Q29 is not triggered. Tape sync is now used to generate the clamp pulse. Refer to figures 173 and 174. Since MSMV Q28 and Q29 is not triggered, this allows C62 in the integrator network to discharge after 200 μ sec and cause Q31 (a dc-switch) to conduct (refer to figure 175 waveform B). This enables 1.5 μ sec AND gate Q32 and Q33. The output pulse from AND gate Q32 and Q33 is fed to OR gate Q27 and Q28. The output pulse of OR gate Q27 and Q28 is sent to the video control module 131B.

When the disturbance is not present, AND gate Q32 and Q33 is not enabled, and regenerated sync again is sent to the video control module 131B.

ADJUSTMENTS

To obtain the proper horizontal and vertical blanking width, connect an oscilloscope to one of the five VID test jacks (TP1, TP2, TP3, TP4, TP5) on the front of the Video Output module and make the following adjustments. (Machine can be in STOP and DEMOD Switch in the MOD. position, with normal input signal.)

Horizontal Blanking Width

1. Select proper line standard on module 228.
2. Adjust the oscilloscope to display a single horizontal blanking interval.
3. Adjust the appropriate HOR BLKG WIDTH control, (R45) for 525/625, (R46) for 405 or 819 lines, on the front of the Sync Logic module for a horizontal blanking width as follows:
 - 11 microseconds for 525.
 - 11.9 microseconds for 625.
 - 18 microseconds for 405.

Vertical Blanking Width

1. Using delayed sweep and external sync (or 3.5H) as a trigger, adjust the oscilloscope to display the vertical blanking interval.
2. Adjust the VERT BLKG WIDTH control (R7) on the front of the Sync Logic module for a vertical blanking width of 1250 microseconds, for 525; 1290 μ sec, for 625; or 1425 μ sec for 405-lines.

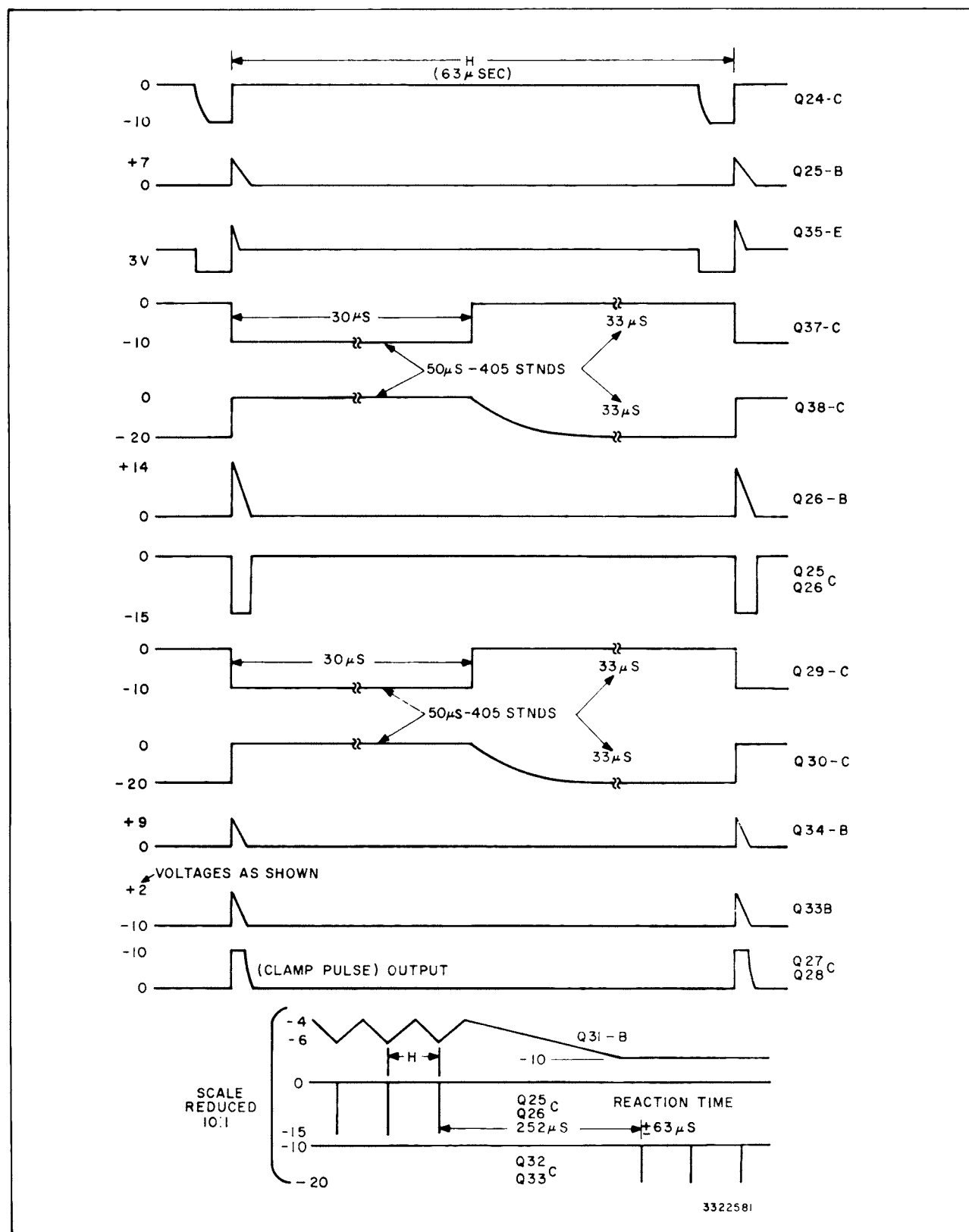


Figure 173—Timing Diagram; Clamp Pulse Circuitry

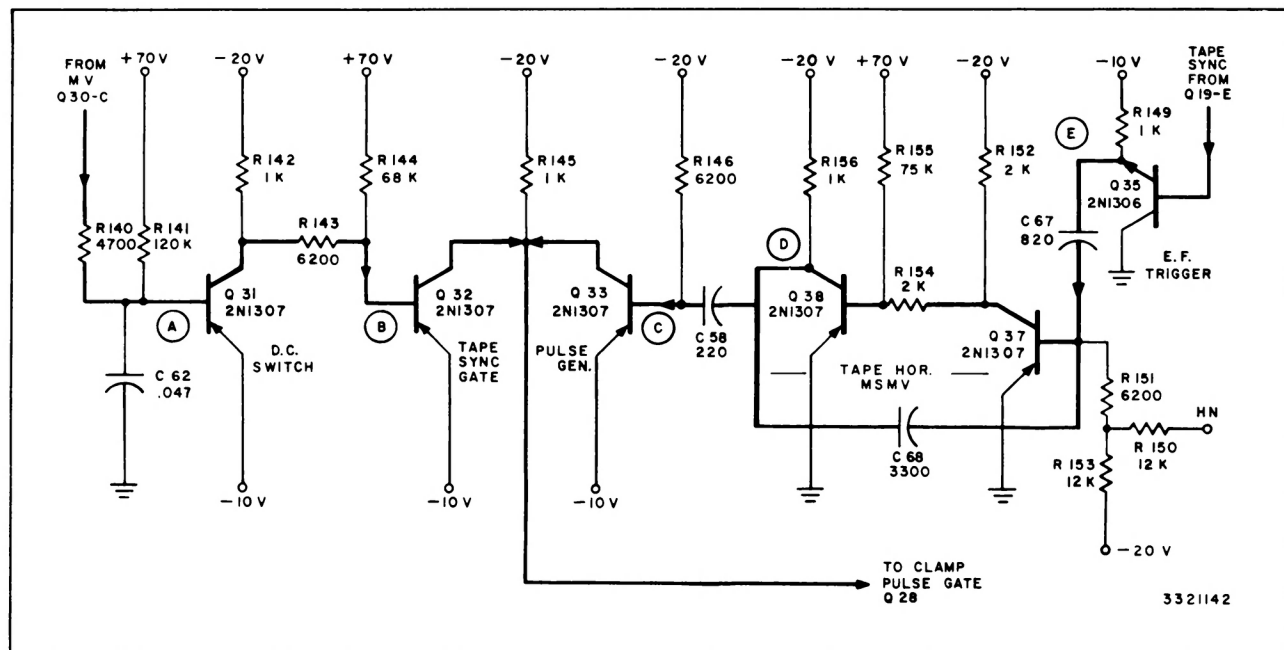


Figure 174—Clamp Pulse Generating Circuits, Tape Sync Gate and Horizontal MV

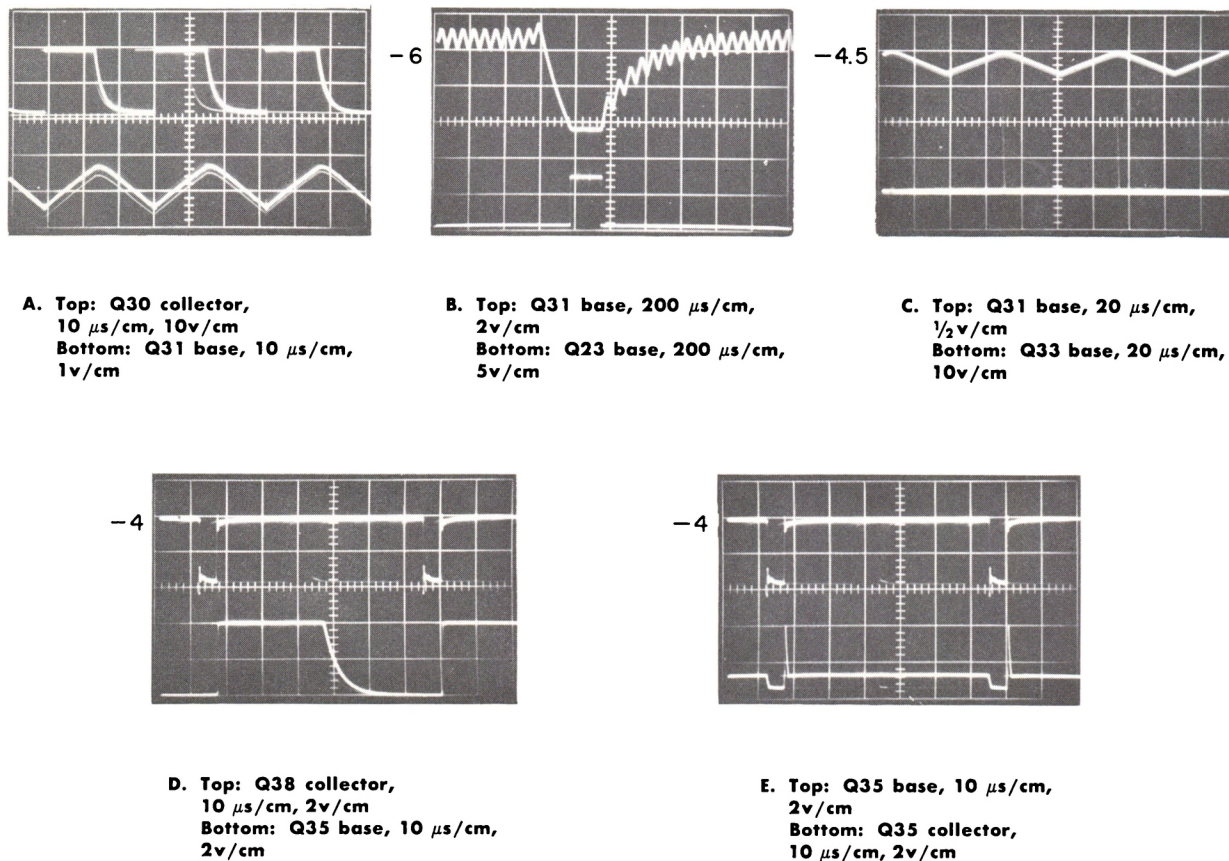


Figure 175—Typical Waveforms; Clamp Pulse Generating Circuits, Sync Gate and Horizontal MV

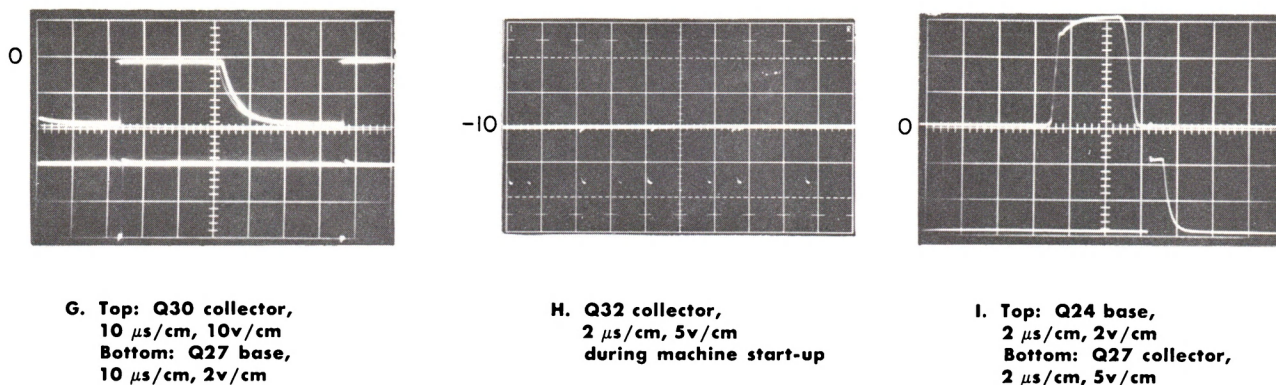


Figure 175—Typical Waveforms; Clamp Pulse Generating Circuits, Sync Gate and Horizontal MV (Continued)

MONOCHROME AUTOMATIC TIMING CORRECTOR SYSTEM

DESCRIPTION

PURPOSE

The Monochrome Automatic Timing Corrector (ATC) eliminates line-by-line timing errors in the video output of a television tape recorder during playback. If uncorrected these errors appear in the picture as geometric distortion and jitter. ATC does not replace the circuits that normally affect picture geometry but removes imperfections remaining after these circuits have performed their functions.

OPERATING MODES

ATC operates by application of an error signal to an electronically variable delay line inserted between the video output of the demodulator section and the input of the signal processing amplifier. The error signal is obtained by comparing the timing of horizontal sync in the composite video playback signal at the demodulator output with the timing of a reference sync.

The ATC circuits operate in either of two modes, *Internal* or *External*. The Internal mode is used only when the headwheel servo is in Tonewheel operation, and the External mode, only when the headwheel servo is in Pixlock. The circuits sense whether the system is in Tonewheel or Pixlock and automatically switch to the Internal or External modes.

In the Internal mode ATC corrects geometric distortion but does not synchronize vertical or horizontal sync pulses from the tape recorder with the corresponding sync pulses from the local sync generator. To accomplish this type of correction the reference sync is timed by deriving an average from a long time-constant AFC loop locked to tape sync. A dc error signal is obtained by making a phase comparison between a sample pulse derived from the trailing edge of tape sync, and a trapezoid waveform generated from reference sync. The trapezoid timing is steady enough to eliminate geometric distortion but changes sufficiently with the average timing of tape sync to prevent slow drifts from causing the error signal to exceed the correction range of the delay line.

In the external mode, essentially the same circuits are used, but the AFC loop is locked to local sync instead of tape sync. Since the local sync signal is fixed in timing, the error signal derived by comparing it with tape sync contains information to correct both jitter and geometric distortion. As a result the ATC greatly reduces residual Pixlock jitter and provides an extremely stable output.

In either of the two modes the error signal is amplified and applied to the delay line. As the demodulated composite video signal passes through the delay

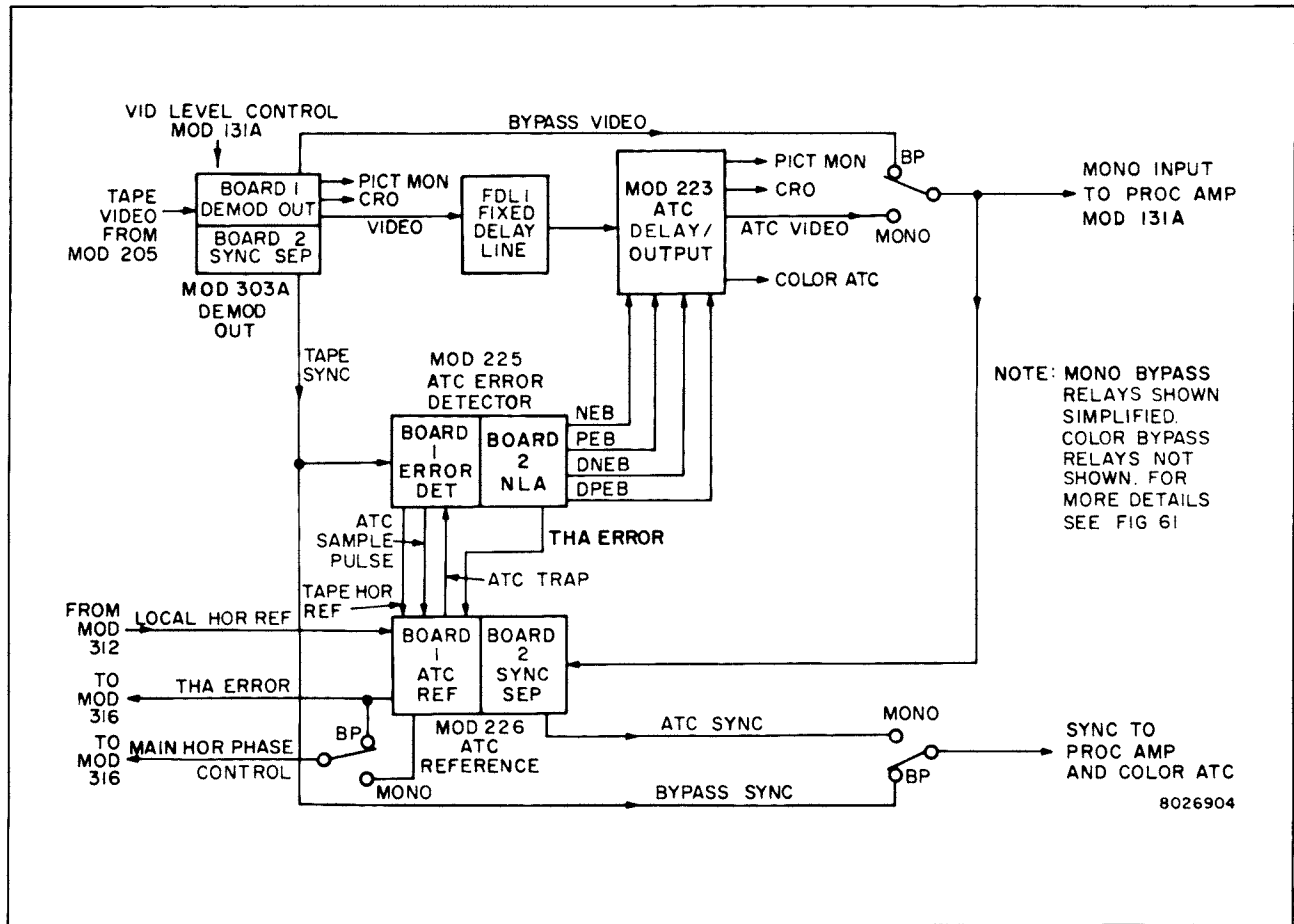


Figure 176—Simplified Functional Diagram Showing Monochrome ATC Modules in TR-22 TV Tape Recorder

line the length of the delay line is modulated by the error signal every 63.5 microseconds (525-line standards), or once per TV line.

BYPASSING

If ATC is not desired, a switch, S1, (marked ATC OFF, COLOR OFF, COLOR ATC, NON-PHASED COLOR) on module 223 permits bypassing the ATC circuit manually. In the bypass condition, the ATC modules can be tested or removed while normal playback continues, since the ATC circuits are completely removed from the signal path. (See figure 176.) Input signals are still provided to the ATC so that it can be checked while out of the signal path. All modules are interlocked so that removal of any module during ATC operation will cause automatic bypassing.

VARIABLE DELAY RANGE

The ATC circuits produce a fixed delay of (nominally) 3.1 microseconds and a variable delay having a

range of 1.0 microsecond peak-to-peak. This means that a TV line containing no timing error is delayed 3.1 microseconds, a line timed 0.5 microseconds ahead of reference sync is delayed 3.6 microseconds, and a line timed 0.5 microseconds behind is delayed 2.6 microseconds.

In the Internal mode of ATC (Tonewheel or Switchlock playback modes) the error may consist of skewing, scalloping, quadrature error, and hum. If the sum of these errors for any one TV line exceeds 1.0 microsecond the line will be uncorrected by the excess amount. In the External (Pixlock) mode the Pixlock jitter component is added to these errors. Thus, if the hum error is 0.3 microseconds, and the jitter is 0.2 microseconds, the sum of all other errors must not exceed 0.5 microseconds.

THA CIRCUIT

Full correction range is maintained automatically by a THA (Tape Horizontal Alignment) feedback

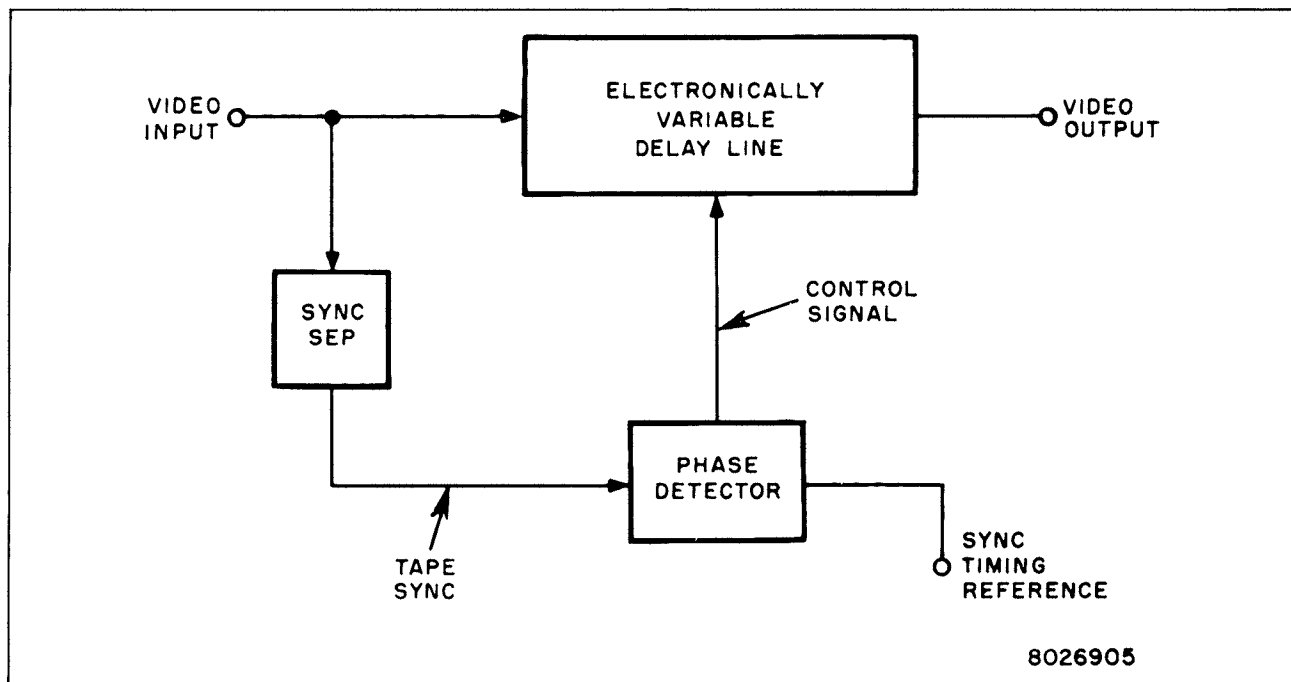


Figure 177—Open Loop Principle of Monochrome ATC

circuit. This circuit adjusts the relative phasing between the ATC sample pulse and the ATC trapezoid so that the average error signal is in the center of the delay line range. In the Internal mode the THA signal controls a variable delay in the internal reference AFC loop. In the External mode, the THA signal causes the Pixlock servo to advance the phasing of tape sync with respect to local sync by controlling the headwheel motor speed.

BASIC PRINCIPLES OF ATC

NEED FOR TIMING CORRECTION

Use of an automatic timing correction system makes it possible to achieve almost perfect time base stability in the reproduced picture without the need for constant attention and critical manual adjustments. Time base instability is introduced by the mechanical scanning process in quadruplex television tape recorders. The instability appears in two forms: geometric distortion and jitter.

Geometric distortion is caused mainly by the process of segmenting the picture signal into 16 or 17 line groups for recording on the various tracks on the tape. This type of distortion is due to rapid timing errors which cause regular horizontal displacements of various portions of the picture. The distortion takes the following three forms: (1) steps, or uniform horizontal displacement of groups of lines due to

quadrature errors in the headwheel; (2) jogs, or a skewed pattern caused by misalignment of the vacuum guide in a direction parallel to the headwheel panel; (3) scallops or bows, caused by misalignment of the vacuum guide in a direction perpendicular to the panel.

The automatic timing corrector completely corrects steps (such as the errors resulting from improper headwheel quadrature) because the timing error remains constant throughout the length of each individual line. It also corrects jogs (skewing) because the timing error from jogs, although increasing throughout the line, increases at a constant rate, and is the same for corresponding points on successive lines. A skewed picture passing through any ATC-type equipment has a small, constant error at its right-hand side but this error is invisible.

The errors resulting from scalloping cannot be completely removed by an ATC-type equipment, because the timing error at the right side of the picture is not the same for successive lines. The difference in timing errors for successive lines will be seen in the ATC output as a small skew-like effect in vertical lines at the right side only. It is, therefore, essential that the mechanical scalloping adjustment on the headwheel panel be performed carefully.

COMPONENTS OF A BASIC ATC SYSTEM

Practical field experience with quadruplex television

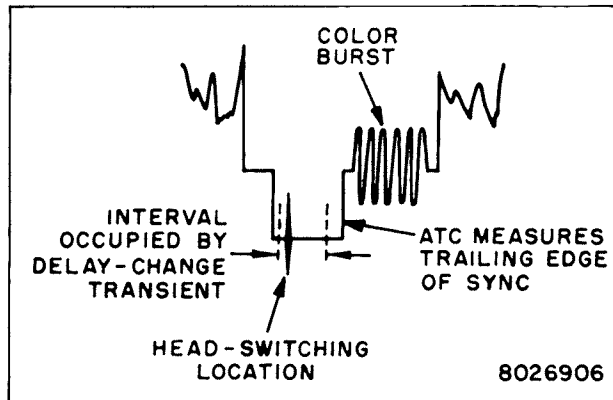


Figure 178—Locations of Head Switching and ATC Delay-Change Transients

tape recorders has shown that it is reasonably easy to maintain the total time base error below 1 microsecond peak-to-peak. Therefore, an automatic timing corrector must have a correction range of about 1 microsecond to permit non-critical operation of the recorder. This range is achieved by use of electronically variable delay lines based on reverse-biased silicon diodes, which act as variable capacitors. (See figure 177.)

In addition to an electronically variable delay line, a time base measuring circuit is required to provide

proper control of the delay line. The circuit used consists of a phase detector which compares the timing of sync pulses in the demodulated video signal with respect to a suitable reference pulse. Since the segmentation errors previously described can produce large timing errors between adjacent TV lines, the circuit measures the timing error at the beginning of each line and applies a single timing correction which lasts for the length of the line.

To achieve line-by-line correction an open loop control system is used (see figure 177). In this system sync separated from the video before application to the variable delay line is compared with the reference signal, but no feedback is provided from the output of the line.

NOTE

The basic ATC system just described is capable of correcting jitter and geometric distortion for monochrome picture reproduction. However for color reproduction, an additional color ATC system is required.

Since a large timing shift may occur when the recorder switches from one head to another during playback, it is essential that the timing error be measured after switching has taken place, so that the proper delay will be provided for the next TV line.

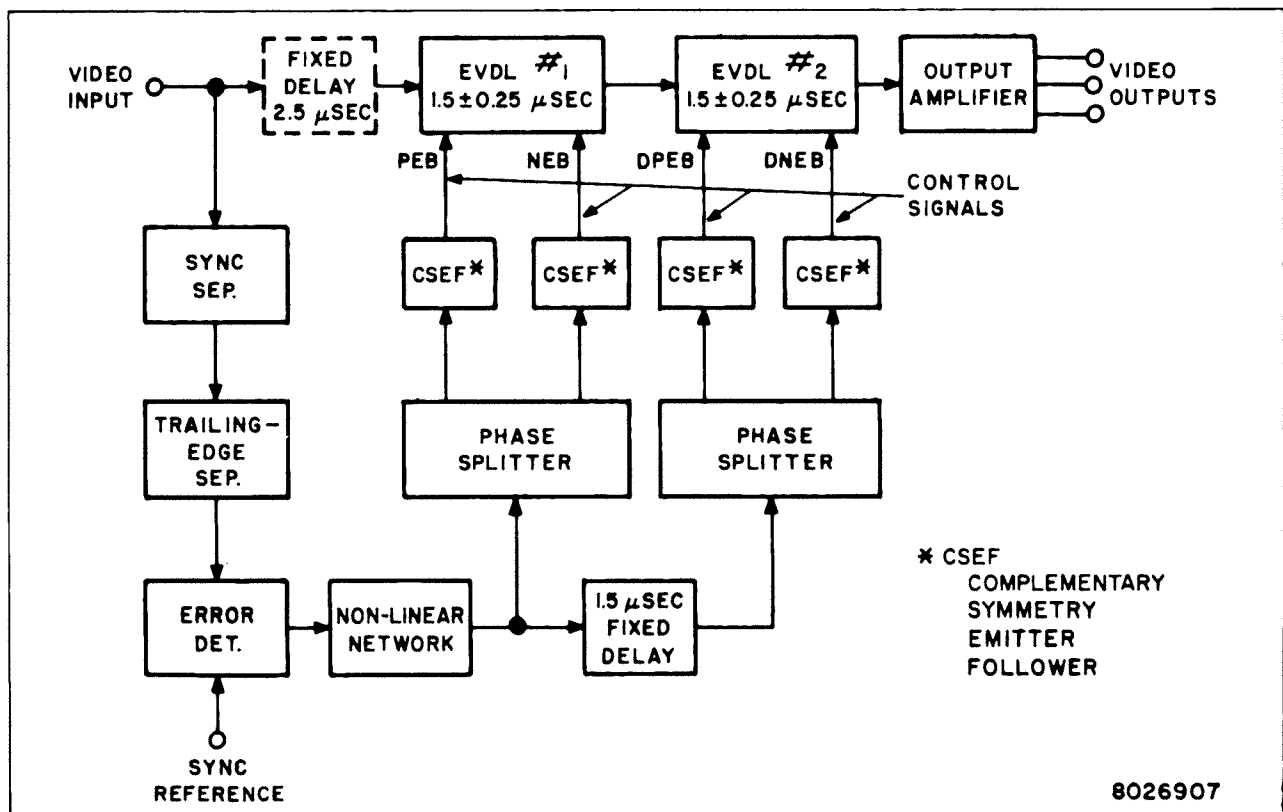


Figure 179—Basic ATC System

distances above and below the voltage applied to the center, and the ac components are equal but oppositely phased. The video input is applied between one end of the coil series and ground, and the delayed video output appears between the other end of the series and ground.

The electronically variable delay line used in the monochrome ATC system consists of two halves connected in series. The PEB and NEB signals are applied to the first half, and a pair of error signals delayed 1.5 microseconds behind the first pair are applied to the second half. The delayed signals are called the DPEB (delayed positive error bus) and DNEB (delayed negative error bus) signals.

The method of generating the ATC error signals is shown in the simplified block diagram, figure 179. Tape sync from the output of the demodulator output module is obtained by use of a clamped sync separator designed to prevent introduction of any timing errors by the separation process. The sync is then applied to a circuit which generates a sampling pulse (approximately 2 microseconds wide) from the trailing edge of tape sync. The leading edge of this pulse coincides with the sync trailing edge. The sample pulse is applied to an error detector which compares the timing or phase of the sample pulse with a reference trapezoid waveform. In the internal mode of ATC the trapezoid is obtained by applying tape sync to a long time constant AFC loop. However, in the external mode, (Pixlock) local sync is fed to the AFC circuit instead of tape sync.

The error detector produces an output voltage which changes linearly with the difference in phase between the sample pulse and the trapezoid. However, since the relation between the voltage applied to the EVDL and time delay is non-linear, the linear signal cannot be used to drive the delay line directly. To overcome this difficulty, the error signal is applied to an amplifier whose output varies non-linearly with the input signal. The amplifier is carefully designed to match the delay line characteristic so that the overall relation is linear. The output of the non-linear amplifier (NLA) is applied to a phase splitter which provides the PEB and NEB signals, and through a fixed 1.5 microsecond delay line to another phase splitter which produces the DPEB and DNEP signals. Each of the four error signals are then applied through individual complementary symmetry emitter follower (CSEF) stages to the variable delay line. CSEF circuits are used because they provide low output source impedance on both positive going and negative going signals to the error busses.

A fixed voltage of about -9.9 volts dc is applied to the center section of the variable delay line. With respect to this voltage, the positive error signal ranges from $+1$ to $+8$ volts, and the negative error signal ranges from -1 to -8 volts. Because of the non-linear characteristic of the line, the EVDL is actually in the center of its correction range when the signals are at 2.9 volts. The delay is maximum at 1 volt, and minimum at 8 volts. The dc level of the error signals must be kept at 2.9 volts or the correction range will be restricted.

TAPE HORIZONTAL ALIGNMENT (THA) LOOP

To keep the dc level of the error signals in the center of the range of the variable delay line a closed loop called the THA circuit is used. (See figure 180.)

The THA circuit provides feedback from the output of the non-linear amplifier, which controls the phasing between the ATC sample pulse and the ATC trapezoid to keep the average error signal on the PEB (positive error bus) in the center of the correction range of the variable delay line. The error is obtained from a differential amplifier which compares the dc level of the PEB signal with a fixed reference voltage. The ultimate effect of the THA current is the same in both the internal and external modes, but the point in the system to which the current is returned is different.

In the internal mode, the THA current is fed to a circuit which controls the delay of the incoming tape horizontal pulses fed to the AFC circuit. In the external mode the THA voltage is fed to a similar delay circuit in the Pixlock error detector in the linelock module, 316A.

In the internal mode, changes in the THA current shift the phase of the output of the AFC loop. As a result the phase of the ATC trapezoid shifts with respect to the ATC sample pulses. This action changes the average ATC error signal, which in turn changes the dc level of the PEB signal. This THA loop stabilizes when the PEB dc level is 2.9 volts with respect to the dc voltage fed to the center of the variable delay line. Under these conditions, the average error signal is in the center of the range of the variable delay line. It should be noted that this centered condition is necessary to permit obtaining the optimum symmetrical correction range.

In the external mode, the THA circuit is again a closed loop, but the THA current controls a variable delay in the Pixlock servo system which causes the headwheel motor to shift the phase of the video

signal at the demodulator output. In turn, this results in equal shifts in the phase of tape sync and the ATC sample pulse with respect to the ATC trapezoid. The resulting change in the PEB level increases or decreases the THA current. As in the internal mode, the loop again becomes stabilized when the PEB dc level is 2.9 volts.

FUNCTIONAL DESCRIPTIONS OF MONOCHROME ATC SYSTEM

The monochrome ATC system includes the following major components:

1. Monochrome Fixed Delay Line, FDL1.
2. ATC Delay/Output Module, 223.
3. ATC Reference Module, 226.
4. Relay bank containing monochrome and color ATC bypass relays.

The circuits on the various modules and the connections are indicated in sufficient detail for operation, system adjustments, and general trouble shooting on the *Overall Functional Block Diagram, Monochrome ATC System*, figure 9 in IB-31616-4. Control and indicator circuits are shown separately on another functional diagram, figure 8 in IB-31616-4.

OVERALL SYSTEM DESCRIPTION

The following is a summary of overall system operation based on the Functional Block Diagram, figure 9 in IB-31616-4. (For more detailed explanations see the various module circuit descriptions.)

Video Circuits

Demodulated video from the FM Standards Module, 205, is fed into the Demodulator Output Module, 303A, through P1-17. The demodulator output module amplifies the video signal and provides four outputs at pins 29, 30, 31, and 32. The outputs at pins 29 and 30 are provided for monitoring and have fixed levels. P1-29 goes to the picture monitor, and P1-30 to the CRO.

The outputs at pins 31 and 32 have variable levels remotely controlled by the LEVEL control, R15, on the Video Control Module, 131B. The video input to the ATC system is obtained from pin 31, which is connected directly to the input jack, J1, of the fixed video delay line, FDL1. The output at pin 31 goes to relay contact 11K11A-1 on the ATC relay bank. In the bypass mode 11K11 is de-energized and the video goes through relay contacts 11K11A (shown at the right side of figure 9 in IB-31616-4) to pin 21 of

module 226. From pin 21 the video is fed to a clamped sync separator in module 226, and also P1-17 of Video Control Module, 131B. When the ATC system is not bypassed, contact 11K11A-1 is open and the output at pin 32 is unterminated.

The fixed delay line, FDL1, delays the video signal obtained from P1-31 of module 303A by approximately 2.5 microseconds. The delayed output is fed through J2 of FDL1 to P1-17 of the ATC Delay/Output Module, 223. This module contains a video input amplifier, the electronically variable delay line, and a video output amplifier. The video input amplifier section amplifies the video signal and provides the proper input impedance to the variable delay line. Three adjustments are provided in this circuit, ATC LEVEL potentiometer, R3, trimmer capacitor, C20, and LINE IN TERM potentiometer, R6 (not shown in figure 9 in IB-31616-4). R3 is normally adjusted to provide a peak-to-peak video signal of 0.3 volts at the input to the delay line. C20 is adjusted to provide an overall flat response at the video output of the module, and R6 is adjusted to provide the proper termination at the input to the delay line. (See section on Module 223, for the correct adjustment procedure.)

The electronically variable delay line consists of two sections, each providing a delay of approximately $1.5 \pm .25$ microseconds. When the trailing edge of tape horizontal sync appears at the output of module 303A, the PEB and NEB error signals are applied to the error busses of the first half of the line. (The PEB signal is fed from pin 19 of module 225 to pin 19 of module 223, and the NEB signal from pin 26 of module 225 to pin 26 of module 223.) 1.5 microseconds later the delayed PEB and NEB error signals are fed to the busses of the second half of the delay line, through pins 20 and 27. In the center of its range, the variable delay line provides a delay of approximately 3.1 microseconds. The maximum obtainable delay is approximately 3.7 microseconds and the minimum, 2.5 microseconds.

The video output of the variable delay line is fed through LINE OUT TERM potentiometer, R9, to the output amplifier section of module 223. This section equalizes the signal to obtain an overall flat response and provides four output signals at pins 32, 31, 29, and 30. Pin 32 goes to the picture monitor, 31 to the CRO, and 29, to the color ATC system. The signal from pin 30 is the monochrome ATC output proper. This signal is fed to two sets of interlocked relay contacts, 11K21A, and 11K11A. 11K21 is a color ATC bypass relay, and 11K11 a monochrome ATC bypass relay. When the system is in the monochrome ATC

mode, the signal is fed through both sets of contacts to pin 21 of module 226. From this pin, the signal is fed to the Video Control Module, 131A, and also to the clamped sync separator on module 226. The output of the sync separator is fed through contact 11K11B to pin P1-18 of module 325, where it loops through to the Horizontal AFC Module (227B) and the Sync Logic Module (230B). (See the ATC connection diagram, figure 11 in IB-31616-4 for details.)

ATC Error Circuits

The circuits that process the tape sync, detect the timing error, develop the four non-linear error signals fed to the variable delay line, and detect the THA error signal are all on the ATC Error Detector Module, 225.

Tape Sync Processing Circuits

Separated sync from P1-27 of module 303A is fed through P1-17 of module 225, to the tape sync processing section on module 225. In this section the sync is amplified and clipped and then used to trigger a horizontal multivibrator. The multivibrator removes the double-rate components in the 9H vertical interval and provides a horizontal reference pulse whose timed edge coincides with the leading edge of tape sync. This pulse is fed out of module 225 through pin 29 and fed into module 226B through pin 17. (In module 226B the pulse is used to control the AFC circuit in the internal mode. This application is discussed under *AFC Reference Circuits*.) The horizontal reference pulse is also fed to a delay multivibrator on module 225. The delay of this circuit can be varied with GATE DELAY control R32.

Trailing Edge Gate and ATC Sample Pulse Circuits

The output of the delay multivibrator is differentiated to produce a pulse which is delayed with respect to the leading edge of tape sync. This pulse is applied to the trailing edge gate circuits, which consist of a pulse former and a gate. An additional input consisting of a sharp pulse which occurs at the trailing edge of tape sync is also applied to the same circuit. This pulse is obtained by differentiating the output of the sync amplifier in the tape sync processing circuits.

The trailing edge gate provides an output only when the two input pulses are coincident. When the GATE DELAY control, R32, is adjusted so that the delayed horizontal pulse occurs after the trailing edge of the equalizing pulses, coincidence will occur on each horizontal sync pulse but cannot occur during the 9H interval. The resulting output of the gate is a

narrow pulse which triggers a gate width multivibrator (no shown in figure 9 in IB-31616-4). The output of this multivibrator is fed to a boxcar and transformer driver circuit which produces the ATC sample pulse. This pulse is approximately 2 microseconds wide and its leading edge is timed with the trailing edge of tape sync.

ATC Error Detector

The ATC sample pulse is fed to a phase comparator on module 225 and also, through pin 21 of module 225 and pin 19 of module 226B, to a step generator on module 226B. The step generator imposes a flat step coinciding with the ATC sample pulse, on the slope of the ATC reference trapezoid. This step improves the accuracy of error measurement by holding the amplitude of the trapezoid constant during the measurement. The ATC trapezoid, with the step superimposed, is fed through pin 32 of module 226 and pin 31 of module 225 to the phase comparator. (The generation and timing of the trapezoid are described later under *ATC Reference Circuits*.) The phase comparator is a keyed clamp circuit which produces an error signal linearly related to the phase difference between the ATC sample pulse and the ATC trapezoid. This error signal is amplified and then fed to the non-linear amplifier on board 2 of module 225. In addition, the error signal is fed to monitor amplifier stages on board 1, which provide an output to the CRO at pin 32 of module 225.

When the recorder is in the STOP mode a clamp circuit controlled by the PLAY bus, clamps the error voltage at the output of module 225 board 1 to a fixed value, to prevent noise or transients from modulating the error detector. The PLAY bus is connected to the circuit through pin 18.

Non-Linear Amplifier

The linear error signal from the output of the error detector on module 225, board 1, is fed to a differential amplifier on module 225, board 2, which is referenced to a voltage divider network. In a monochrome ATC system, the dc reference voltage and the corresponding operating point of the amplifier are fixed. However, in a color ATC system a signal from the THAF (Tape Horizontal Alignment-Fine) circuit shifts the dc operating point to keep the color ATC system in the center of its range.

A 10-section Gamma circuit consisting of diodes and resistors, in the output circuit of the differential amplifier, changes the load impedance as the input error signal changes, and thus provides an output which varies non-linearly with the input. The output

characteristic equalizes the non-linearity of the variable delay line, so that the overall relation between the original timing error and the correction provided by the variable delay line is linear.

The output of the Gamma circuit is fed directly to a phase splitter, and also to a 1.5 microsecond fixed delay line which is connected to a second phase splitter. Each of the four outputs of the phase splitters is fed to an individual complementary symmetry emitter follower (CSEF). The pair of CSEF circuits connected to the first phase splitter produces the PEB and NEB signals previously discussed, and the other pair produces the DPEB and DNEB signals. The PEB and NEB signals are applied to opposite sides of the first half of the variable delay line, through pins 19 and 26, and the DPEB and DNEB signals to opposite sides of the second half of the delay line through pins 20 and 27.

A voltage of approximately -9.9 volts dc is applied from a precision voltage divider on board 2 of module 225, through pin 12 of module 225 and pin 18 of module 223, to the center section of the variable delay line. This voltage is factory adjusted with the LINE CENT potentiometer. The error fed to the delay line ranges from 1 to 8 volts with respect to the delay line reference. The delay provided by the variable delay line is approximately 3.7 microseconds when the error is 1 volt, and approximately 2.5 microseconds when the error is 8 volts. In the center of the delay range (approximately 3.1 microseconds) the value is about 2.9 volts.

THA Circuit

To maintain full correction range it is essential that the average PEB voltage be about 2.9 volts positive with respect to the center voltage. This condition is maintained automatically by the THA loop. (See *Basic Principles of ATC*.) The THA differential amplifier is on module 225, board 2. A sample of the PEB signal is filtered to produce an average voltage and then applied to one section of the THA differential amplifier. The THA reference voltage, obtained from the same divider as the delay line center voltage, is applied to the other section of the differential amplifier. The THA error signal, which is proportional to the difference between the two voltages, is fed through pin 5 of module 225 and pin 10 of module 226 to relay contacts K2A and K2B on module 226. In the internal mode, K2B feeds the THA signal to a delay control stage on module 226. Under these conditions, changes in the THA signal shift the average position of the ATC reference trapezoid so that the average PEB signal is 2.9 volts posi-

tive. In the external mode, K2A feeds the THA signal out, through pin 14 of module 226. Pin 14 is connected through the normally closed contacts of color ATC bypass relay 11K32 to pin 6 of the Linelock module, 316A. Pin 6, in turn, is connected to a delay control stage in the Pixlock error detector. Under these conditions changes in the THA signal cause the Pixlock system to change the phase of the demodulated tape composite video. The resulting change in the phase of sync separated from this video signal shifts the average position of the ATC sample pulse with respect to the ATC trapezoid to maintain the average PEB voltage at +2.9 volts.

ATC Reference Circuits

The ATC reference circuits on board 1 of module 226 are controlled by three relays K1, K2, and K3. The AFC circuit is switched out during the NPC mode and the ATC trapezoid is referenced to the local horizontal sync. Relay K1 is de-energized in all modes except NPC. Relays K2 and K3 are de-energized in the internal (tonewheel or switchlock) mode and energized in the external (pixlock) mode. (See *ATC Control and Indicator Circuits* for details.) Contact K1A connects the internal reference multivibrator to ATC trapezoid generator. K2A switches the THA signal from module 225 to module 316 when the system is in the external mode, as previously explained. K2B and K3A determine whether the delay control stage is automatically controlled by the THA signal or manually controlled by potentiometer adjustments.

The tape horizontal reference pulse from pin 29 of module 225 is fed to pin 17 of module 226 and the normally closed contact of K3A. The local horizontal reference pulse originating at the Reference Generator Module, 312, is fed to pin 18 and the normally open contact of K1A. The selected reference pulse is delayed by the delay generator and fed to circuits which generate a narrow sample pulse used to control the AFC circuit. The amount of delay between this AFC sample pulse and the horizontal reference is determined by the current fed into the delay generator from a delay control source. When the recorder is in play and ATC is in the internal mode this current is automatically controlled by the THA signal, which is fed to the delay control stage through the normally closed contact of K2B. In the external mode, the current can be adjusted manually by the AUX HOR PHASE control on module 223 and the MAIN HOR PHASE control on module 316. The two controls are connected to the delay control stage through normally open contacts of K2B and K3A.

The AFC sample pulse provides timing information to an AFC loop which controls the timing of the ATC reference trapezoid. The AFC loop consists basically of a phase comparator, a variable frequency oscillator, (marked HOR OSC. in figure 9 in IB-31616-4) a horizontal multivibrator, a switched delay stage, and an AFC trapezoid generator. The variable frequency oscillator, or internal reference multivibrator, is basically a free running multivibrator whose frequency can be varied by application of an error signal. The output of the internal reference multivibrator triggers the AFC horizontal multivibrator, and the resulting output pulse is fed through the switched delay stage to the AFC trapezoid generator. The switched delay stage is controlled by logic inverter Q19 on module 226, and relay contact 11K21B on the ATC Relay Bank. This stage delays the start of the AFC trapezoid by approximately 6.5 microseconds in the external mode of monochrome ATC, or 11.5 microseconds in the color ATC mode. In the internal mode, the switched delay is zero.

The AFC trapezoid is fed to the phase comparator where it is compared with the AFC sample pulse to produce an error signal linearly related to the phase difference. This error signal is averaged by a long time constant RC circuit and then fed back to the internal reference multivibrator.

The free-running frequency of the internal reference multivibrator is manually adjustable by two controls on the front panel of module 226, one for 525-625 line TV standards and the other for 405-line standards. This frequency is adjusted to equal the horizontal line rate corresponding to the desired TV standards. When the AFC loop has reached equilibrium, the frequency of the multivibrator will be equal to that of the AFC sample pulse and the AFC trapezoid will be approximately centered with respect to the sample pulse. If the phase of the sample pulse changes, the multivibrator phase will also change to maintain centering of the trapezoid. However the multivibrator phase cannot vary at a horizontal rate because of the long time constant of the loop.

The output of the internal reference multivibrator is fed to a circuit which generates the ATC reference trapezoid. In the internal mode, the ATC trapezoid starts at the same time as the AFC trapezoid because the switched delay stage between the internal reference multivibrator and the AFC trapezoid generator produces zero delay. However, in the external or color ATC mode the ATC trapezoid starts in *advance* of the AFC trapezoid by the amount of switched delay

(approximately 6.5 microseconds in monochrome ATC or 11.5 microseconds in color ATC).

As previously described under *ATC Error Detector* a step generator stage superimposes a flat step, which coincides with the ATC sample pulse, on the slope of the ATC trapezoid. The step generator is controlled by the ATC sample pulse, which enters module 226 through pin 19.

The ATC trapezoid, with the superimposed step is fed through the ERROR GAIN control (on the front panel of module 226), pin 32 of module 226, and pin 31 of module 225 to the phase comparator on board 1 of module 225. The ERROR GAIN control determines the slope of the ATC trapezoid and thus establishes the absolute relation between timing error detected and change in error voltage.

ATC CONTROL AND INDICATOR CIRCUITS

A functional diagram of the control and indicator circuit is shown in figure 8 in IB-31616-4. This diagram includes the color ATC control circuits. However, only the monochrome circuits will be described in this book. The ATC relay bank includes the external relays for color ATC, but all of these relays remain de-energized unless the color ATC system is installed.

Monochrome ATC Bypass System

Two monochrome ATC bypass relays, 11K11, and 11K12 (see figure 8 in IB-31616-4), are provided on the ATC Relay bank. One side of the coils of these relays is connected to -26 volts, and the other side is connected through the monochrome ATC module interlock system to the circuit of ATC function selector switch S1 on module 223. S1 is a four-position switch with its arm grounded. The four switch positions are marked ATC OFF, COL OFF, COLOR ATC and NON-PHASED COLOR. In either the COL OFF, or COLOR ATC positions, the switch grounds the interlock bus through a diode. If the three monochrome ATC modules, 223, 225, 226, are in place, this action energizes the two relays and also lights the ATC indicator lamp, 5DS15 on the front of the recorder.

Each of the two bypass relays, 11K11 and 11K12 has two sets of two-way contacts, A and B. 11K11A and B, and 11K12A are shown in figure 9 in IB-31616-4, and 11K12B is shown in figure 8 in IB-31616-4. In both diagrams the contacts are in the de-energized or bypass condition. In this condition the contacts perform the following functions:

1. 11K11A disconnects and unterminates the ATC video output at module 223, pin 30, and connects the video signal from pin 32 of module 303A, through pin 21 of module 226 to the processing amplifier input on module 131B.

2. 11K11B disconnects the output of the clamped sync separator on module 226, and feeds tape sync from the separator on module 303A to the color ATC system and the horizontal AFC and sync logic modules of the processing amplifier.

3. 11K12A connects the MAIN HOR PHASE control on the linelock module, 316A, to a delay control stage on the same module (through normally closed contacts of 11K32).

4. 11K12B (see figure 8 in IB-31616-4) disconnects the linelock control bus from the coils of internal-external reference relays K2, K3, so that the ATC system cannot enter the external mode.

When the relays are energized (S1 in NPC, COLOR ATC, or COL OFF) the following occurs:

1. 11K11A connects the ATC video output to the processing amplifier and the clamped sync separator on module 226.

2. 11K11B connects the output of the clamped sync separator on module 226 to the color ATC system and the horizontal AFC and sync logic modules.

3. 11K12A connects the MAIN HOR PHASE control on the linelock module, 316A, to the delay control stage on module 226.

4. 11K12B (see figure 8 in IB-31616-4) connects the linelock control bus to the coils of K2 and K3 on module 226.

Monochrome ATC Reference Relays (on Module 226)

The coil circuits of relays K1, K2, K3 on module 226 are shown in figure 8 in IB-31616-4. One side of the three relay coils is connected to -26 volts and the other side of relays K2 and K3 go to contacts of 11K12B. While relay K1 is controlled by the NPC bus.

In the bypass condition 11K12 is de-energized and consequently the coil circuits of K2, K3 are opened. In the monochrome or color ATC modes 11K12 is energized and 11K12B connects the K2 and K3 relay coils to a control bus from the linelock module 316A which goes to contact K1B on 316A.

When the recorder servos are in the tonewheel or

switchlock mode, the linelock control bus from module 316A is open, the two reference relays K2 and K3 are de-energized, and the ATC system is in the internal mode. However, when the headwheel servo system is in Pixlock, K1B on the linelock module grounds the control bus. This energizes the relays, and the system enters the external mode (unless the system is in the bypass condition).

Each of the three reference relays (K1, K2, K3) has two sets of two-way contacts, A and B. K1B is not used. All other contacts are shown in figure 9 in IB-31616-4.

In the internal mode the following actions occur:

1. K1A connects the output of internal reference multivibrator to the ATC trapezoid generator.

2. K2A disconnects the THA signal from the linelock module.

3. K2B disconnects the auxiliary HOR PHASE control on module 223 from the delay control stage on module 226 and feeds the THA voltage to this stage.

4. K3A disconnects the main HOR PHASE control from the delay generator on module 226.

5. K3B connects the tape horizontal reference from module 225 to the delay generator on module 226.

In the external mode the contacts act as follows:

1. K1A connects the output of internal reference multivibrator to the ATC trapezoid generator.

2. K2A connects the THA signal to the delay control stage on the linelock module.

3. K2B connects the auxiliary HOR PHASE control to the delay control stage on module 226.

4. K3A connects the main HOR PHASE control to the delay control stage on module 226.

5. K3B connects the local horizontal reference to the delay generator on module 226 instead of the tape horizontal reference.

In the NPC mode the contacts act as follows:

K1A switches out the internal reference multivibrator and feeds the local horizontal reference signal to the ATC trapezoid generator.

The tonewheel/pixlock mode control system also contains relay K41, figure 8, of IB-31616-4. One side of the coil of relay K41 is connected to the -26 volt dc supply. The other side of the relay coil is connected to the Linelock or Pixlock position of the servo mode selector switch on the tape sync processor module (no.

317) via diode CR13 or CR14. See diagram of module 317B.

When the selector switch on 317B is in the Linelock or Pixlock position and the machine is operating in the PLAY mode, ground potential is applied to the arm of the selector switch via pin 6 of the module, and thus to the coil of relay K41. Relay K41 is thereby energized and is inserted in series with relay K24A, thus allowing ground potential to be applied to the NPC bus when the selector switch on the 223 ATC delay module is in the NPC position.

See Color ATC, IB-31652, for more information concerning operation of the ATC and CATC relays.

Error Voltage Clamp

When the recorder is in any mode but PLAY (AUD or CUE RECORD) the PLAY control bus, which enters module 225 through pin 18, is connected to -26 volts. This causes a clamp circuit on module 225 to clamp the output of the ATC error detector to a fixed value (+4 volts). In the PLAY (AUD or CUE RECORD) modes the PLAY bus becomes grounded and the clamp circuit is inactive.

OVERALL TIMING RELATIONS

Overall timing relations between the most important waveforms in the monochrome ATC system, under zero error conditions, are shown in figures 181 and 182. Figure 181 pertains to the internal mode of ATC (tonewheel or switchlock) and figure 182 to the external mode (Pixlock).

STOP Mode

When the recorder is in the STOP mode (or any other mode except PLAY, AUDIO RECORD, or CUE RECORD) the reference relays on module 226 place the system in the internal mode, and the clamp circuit on module 225 clamps the linear ATC signal at the output of module 225, board 1, to a fixed value of approximately +4 volts. As a result, the non-linear error signals on the busses of the variable delay line are fixed at a value producing a delay approximately in the center of the range of the variable delay line (3.1 microseconds). In addition, the signal fed to the input of the ATC system is obtained by modulating and demodulating the video entering the recorder from the incoming line.

Under these conditions, the timing relations are approximately as shown in figure 181. The primary timing reference for the error signals is the sync from the demodulator output (item 1 of figure 181). The

leading edge of this sync produces the timed edge of the tape horizontal reference signal (item 7). The variable delay generator in module 226 delays the AFC sample pulse (item 5) behind this timed edge by an amount determined by the THA circuit (item 6). However, since the ATC error signal is clamped to a fixed value, the THA signal also remains fixed and causes the generator to produce a fixed delay approximately in the center of its range (item 6).

The AFC circuit on module 226 causes the AFC trapezoid (item 4) to center itself with respect to the AFC sample pulse. This action also times the ATC trapezoid (item 3) since the two trapezoids start simultaneously.

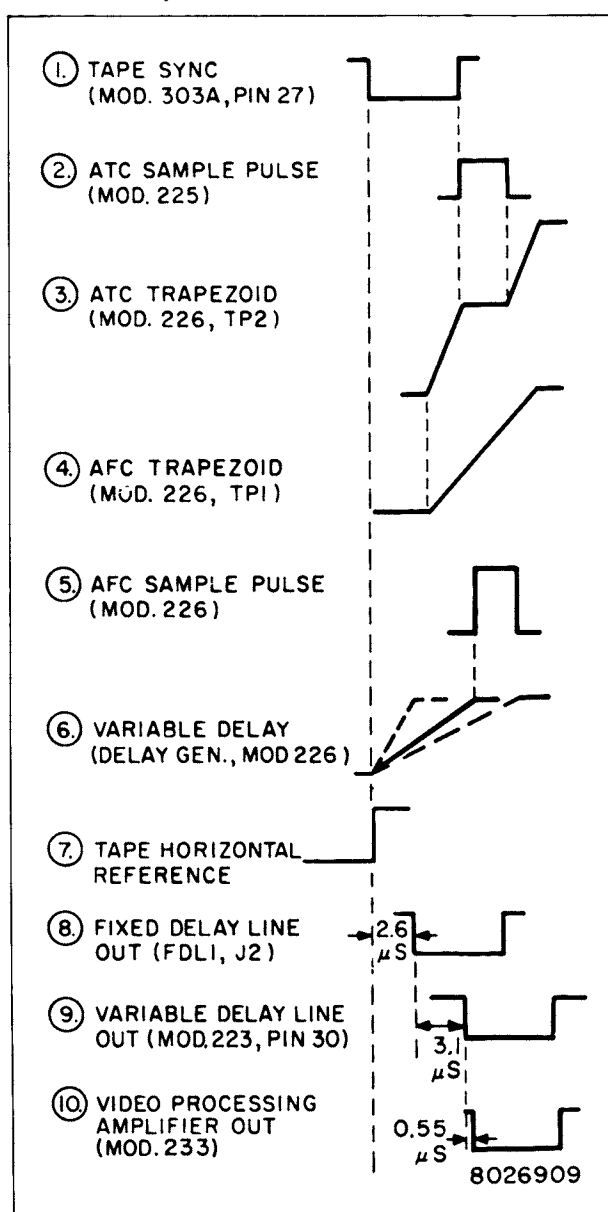


Figure 181—ATC System Timing Relations, Internal Mode

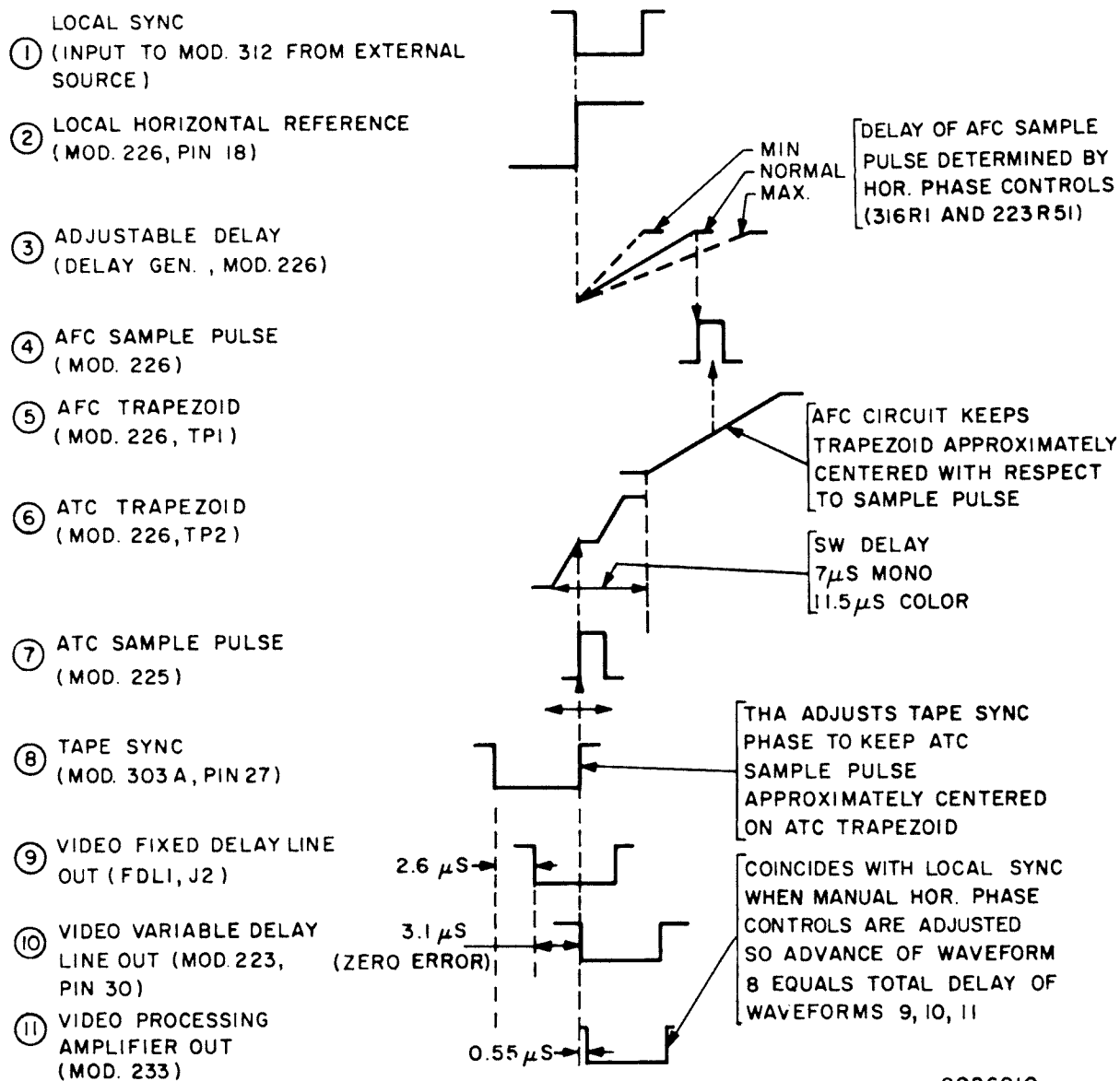


Figure 182—ATC System Timing Relations, External Mode

The leading edge of the ATC sample pulse (item 2) coincides with the trailing edge of demodulated sync (item 1), and the step on the ATC trapezoid coincides with this sampled pulse.

The output of the fixed video delay line (item 8) is delayed behind the demodulated sync by approximately 2.6 microseconds. The video output of the variable delay line (item 9) is further delayed by a fixed amount of approximately 3.1 microseconds.

PLAY Mode (Tonewheel or Switchlock)

When the recorder is in the play mode the video signal at the demodulator output is derived from tape playback, the output of the ATC error detector on module 225 is unclamped, and the monochrome ATC system functions normally. While the recorder servo systems are in tonewheel or switchlock the ATC system is always in the internal mode. (If the recorder is in Pixlock the ATC system will be in the external mode, unless the ATC function selector switch on module 223 is in the ATC OFF position or the ATC interlock system is open.)

In the internal mode, the timing relations are as shown in figure 6 if tape sync is occurring at the correct horizontal frequency, and is free of timing variations. Conditions are then the same as previously described for the STOP mode except that the variable delay of the AFC sample pulse (item 6) is automatically set by the THA circuit so that the PEB is 2.9 volts positive with respect to the voltage fed to the center of the variable delay line. As a result the position of the ATC trapezoid with respect to the ATC sample pulse, and the corresponding value of the variable delay may be slightly different than in the STOP mode.

If timing errors do exist in tape sync, figure 181 represents average conditions. All the error detection waveforms shown, except the two trapezoids are locked directly to tape sync and therefore shift together by equal amounts when line-to-line timing variations occur. The two trapezoids are also locked together, but the long time constant network in the AFC circuit eliminates the horizontal rate timing variations in the trapezoids and allows them to follow only slow drifts in the phase of the AFC sample pulse.

Assume that conditions are as shown in figure 181, in one TV line, but, in the next TV line, tape sync occurs 0.1 microsecond too soon. Waveforms 1, 2, 5, 6, 7, and 8 then move to the left with respect to the two trapezoids by an amount corresponding to 0.1 microseconds. However the change in position of the

ATC sample pulse (item 2) with respect to the ATC trapezoid (item 3) changes the ATC error signal. As a result, the delay of the variable delay line will increase by 0.1 microsecond and the sync at the video output of the variable delay line (item 9) will remain in exactly the same position with respect to the trapezoids.

If a slow drift occurs in the phase of tape sync the AFC circuit will allow the AFC trapezoid to follow the drift and to remain centered with respect to the AFC sample pulse. In addition, the THA circuit will maintain the variable delay of the sample pulse at the correct value to keep the average ATC error signal in the center of the range of the variable delay line. As a result, all ten of the waveforms shown in figure 181 will drift by the same amount.

PLAY Mode (Pixlock)

Timing relations for the external (PIXLOCK) mode of ATC are shown and explained briefly in figure 182. Further details are given in the section on the ATC Reference Module, 226.

OPERATING PROCEDURE

The setup procedure for routine operation of the ATC System is given in the following paragraphs.

NOTE

If the procedure is being performed for the first time do not install modules 225 and 226 until step 17.

1. Place the machine in STOP. Apply video and sync to the inputs of the machine.
2. Press Picture Monitor and CRO VID IN buttons.
3. Adjust the video LEVEL control on module 103 (R3) for normal video level (140 IRE units).
4. Depress DEMOD OUT buttons of Monitor and CRO.
5. Adjust the DEMOD LEVEL control on module 205 (R40) for proper level (140 IRE units). Adjust deviation if necessary.
6. Place function selector S1, on module 223, in the ATC OFF position. Connect an oscilloscope to test point TP1 (VID OUT VARIABLE) on module 303A and adjust LEVEL control (R15) on module 131A for 1 volt peak-to-peak.
7. Move the oscilloscope probe to TP5 on module 223. The peak-to-peak amplitude of the composite video should be 1 volt. If the amplitude at this point is incorrect by about ± 0.15 volts place module 223

on an extender and adjust R3 on that module to produce 1 volt.

NOTE

If the amplitude at TP5 is off by more than ± 0.15 volt more accurate adjustments are required in the video path of this module. These adjustments should be made as directed under *Maintenance* in the section on module 223.

8. Remove the extender and re-install module 223 in the machine.

9. Place module 131B on an extender.

10. Press VID OUT buttons of CRO and Picture Monitor.

11. Adjust sync LEVEL control (R27) on module 132 to produce 40 IRE units of sync on the CRO.

12. Adjust potentiometer R48 on 131B to produce 95 IRE units of video on the CRO. It may be necessary to readjust the PEDESTAL control (R43) on module 131B to obtain the normal 5 units of pedestal.

13. Remove module 131B from the extender and reinsert it in the machine.

14. Thread a test tape onto the machine. Play the tape, and make necessary adjustments (such as vacuum-guide position) to produce normal playback.

15. Check the machine for normal operation on Tonewheel, Switchlock, Linelock and Pixlock modes and make adjustments if necessary.

16. Stop the machine and insert modules 225 and 226, if they are not already in machine. (See note before step 1).

17. Play standard tape.

18. Depress the ATC OUT pushbuttons on the Picture Monitor and CRO.

19. If a normal picture appears, steps 20 and 21 may be omitted. If the picture has groups of lines shifted to the left and to the right, follow steps 20 through 21 to adjust the horizontal AFC frequency.

20. On module 226 adjust the screwdriver potentiometer marked HOR FREQ SET (525-625) for a perfect lock of the picture. Then press the button marked HOR FREQ SET. The picture should remain locked. If necessary repeat the adjustment while holding down the button, until a perfect lock is obtained.

21. Stop the machine. The picture should remain locked.

NOTE

If difficulty is encountered in obtaining a lock connect oscilloscope to TP2 on module 226 and check the centering of the step on the trapezoid while playing the tape with S1 on module 223 in ATC OFF. If step is not centered adjust R60 as directed in the section on 226.

22. If the machine is to be operated on 405 line standards, also adjust the HOR FREQ SET (405) potentiometer as in steps 20 and 21.

23. Play the test tape and observe the CRO with either the ATC OUT or VID OUT buttons pressed. The video amplitude should be the same as on DEMOD OUT. If necessary, adjust LEVEL CONTROL R15 on module 131B for the required level.

24. Connect one probe of a dual-trace oscilloscope to TP2 (DYLD HOR) on module 225. A narrow triangular pulse will be seen. Connect the other probe to TP6, on module 303A. Sync will be seen.

25. Adjust GATE DELAY (R32, module 225) to make the leading edge of the triangular pulse occur 3.0 microseconds after the leading edge of sync.

26. Set up the machine in the following manner.

- a. *Servo mode*: Tonewheel.
- b. *Monitor Switcher*: DEMOD OUT.
- c. *CRO Switcher*: ATC ERROR.
- d. *Picture monitor*: Internal Sync.
- e. *Guide Servo*: MANUAL.
- f. *ATC mode switch*: ATC OFF.
- g. *CRO deflection*: Vertical, Normal.

27. Play back a test tape. Adjust the manual guide control for approximately 1 microsecond of jogs light pressure. 1 microsecond of jogs equals 100 IRE units on the CRO.

NOTE

If headwheel tends to lose contact at 1 μ sec, slightly smaller jogs may be used for the following tests.

28. Press the ATC OUT button on the picture monitor switcher.

29. Adjust ERR. GAIN (front of module 225) to remove the jogs in the picture. Adjust for no jogs at the left of the picture. If jogs then are visible on the right of the picture, the guide height is not properly adjusted. If this occurs, return the picture monitor to DEMOD OUT and, with a scalloping wrench, adjust guide height in the normal manner to remove scallops. Then repeat this step. The entire picture should be free of jogs.

30. Put the guide servo in AUTO and place the machine in PIXLOCK.

31. Leave the guide servo in MANUAL with 1 microsecond jogs.

32. Put the picture monitor on pulse cross and simultaneously depress VID IN and VID OUT push-buttons on the picture monitor switcher.

33. Put the machine in the STOP mode and connect the external CRO probe to test point TP2 on the ATC reference module 226A. Observe the sampling step (which should be centered on the ATC trapezoid).

34. Turn the HOR PHASE knob on Linelock module 316B maximum ccw. Turn AUX HOR PHASE control on module 223B maximum ccw. Play tape in PIXLOCK and ATC.

35. Slowly turn the HOR PHASE control on module 223B clockwise until the horizontal phase of video output is 4 microseconds delayed with respect to video input. (Leading edge of sync output approximately aligned with the trailing edge of input sync as observed on pulse cross.) This adjustment is correct if the HOR PHASE knob, on module 316B, can be turned from one extreme to the other without forcing

the ATC sampling more than 5-10% away from the center of the slope.

36. Adjust the HOR PHASE knob on module 316B to align the leading edges of input and output sync.

37. Place the FM EQ control on the FM Equalizer Module (1,2) in the 11 o'clock position (between $\frac{1}{4}$ and $\frac{1}{2}$ turn from the maximum counterclockwise position).

38. Press the DEMOD OUT button on the CRO. Play back the test tape and, while watching the multiburst pattern on the CRO, adjust the four channel equalizer controls on the P.B. Amp. Modules (215, 216, 217, 218) for flat response.

39. Press the DEMOD OUT button on the picture monitor. Observe the multiburst pattern on the picture monitor and, if necessary, retouch the channel equalizer controls for equal response in the four head bands.

40. Press the ATC OUT button on the CRO Switcher and observe the multiburst pattern on the CRO. If the response is not flat adjust trimmer capacitor C20 on the ATC Delay/Output Module (223A) for flat response.

MODULE CIRCUIT DESCRIPTIONS AND MAINTENANCE

Detailed circuit descriptions, block diagrams, simplified schematics, waveforms and maintenance procedures for the individual modules of the Monochrome ATC system are given in the following sections. The simplified schematics are provided mainly to illustrate the circuit descriptions. Complete schematic diagrams are given in the Diagram Manual IB-31616-4.

FIXED DELAY LINE, FDL1

The Fixed Delay Line, FDL1 (see figure in IB-31616-4) provides a fixed delay of approximately 2.6 microseconds between the video output of the Demodulator Output module, 303A, and the video input amplifier on the ATC Delay/Output module, 223. The line consists of 58 series coils and 59 shunt capacitors. Both the input and output terminations are adjustable.

Video from P1-13 of the output connector on module 303A is fed into the fixed delay line through coaxial connector J1. The level of this signal can be adjusted by the video LEVEL control, R15, on module 131B, which remotely controls a lamp and photocell circuit on module 303A. A potentiometer, R2, in an RC network at the input of the line permits adjusting

the line termination to provide an overall flat response. Another potentiometer, R4, and a tunable coil, L59, permit adjusting the output termination. The video output of the line is fed from coaxial connector J2 to P1-17 of the connector on module 223. The input to the fixed delay line can be observed at test point TP1 on module 303A, and the output, at TP1 on module 223.

FIXED DELAY LINE TERMINATION ADJUSTMENTS

The delay line termination potentiometers have been adjusted for optimum performance at the factory, utilizing equipment not generally available in most television studios, and it is extremely unlikely that any readjustment will ever be required. Therefore, unless trouble in the ATC system is traced directly to the delay lines, DO NOT CHANGE THE SETTING OF ANY TERMINATION POTENTIOMETER.

Since component failure within a delay line unit cannot be compensated for by adjusting the associated termination potentiometer, readjustment of a potentiometer is only required when the potentiometer has been inadvertently misadjusted. If misadjustment

occurs, the procedures presented below may be followed in readjusting the termination potentiometers for satisfactory ATC system performance.

NOTE

Before making any adjustments it is advisable to mark the present potentiometer setting by some convenient means (e.g., a scribe mark on the shaft).

Test equipment required for termination potentiometer readjustment includes the following:

75-ohm Attenuator

Video Sweep Generator

(Marconi Model 1099 or equivalent)

Dual Trace Oscilloscope

(Tektronix Type 535A, or Type 545A with CA plug-in, or equivalent)

Vacuum-Tube Voltmeter

(RCA Voltomyst or equivalent)

1. Disconnect the coax cables from the input and output jacks (J1 and J2) of the fixed delay line FDL1 which is located at the rear of the machine.

2. Connect a length of RG59U cable between the delay line output (jack J2) and the oscilloscope input, utilizing a T connector at the oscilloscope. Terminate the line at the T connector with 75 ohms.

3. Connect the sweep generator to the delay line input (jack J1). Adjust the generator for a sweep range of 1 to 11 mc, and an output signal amplitude of 1 volt at 5 mc.

4. Remove the delay line cover.

5. Observe the oscilloscope and tune inductor L59 to obtain the flattest overall frequency response, referenced to the sweep generator output, between 1 and 6 mc. The response should be flat $\pm 5\%$ to 5.0 mc, $\pm 10\%$ to 7.0 mc, and cut off at approximately 9.5 mc.

6. Alternately adjust termination potentiometers R2 and R4 to minimize ripple at 1 and 8 mc. (The output level should not be less than 0.38 volt peak-to-peak when the potentiometers have been adjusted.)

7. Disconnect the sweep generator from the delay line input (jack J1) and feed a video signal to the delay line.

8. With the oscilloscope "B" input connected to the delay line output, as in step 2 above, connect the oscilloscope "A" input to the delay line input.

9. Place the oscilloscope selector switch in ALTERNATE position, and observe the delay generated by the delay line. The delay, as observed on the oscilloscope, should be 2.68 microseconds (-0.1 , $+0.2$).

10. Remove the oscilloscope probes and video input, replace the delay line cover, and re-connect the coax cables to the fixed delay line input and output jacks (J1 and J2).

ATC DELAY/OUTPUT (Module 223)

The ATC Delay/Output module, 223A, contains two circuit boards. Board 1 (see figure 183) contains the video input and output amplifiers for the electronically variable delay line, and board 2, the delay line itself. The front panel contains the AUX HOR PHASE control, R51, and the ATC function selector switch, S1.

CIRCUIT DESCRIPTIONS

Video Input Amplifier Circuit (Q11, Q1, Q2)

The video input amplifier circuit (see figure 184) amplifies the output of the fixed delay line, FDL1, and provides the proper input impedance to the variable delay line. The circuit consists of an emitter follower, Q11, common base amplifier, Q2, and driver, Q1. Three adjustments are provided in this circuit: the ATC LEVEL potentiometer, R3, which determines the input level to the first stage, trimmer capacitor C20, which permits peaking the output of the first stage to obtain an overall flat response, and potentiometer R6, which permits adjusting the termination at the input of the variable delay line.

Video having an amplitude of approximately 0.4 volts peak-to-peak is fed from the output connector J2 of the fixed delay line, to the input on module 223 at P1-17. The signal at this point can be observed at test point TP1 on the front panel (see figure 185A). The video signal is fed to the base of emitter follower Q11 through a voltage divider which includes the ATC LEVEL potentiometer, R3. The operating point of Q11 is determined by two resistors, R40 and R39, which are connected in series from the emitter to +70 volts. The junction point is also connected to resistor R41 in the output amplifier section to provide base bias for stage Q4. The output of Q11 (figure 185B) is fed to the emitter of common base amplifier Q2 through an RC high-frequency peaking network consisting of R35, R36, and trimmer capacitor C20. The capacitor permits adjusting the peaking for an overall flat response at the output of the module. Base bias for Q2 is obtained from a voltage divider consisting of R33 and R32, which runs from ground to -10 volts. The junction of the two resistors is bypassed to ground by 220 mf capacitor, C19. The junction point is also connected to the base of stage Q3 in the video output section to provide base bias. The

Figure 183—Block Diagram, ATC Delay/Output Module 223

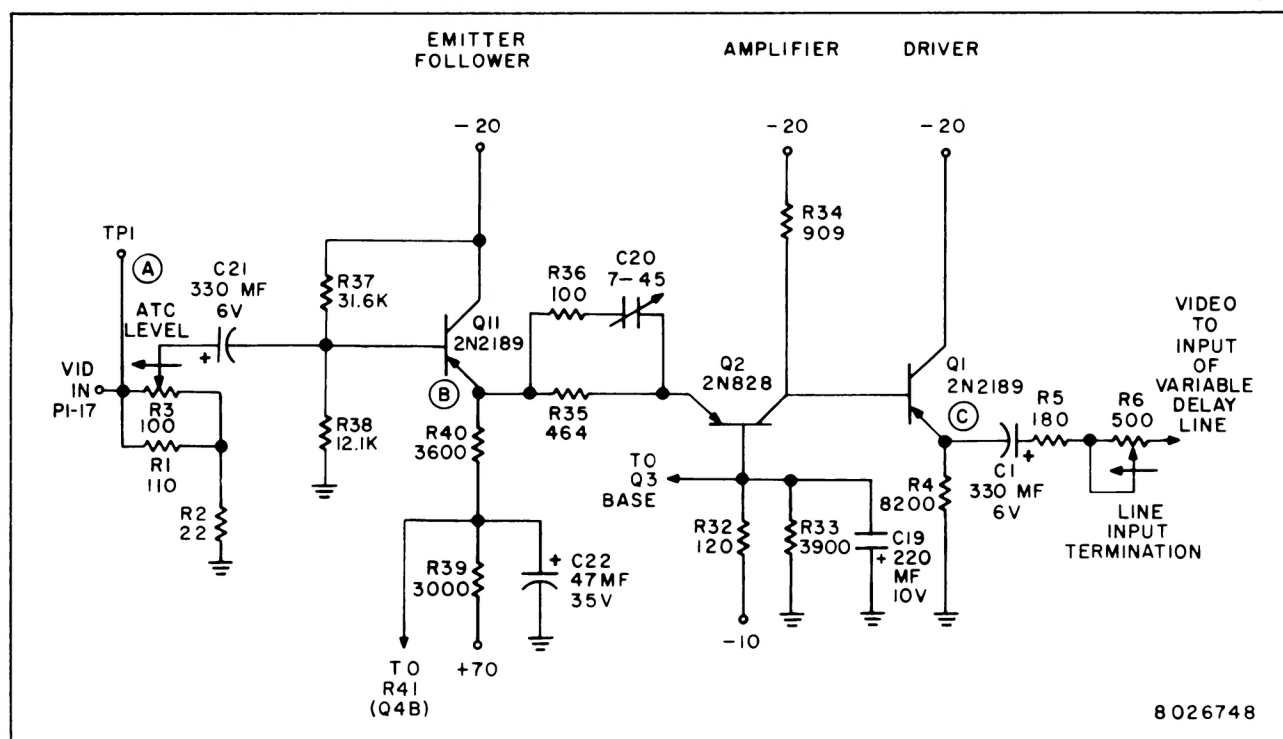
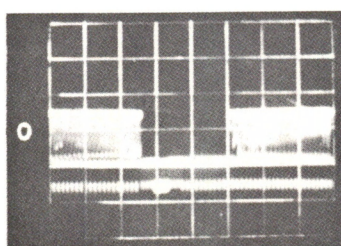
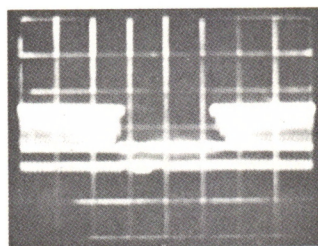


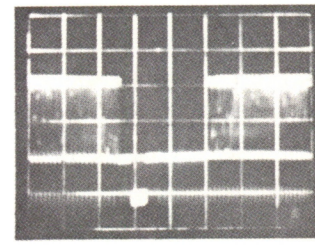
Figure 184—Video Input Amplifiers, Module 223



A. TPI, 0.5 ms/cm,
0.2 v/cm.



B. Q11 emitter, 0.5 ms/cm,
0.2 v/cm.



C. Q1 base, 0.5 ms/cm,
0.2 v/cm.

Figure 185—Typical Waveforms; Video Input Amplifiers Module 223

output from the collector of Q2 is fed to emitter follower Q1, which acts as the driver for the variable delay line (see figure 185C). Q1 provides a high input impedance to the incoming video signal, and a low input impedance to the variable delay line. The input termination can be adjusted by potentiometer R6, between the output of Q1 and the input to the line.

Electronically Variable Delay Line

The electronically variable delay line (figure 186) consists of 84 sections composed of iron core coils connected in series and silicon diode capacitors. The line is mounted on the board in the form of a horse-shoe, to fit it into the module length without introducing any discontinuities. Two silicon diodes are connected to the beginning and end of each coil as

shown in figure 186. The anodes of the odd numbered diodes, and the cathodes of the even numbered diodes are connected to the coils. The cathodes of odd numbered diodes CR1 through CR83 are connected to the positive error bus (PEB), and the anodes of even numbered diodes CR2 through CR84 are connected to the negative error bus (NEB). Similarly, the cathodes of odd numbered diodes CR85 through CR169 are connected to the delayed positive error bus (DPEB) and the anodes of even numbered diodes CR86 through CR170 are connected to the delayed negative error bus (DNEB). This arrangement divides the line into two halves joined in the center by coil L42. A negative 10 volt dc bias from a precision voltage divider on board 2 of module 225 is fed to the

center section of the line through R7, and the PEB, NEB, DPEB, and DNEB error signals from module 225 are applied to their respective error busses. The dc levels on the positive error busses are maintained at approximately +2.9 volts with respect to the reference voltage fed to the center, and the dc levels on the negative error busses are maintained at approximately -2.9 volts with respect to the reference voltage (See figure 187C). Fixed capacitors (C3, C4, C5, C6) are connected from each error bus to ground to provide a low impedance at high frequencies. The video signal from the LINE IN TERM potentiometer, R6, is fed into the line at coil L1 (figure 187A) and the video output signal is fed from coil L84 (figure 187B) through C5, R8, and LINE OUT TERM potentiometer, R9, to common base amplifier Q3 in the video output amplifier.

The dc levels on the four error busses are controlled by the THA circuits so that the average reverse bias on the silicon diodes, measured between the busses and the center section of the line is approximately 2.9 volts. When no timing error exists, the voltage at the output of the error detector, Q21, on module 225 is approximately 4.5 volts and the absolute value of the dc voltages on the four busses with respect to the section is approximately 2.9 volts. Under these conditions, the total delay provided by the variable delay line is approximately 3.1 microseconds. This delay is in the center of the correction range. When the absolute value of the dc voltage on the error busses increases, the time delay decreases. Conversely, when the absolute value decreases the delay increases.

The relation between the error voltages on the

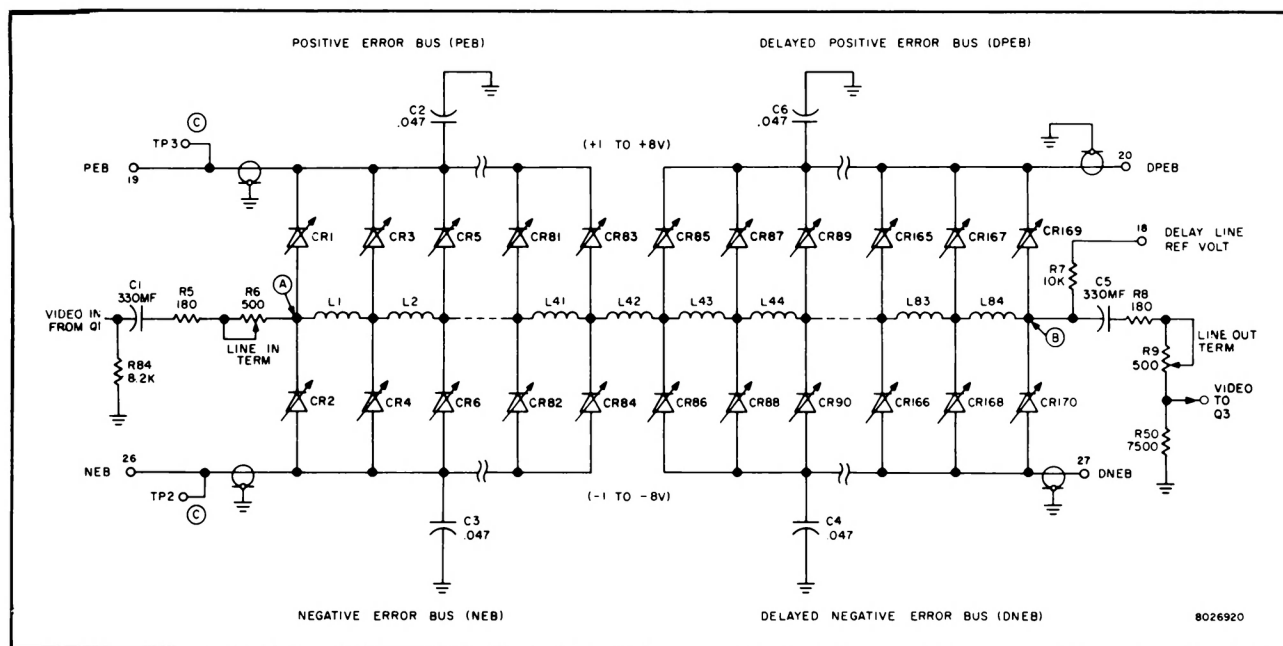
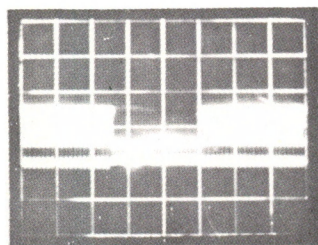
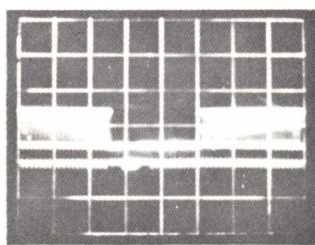


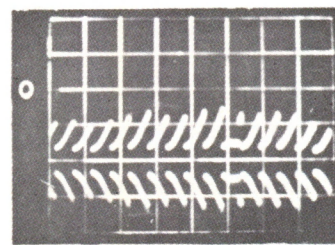
Figure 186—Electronically Variable Delay Line



A. Junction CR1, L1, 0.5 ms/cm, 0.2v/cm



B. Junction CR169, L84, 0.5 ms/cm, 0.2v/cm.



C. Top: PEB, 2 ms/cm, 5v/cm, Bottom: NEB, 2 ms/cm, 5v/cm. (PLAY mode, 223 S1 on COLOR OFF)

Figure 187—Typical Waveforms; Electronically Variable Delay Lines

busses and the delay of the line is non-linear. (The capacitance versus voltage characteristic of the silicon diodes is highly non-linear and the delay varies as the square root of capacitance which is a further non-linearity.)

The absolute error voltages range from +1 to +8 volts. At the lower end of the voltage range the delay of the line is approximately 3.7 microseconds, and at the upper end of the voltage range the delay is approximately 2.5 microseconds.

The overall relationship between timing error and timing correction is linear because the non-linear amplifier between the ATC error detector on module 225, and the error busses equalize the characteristic curve of the delay line. (See description of non-linear amplifier in the section on Module 225, Board 2.)

Video Output Amplifier Section (Q3, Q4, Q5, Q6 and CR174, CR175)

The video output amplifier section (see figure 188) amplifies the video output of the variable delay line to the level required by the output line driver circuit, and applies automatic post equalization that keeps the response flat throughout the control range of the delay line. The circuit consists of a common base amplifier, Q3, two video amplifiers, Q4, Q5, and an emitter follower, Q6. Two silicon diodes, CR174, CR175, provide a variable capacitance in the feedback circuit between the emitter of Q5 and the base of Q4, which is controlled by the PEB and NEB signals, to provide post equalization.

Video from the LINE OUT TERMINATION potentiometer, R9, is applied to the emitter of common base amplifier Q3. This stage provides the low input impedance required by the line, and acts as a voltage amplifier. Base bias for Q3 and collector supply voltage for Q4 are obtained from the base of Q2 in the video input amplifier section (see figure 184). The input to Q3 has an amplitude of about 0.4 volts peak-to-peak, and the output has an amplitude of 0.1 volt (see waveforms in figure 189A, B).

Video amplifier Q4 increases the amplitude of the video signal to about 2 volts peak-to-peak and inverts the signal (figure 189C). Q5 acts as an inverter and provides essentially no gain (figure 189D). Base bias for Q4 is obtained from a voltage divider in the video input amplifier section. Two silicon diodes, CR174 and CR175 provide a variable capacitance to ground at the center of a voltage divider which pro-

vides feedback from the emitter of Q5 to the base of Q4. The anode of CR175 and cathode CR174 are connected through resistor R43 to the -10 volt (nominal) delay line reference voltage. The anode of CR174 is connected to the NEB through resistor R44, while, the cathode of CR175 is connected to the PEB through R46. As the error signals vary, the reverse bias of the diodes, and the resulting capacitance to ground changes. This maintains the overall response of the line flat throughout the correction range.

The output of Q5 is fed directly to emitter follower Q6, and then ac coupled to emitter follower Q7 in the output line driver circuit. The video output of Q6 has negative going sync pulses and an amplitude of 2 volts peak-to-peak (figure 189E).

Output Line Driver (Q7, Q8, Q9, Q10)

The output line driver (see figure 190) consists of two emitter followers, Q7, Q8, and a series line driver Q9, Q10. Q7 is a PNP type and Q8, an NPN. Signal from the collector of Q9 is fed through capacitor C13 to the base of Q10. A Zener diode, CR173, provides a constant voltage difference of 12 volts between the collector of Q9 and the base of Q10. The output is taken from the junction of the emitter of Q9 and the collector of Q10 (figure 191B) and fed through individual resistors and capacitors to four outputs. The resistors provide the required 75 ohm terminations to the coaxial lines, and the capacitors block the dc. The first output, at P1-29, goes to color ATC system. The second, which is the main video output of the monochrome ATC system, goes through P1-30 and relays 11K21 and 11K11 to the input of module 131A, and to the input of a clamped sync separator on module 226. (The sync separator provides sync to the processing amplifier, and to the color ATC system). The third and fourth outputs, at P1-31 and P1-32 go to the CRO and picture monitor respectively. Outputs 2, 3, and 4 are provided with individual test points, TP4, TP5, TP6 (see figure 191C, D, E).

When the video outputs are properly terminated with 75 ohms and the input voltage at the junction of L1 and CR1 is set at 0.3 volts peak-to-peak the amplitude of the signal at the outputs is 1 volt.

Because relays 11K11 and 11K21 either terminate or unterminate the output at TP4, depending on the ATC mode, the level at this point depends on the position of the ATC function selector switch, S1 as follows:

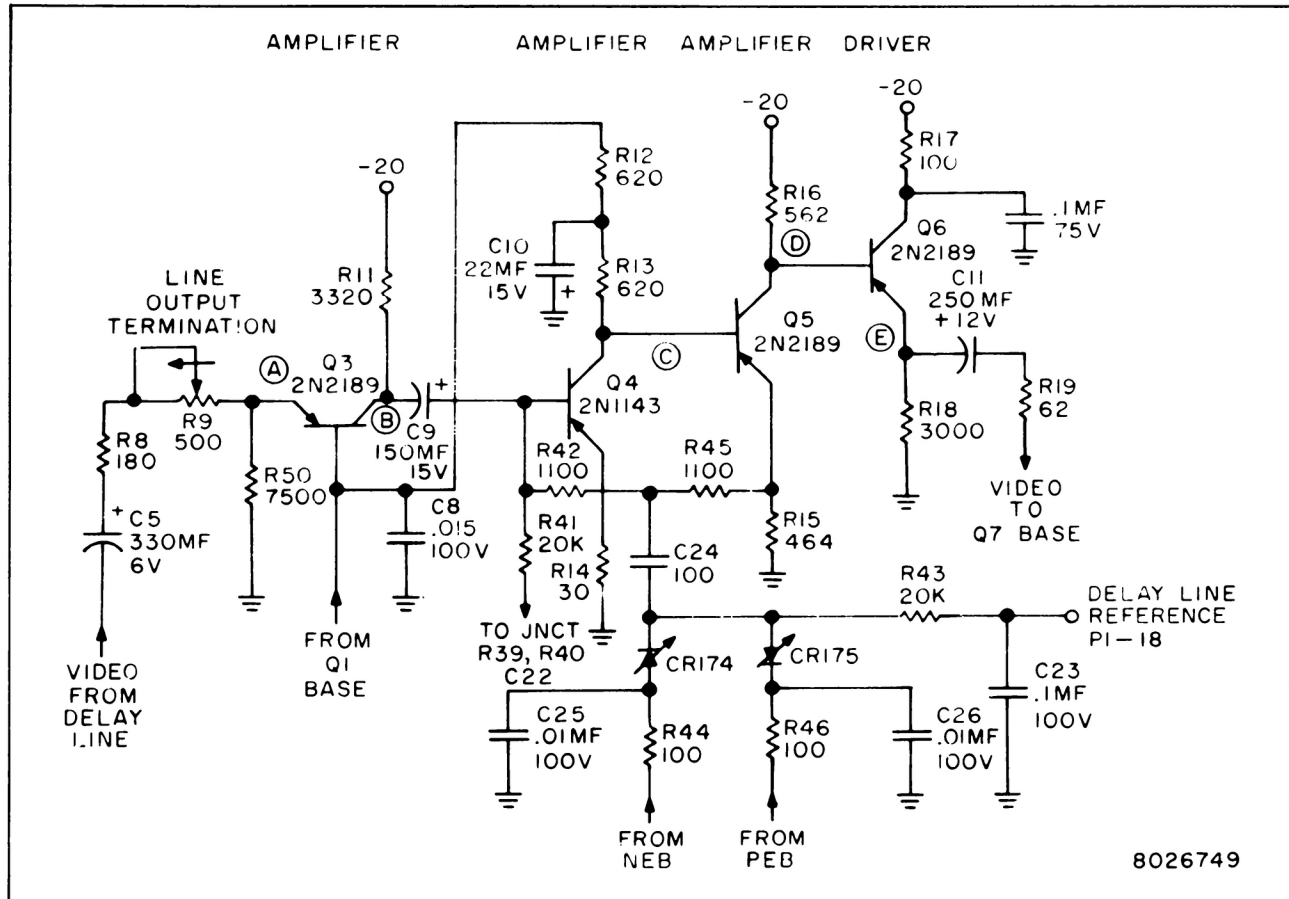
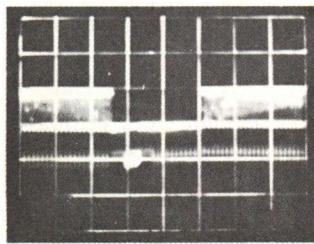
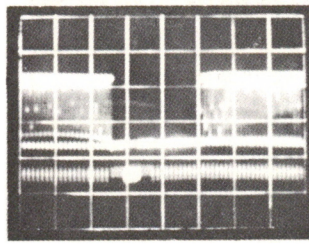


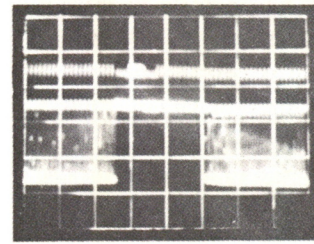
Figure 188—Delay Line Output Amplifier, Module 223



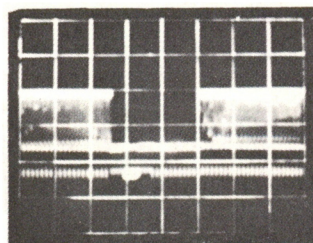
A. Q3 emitter, 0.5 ms/cm, 0.02v/cm.



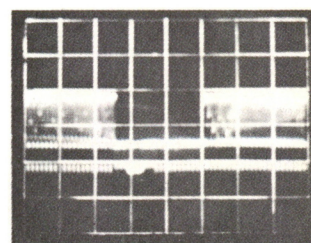
B. Q3 collector, 0.5 ms/cm, 0.05v/cm.



C. Q4 collector, 0.5 ms/cm, 0.5v/cm.



D. Q5 collector, 0.5 ms/cm, 1v/cm.



E. Q6 emitter, 0.5 ms/cm, 1v/cm.

Figure 189—Typical Waveforms; Delay Line Output Amplifiers, Module 223

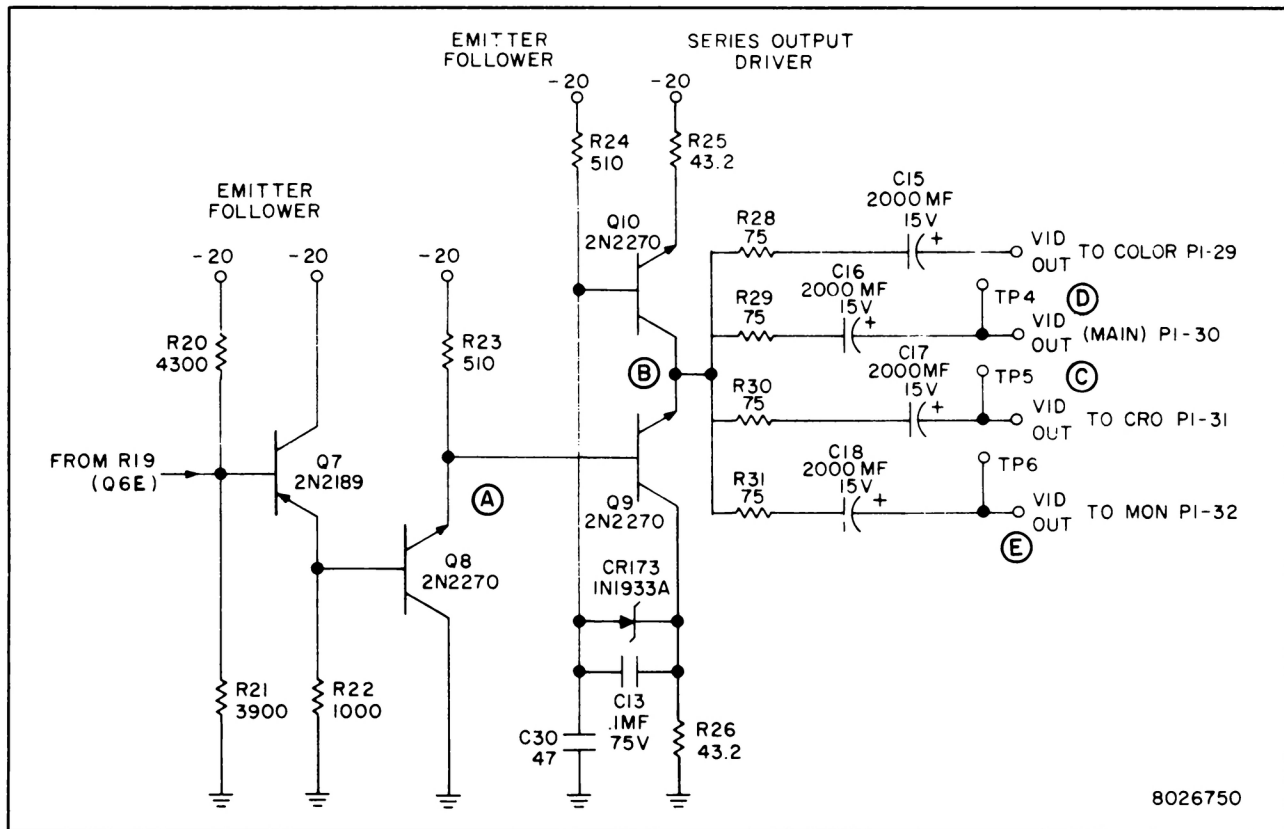
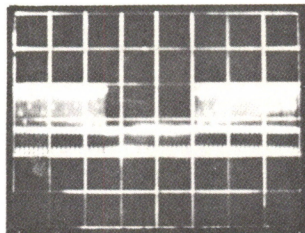
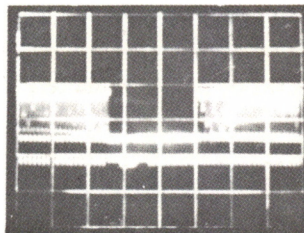


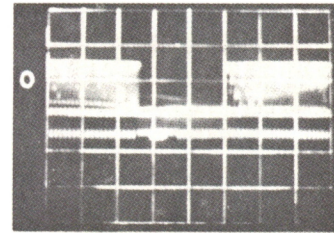
Figure 190—Output Line Driver, Module 223



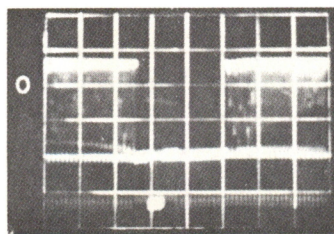
A. Q8 emitter, 0.5 ms/cm, 1v/cm.



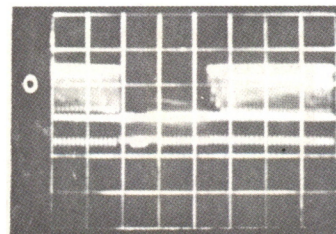
B. Q9 emitter, 0.5 ms/cm, 1v/cm.



C. TP5, 0.5 ms/cm, 0.2v/cm. (S1 on ATC OFF)



D. TP4, 0.5 ms/cm, 0.5v/cm (S1 on ATC OFF)



E. TP6, 0.5 ms/cm, 0.5v/cm.

Figure 191—Typical Waveforms; Output Line Driver, Module 223

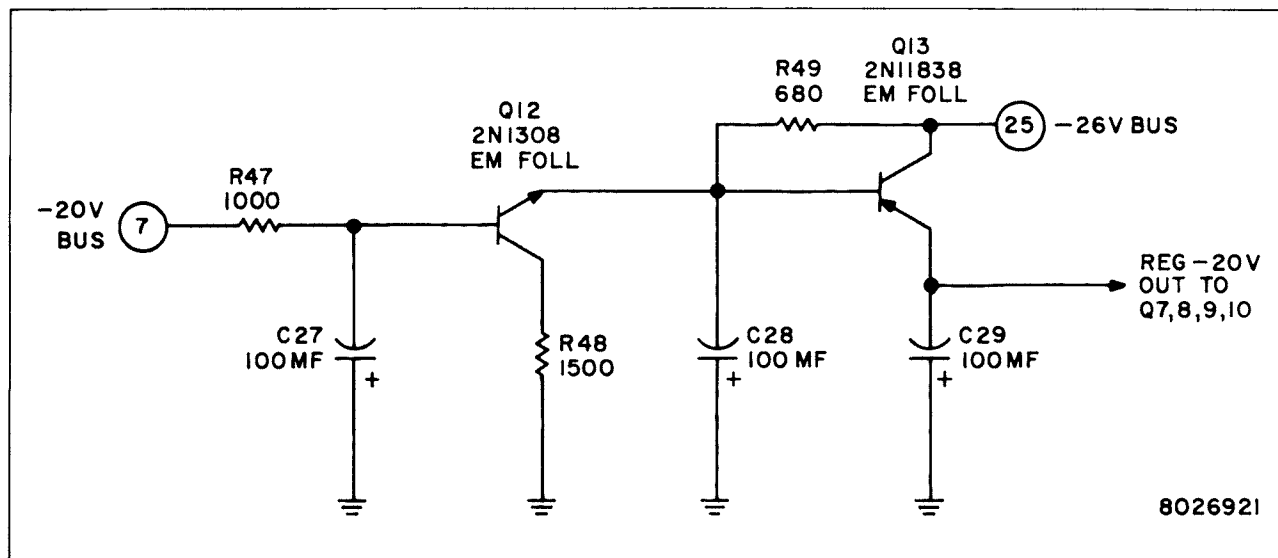


Figure 192—20-volt Voltage Regulator, Module 223

S1 Position	TP4 Output
ATC OFF	2 volts
COLOR OFF	1 volt
COLOR ATC	1 volt*
NON-PHASED COLOR	1 volt*

Voltage Regulator (Q12, Q13)

The -20 volt supply voltage for stages Q7, Q8, Q9, Q10 is obtained from a voltage regulator (see figure 192) which uses the recorder regulated -20 volt bus as reference and derives its power from -26 volts. The voltage regulator consists of two emitter followers in cascade, Q12 and Q13. The -20 volt bus is connected to the base of Q12 through R47, and the emitter of Q12 is connected to the -26 volt bus through R49. Therefore, the emitter of Q12 will be approximately at -20 volts because of the emitter-base diode action. A 100 mf filter capacitor, C27, is connected between the base and ground. Since the input impedance of the circuit is about Beta times the output impedance, the filtering effect of this capacitor is Beta times as great as if it were connected from the emitter to ground. Thus the emitter circuit is isolated from the -20 volt bus. The emitter of Q12 is directly connected to the base of Q13. The emitter of Q13 provides -20 volts from the -26 supply. Additional filtering is provided by 100 mf capacitor C28 from the base to ground, and C29, from the emitter to ground.

AUX HOR PHASE CONTROL (R51)

The AUX HOR PHASE control, R51 (see figure

183) is a screw driver adjusted potentiometer on the front panel of module 223A, that permits adjusting the phase of tape sync with respect to local sync when the system is in the external mode. Although the potentiometer is mounted on module 223A, the circuits that it controls are on board 1 of module 226. One end of the potentiometer is connected through P1-7 to the -20 volt bus. The other end and the arm are connected through P1-5 and pin 12 of the connector on module 226B to normally open contacts of relay K2 on module 226B. In the external mode only, the contacts connect the potentiometer to delay control stage Q18 in the AFC sample pulse circuits on module 226.

When the ATC function selector switch S1, on the front panel of module 223A, is in the NORM or COLOR OFF positions, relay K2 in module 226 is energized. Under these conditions adjustment of R51 varies the current supplied by delay control stage Q18 on module 226 to delay generator Q17. The current variation, in turn, changes the delay of the AFC sample pulse. This action, through the effect of the ATC reference circuits and THA loop on the head-wheel servo system change the phase of tape sync at the input to the ATC system. (See *overall timing of ATC reference circuits* in the section on module 226B).

Actually R51 is merely an auxiliary screwdriver adjustment which permits compensating for changes in tape horizontal phasing introduced by the ATC system. The main horizontal phasing adjustment, R1, is an operating control with a knob, which is mounted on the front panel of the Lineclock module, 316A. When the ATC system is in the bypass condition, R1 is connected directly to delay generator on the line-

*2 volts if machine includes color ATC.

lock module, and R51 is disabled. Under these conditions R1 is adjusted until the demodulated tape sync coincides with the incoming local sync. The adjustment is performed while viewing incoming video and tape video simultaneously on the CRO (VID IN and VID OUT buttons on the CRO monitor switcher pressed simultaneously).

When the system is in the external mode, R1 on the Linelock module is connected (by relays K2 and K3 on module 226B) in parallel with R51, on module 223 to delay control stage Q18 on module 226. Under these conditions the setting of R1 is normally not disturbed from the position determined in the bypass mode, but R51 is adjusted so that the tape sync at the output of the monochrome ATC system lines up with external horizontal sync (VID IN and VID OUT buttons pressed on CRO). Thus, with both controls properly adjusted tape sync at the outgoing line from the recorder will coincide with local sync whether the machine is in the monochrome ATC or bypass modes.

ATC Function Selector Switch (S1)

The ATC function selector switch, S1, on the front panel of module 223, permits selecting the mode of operation of the ATC system. The switch has four positions marked NON-PHASED COLOR, COLOR ATC, COLOR OFF, and ATC OFF. The arm of the switch is connected to ground. In the ATC OFF position, S1 is open, and since monochrome bypass relays 11K11 and 11K12 on the ATC relay bank cannot be energized, the ATC system is in the bypass condition. In the COLOR OFF position, the anode of CR171 is returned to ground through the arm of S1. The cathode of CR171 goes to the ATC module interlock bus which runs through jumpers in the connectors of modules 223, 225, and 226, to the coils of 11K11 and 11K12. Thus, if the three modules are in place the two relays become energized and unbypass the Monochrome ATC system. In the COLOR ATC position, the switch grounds a control bus to the color ATC interlock system through diode CR178 and grounds the monochrome interlock bus previously described through diode CR172. In the NPC position the switch grounds the MATC bus only, through diode CR176.

NOTE

For details on the relay circuits see *ATC Control and Indicator Circuits* in the *System* section.

MODULE 223, MAINTENANCE

The following equipment will be required for mak-

ing the maintenance adjustments on the Delay/Output Module:

1. Oscilloscope (Tektronix 535A or equivalent).
2. VoltOhmyst.
3. Module extender.

The maintenance adjustments have been carefully performed at the factory. The screwdriver type potentiometers are locked in position and should not require readjustment unless the settings have been changed.

Video Input Level to Variable Delay Line

1. Install a tape containing a monoscope signal on the recorder. Place module 223 on an extender and turn the ATC function selector switch, S1, on the front panel of the module to the ATC OFF position. Leave the switch in this position unless otherwise directed. Place the machine in Play mode.

2. Connect oscilloscope to TP3 FIXED VIDEO on 303A and adjust demodulator level on module 205 to read 1 volt peak-to-peak. Move oscilloscope probe to test point TP1 on the front panel of module 303A and adjust the video LEVEL control on the front panel of module 131B until the amplitude of the video signal on the oscilloscope is 1 volt peak-to-peak. Check to see that the same level is present at TP2 of module 303A.

NOTE

If the ATC function selector switch, S1, is placed in the COLOR OFF or NORM position instead of the ATC OFF position, TP2 of module 303A becomes unterminated and the video level at that point rises to 2 volts. However, the video levels at TP1, TP3, and TP4 of module 303A remain at 1 volt.

3. Connect the oscilloscope between the junction of CR1 and L1, and ground on module 223. Loosen the locknut on potentiometer R3 on module 223 and adjust R3 for a video level of 0.3 volts on the oscilloscope.

4. Connect the oscilloscope to the VID 1 test jack on module 223. With the ATC function selector in the ATC OFF position, the video level should be 2 volts.

5. Change the position of the ATC function selector to the COLOR OFF position. The VID 1 output level should become 1 volt peak-to-peak.

6. Place the function selector switch in the NORM position. If the system does not include color ATC the VID 1 output should be 1 volt. If the system contains color ATC, the VID 1 output level should be

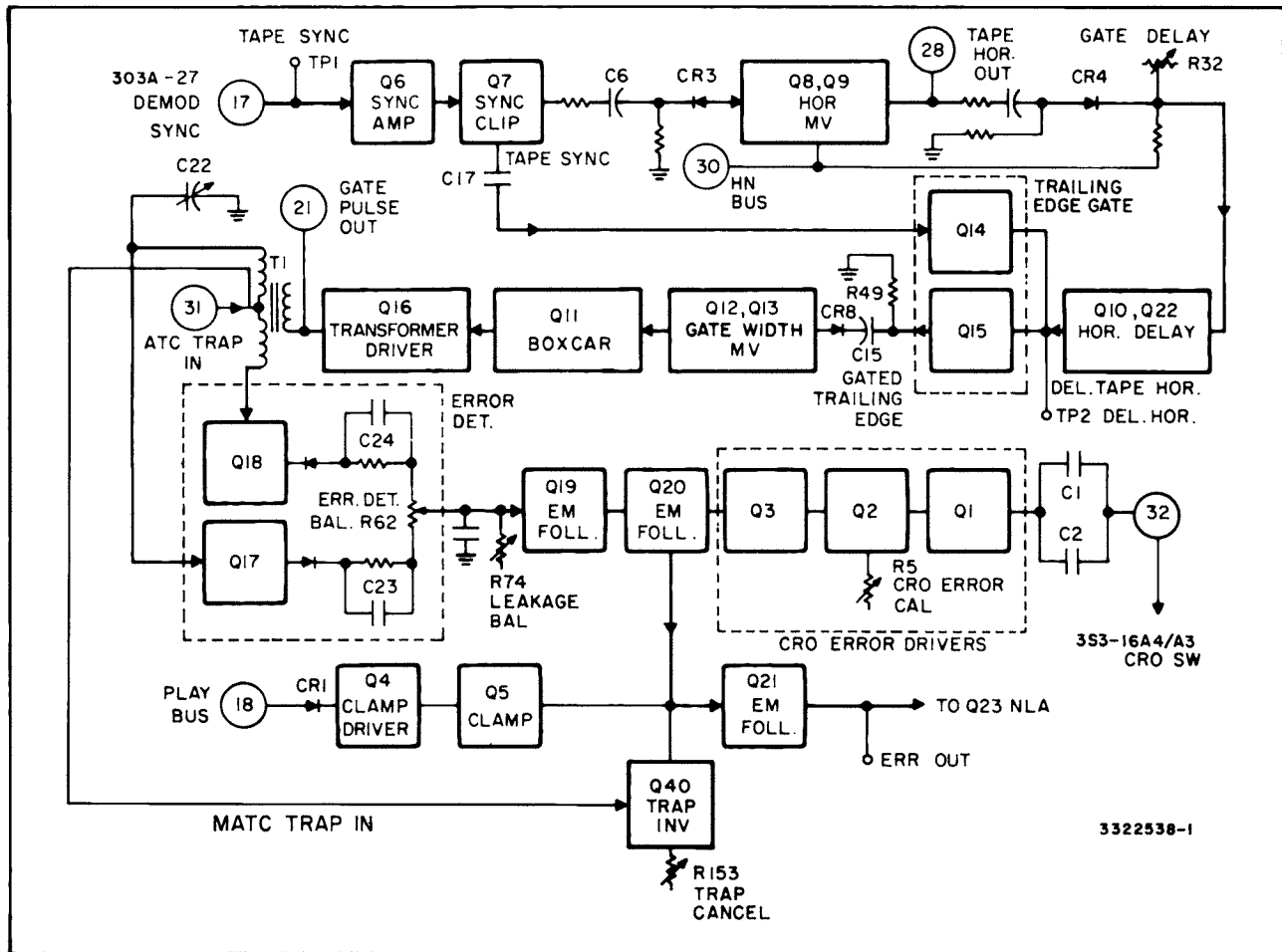


Figure 193—Block Diagram, ATC Error Detector, Module 225, Board 1

1 volt on monochrome standards or 2 volts on color standards.

Terminations of Variable Delay Line

1. Install a tape containing a monoscope signal. Place module 223 on an extender. With the machine in PLAY check the adjustment of R3 on module 223 as directed in steps 1, 2, and 3 under *Video Input Level to Variable Delay Line*. Do not change the adjustment of R3 unless necessary.

2. Place the guide servo in MANUAL. Press the DEMOD OUT button on the picture monitor and the ATC ERROR button of the CRO. Adjust the PB GUIDE POSITION control on the front panel of the Guide Servo Module for a light guide pressure producing a 1 microsecond error. (Light pressure is obtained when the jogs on the picture monitor slant upward to the right, and an error of 1 microsecond is present when the amplitude of any one slanted dotted line on the CRO graticule is 100 I.R.E. units.)

3. Make certain that Demodulator Module, 203B, is balanced and that the video heads are equalized.

4. Press ATC OUT button of picture monitor. Reduce the brightness of the picture and increase the contrast until shading and reflections are visible.

5. Observe the shading on the left side of the picture. In each 16-line segment the shading will progress from dark to light. Adjust the line termination potentiometers, R6 and R9 on module 223, until the shading becomes even and blends with the background.

6. Readjust R3 to maintain a video level of 0.3 volts at the junction of CR1 and L1 on module 223 (with a level of 1 volt at TP1 of module 303A3).

7. Press ATC OUT button of the CRO and slightly readjust R9 to obtain a video output level on the CRO as close to 1 volt as possible without making the ghosts following the large circle on the picture monitor apparent.

8. With the external oscilloscope connected to the junction of CR1 and L1, slightly retouch R6 and R9 until the optimum settings are obtained, as in step 7, while keeping R3 adjusted to maintain a level of 0.3 volts at CR1.

9. Press the DEMOD OUT button on the picture monitor and the ATC ERROR button of the CRO. Adjust the PB GUIDE POSITION control on the guide servo module for a heavy pressure producing a 1 microsecond error (jogs on picture monitor slanting upward to the left, and amplitude of any one dotted line on CRO equal to 100 I.R.E. units).

10. Check for shading and ghosts as directed in steps 5 through 8 and, if necessary retouch R3, R6, and R9. The final conditions should be optimum for both heavy and light guide pressure.

11. Remove module from extender and tighten the locknuts on R3, R6, and R9.

Servicing the Variable Delay Line

Should accidental damage to the line occur, it will be indicated by ghosts and/or reflections which cannot be eliminated by adjusting R3, R6, or R9. The following checks may assist in locating the defective component.

1. Measure the total resistance of the center (video section) of the variable delay line. The value is approximately 32 ohms.

2. Check the dc levels on the error busses. Under zero errors conditions the voltage from the video section of the line to ground should be approximately -9.9 volts. With respect to the video section, the PEB should be 2.9 volts positive and the NEB, 2.9 volts negative.

3. If a particular coil or diode presents visual appearance of damage carefully remove it from the line and check it with a Tektronix LC 130 meter. The capacitance of a normal diode is between 119 and 128 $\mu\mu\text{f}$, and the inductance of a normal coil is between 8 and 9 μh .

NOTE

If it is not possible to locate the defective coil or diode by routine trouble shooting methods it is recommended that the RCA Service Company be consulted.

Coil Replacement

To replace a defective coil on the variable delay line, proceed as follows:

1. Remove the cement around the coil with a sharp knife.

2. Unsolder the leads and remove the coil.

3. Solder the white and red leads of the new coil to the same terminals as the original. Then cement the coil in place with coil cement.

IMPORTANT: Each coil in the variable delay line is color coded (brown, red, yellow, or blue) to indicate the range to which it belongs. When ordering a new coil specify the color code, in addition to the stock and drawing numbers given in the replacement parts list.

ATC ERROR DETECTOR (Module 225)

GENERAL

The ATC Error Detector Module is a single width module containing two circuit boards mounted back to back. The circuits on board 1 perform the following functions:

1. Process the tape sync signal from the Demodulator Output Module, 303A.

2. Gate the trailing edge of tape sync.

3. Detect the timing error of the trailing edge of tape sync.

4. Drive the non-linear amplifier (NLA) circuit on board 2.

5. Permit monitoring the ATC error voltage on the CRO.

6. Clamp the error voltage to a fixed value when the recorder is in any mode but PLAY.

Board 2 contains the non-linear amplifier and the tape horizontal alignment (THA) differential amplifier. The NLA converts the linear ATC error signal from board 1 to a non-linear signal and provides four outputs which drive the variable delay line on module 223. (A non-linear input for the variable delay line is necessary because the delay line is a non-linear device.) The THA differential amplifier provides feedback which keeps the average voltages on the output busses of the NLA in the center of the correction range of the variable delay line.

CIRCUITS ON MODULE 225, BOARD 1

Functional Description

Please refer to the block diagram, figure 193 and the two timing diagrams, figures 194 and 195, while reading the following description.

Tape Horizontal Sync Circuits

The tape horizontal sync circuits consist of an amplifier (Q6), clipper (Q7), horizontal multivibrator (Q8, Q9) and horizontal delay multivibrator (Q10, Q22). Tape sync from module 303A is fed to pin 17

of plug P1 on module 225. After amplification by Q6 and clipping by Q7 the sync is fed to horizontal multivibrator Q8, Q9, and also to Q14 in the trailing edge gate.

Multivibrator Q8, Q9 divides by two during the 9H interval of sync, and thus removes all vertical components. The output of Q9 (see figure 194B) is a negative pulse whose positive going or timed edge coincides with the leading edge of tape sync (figure 194A). This pulse is fed out through pin 28 of P1 to the ATC Reference Circuits on module 226, board 1, where it serves as the tape horizontal reference. The pulse is also fed to horizontal delay multivibrator Q10, Q22.

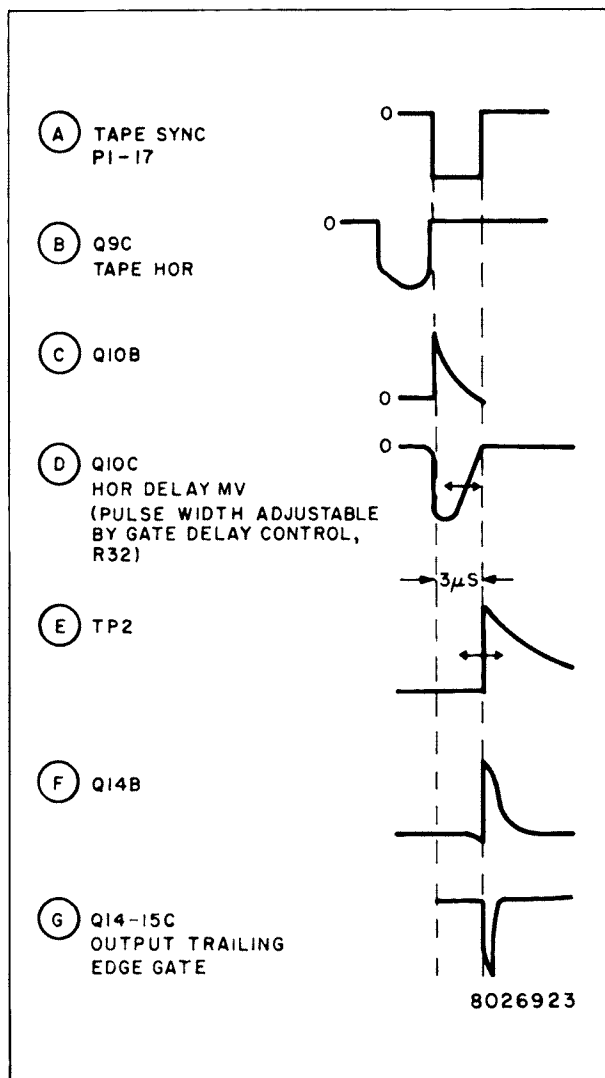
Delay multivibrator Q10, Q22, produces a pulse (figure 194D) whose width can be adjusted with GATE DELAY potentiometer, R32, on the front panel. This pulse is differentiated to form a relatively broad positive going triangular waveform, and then applied to Q15 in the trailing edge gate. The GATE DELAY control is normally adjusted so that the differentiated pulse starts 3.0 microseconds after the leading edge of tape sync. (See figure 194F).

ATC Sample Pulse Circuits

The ATC sample pulse circuits consist of a trailing edge gate (Q14, Q15), gate width multivibrator (Q12, Q13) and a boxcar (Q11). The trailing edge gate produces a narrow pulse whose leading edge coincides with the trailing edge of tape horizontal sync. Q12, Q13, and Q11 produce a sample pulse timed by the output of the trailing edge gate. This ATC sample pulse is compared with the ATC trapezoid derived from Q12 in the ATC Reference module 226.

The trailing edge gate produces an output only when both of its input signals are present. One of these inputs is the differentiated trailing edge of clipped sync from Q7 (figure 194F), and the other is the delayed horizontal pulse from Q10 (figure 194E). The pulse from Q7 occurs at the trailing edges of both horizontal sync and the half-width equalizing pulses. However, the delayed horizontal pulse is timed so that the gate opens only at the trailing edge of horizontal sync (see figure 194G).

The gate width multivibrator (Q12, Q13) eliminates noise and switching pulses which may be present in the output of the trailing edge gate during the back porch interval. Boxcar Q11 narrows the output of Q13 (figure 195C), which is approximately 30 microseconds wide, to 2 microseconds (see figure 195D). The output of Q11 which constitutes the ATC sample pulse, is fed to transformer driver Q16.



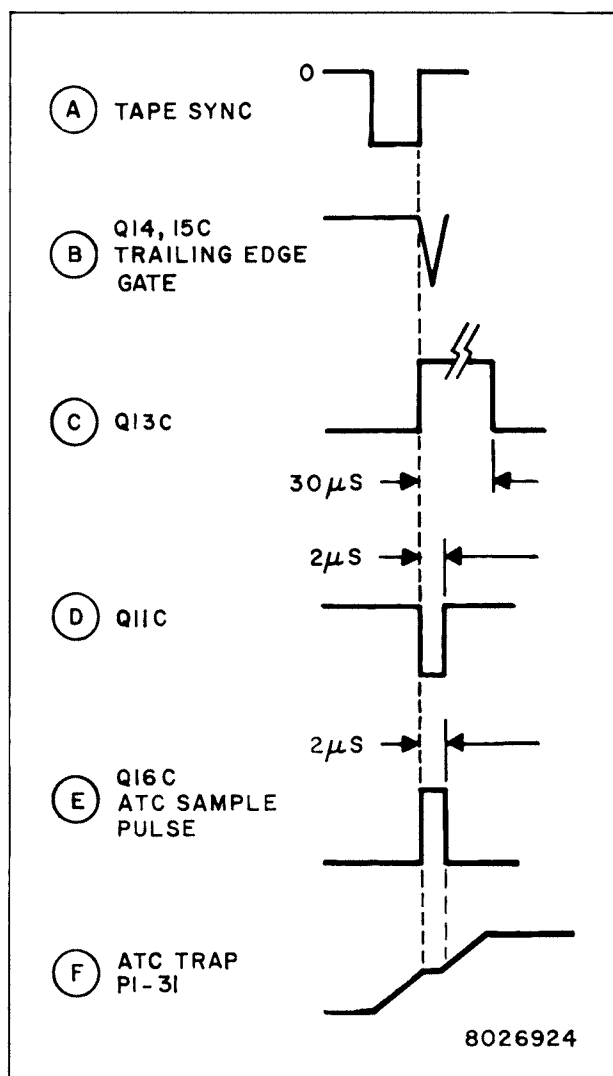
**Figure 194—Timing Relations,
ATC Error Detector**

ATC Error Detector and Output Circuits

The ATC error detector and output circuits consist of transformer driver Q16, phase splitting transformer T1, push-pull error detectors Q17, Q18, and emitter followers Q19, Q20, Q21. These circuits produce an error voltage linearly related to the phase difference between the ATC sample pulse and the ATC trapezoid. The ATC sample pulse (figure 195E) is fed from Q16 to the primary of T1 and also to pin 21 of plug P1. From pin 21 the pulse goes to module 226, board 1, where it gates a stage (Q5) that produces the step on the ATC trapezoid (figure 195F). The ATC trapezoid is fed from module 226, board 1, through pin 31 of P1 on module 225, to the center tap of the secondary of T1.

T1 splits the ATC sample pulse into two oppositely phased pulses, one of which is applied to Q17, and

the other to Q18. These two transistors conduct only at the sample pulse tips. The error signal, which is equal to the voltage on the trapezoid during the sample pulse, appears at the arm of the ERR DET BAL potentiometer, R62. This control is connected between the outputs of Q17 and Q18. A capacitor from the arm to ground holds the error voltage constant between sample pulses. R62 permits balancing the outputs of Q17 and Q18 so that transients which occur during the sampling pulse cancel each other at the arm. A trimmer capacitor, C22, permits balancing the input capacity of the two transistors. The error signal is fed through the three emitter followers, Q19, Q20 and Q21, which provide a very low output impedance and then to the input of the non-linear amplifier on board 2 of module 225.



**Figure 195—Timing Relations,
ATC Error Detector**

Error Voltage Clamp Circuit (Q4, Q5)

The error voltage clamp circuit consists of a driver, Q4, and a bidirectional switch, Q5. This circuit disables the ATC system by clamping the base of emitter follower Q21 to +4 volts when the recorder is in any mode but PLAY, AUDIO REC, or CUE REC.

CRO Drivers (Q3, Q2, Q1)

The three CRO drivers, Q3, Q2, Q1, amplify the ATC error signal obtained from output emitter follower Q20, to the level required for driving the CRO. Potentiometer R5 (CRO CAL), which varies the gain of Q2, permits calibrating the CRO scale so that 100 I.R.E. units correspond to 1 microsecond of timing error.

Circuit Descriptions Module 225, Board 1

Tape Horizontal Sync Circuits (see figure 196)

1. Sync Amplifier and Clipper (Q6, Q7).

A negative tape sync pulse approximately 4 volts in amplitude is fed from module 303A to P17-1 on module 225 and then ac coupled to the base of sync amplifier Q6. (This signal is shown in figure 197A and may be observed at the TAPE SYNC test point, TP1, on the front panel of module 225.) The base of Q6 is biased "on" at approximately -2.8 volts and the collector normally rests at approximately -12 volts. When the sync pulse is applied the collector goes towards ground (figure 197B) but is clamped to approximately -8 volts by the base-emitter diode action of sync clipper Q7, which saturates at that voltage. The collector of Q7 (figure 197C) is normally at ground but goes to approximately -8 volts on each sync pulse. The resulting -8 volt negative pulse, after differentiation, is used to trigger horizontal multivibrator Q8 and Q9. An additional output consisting of a six volt negative pulse, which is obtained from a tap on the collector resistance, is fed to trailing-edge gate transistor Q14.

2. Horizontal Multivibrator (Q8, Q9).

The negative sync pulse at the collector of transistor Q7 is differentiated by capacitor C6 and resistor R24, and the positive-going excursion of the differentiated waveform is limited by diode CR3. The negative going edge overcomes the normally "off" bias on the base of Q9 and triggers multivibrator Q8 and Q9. Just before Q9 conducts its collector (figure 197D) is at -20 volts, the base of Q8 is at ground, and therefore, capacitor C7 is charged to -20 volts. At the instant of conduction, the collector voltage of Q9 rises very rapidly to ground and the full 20 volt

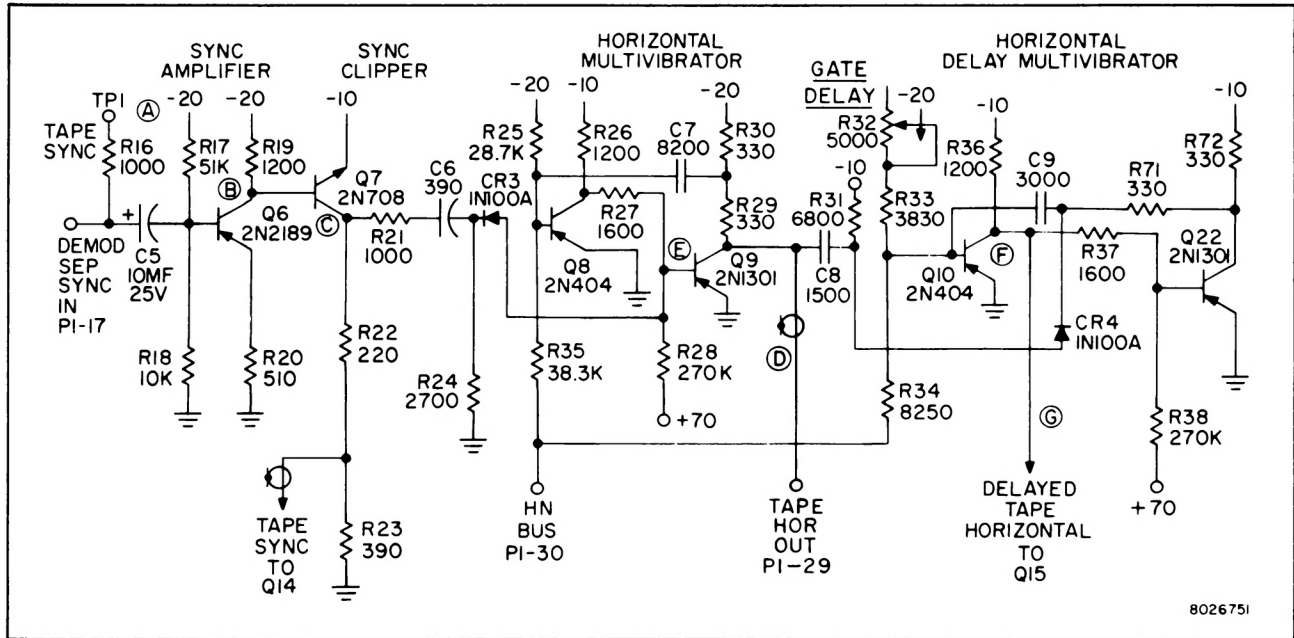


Figure 196—Tape Horizontal Circuits

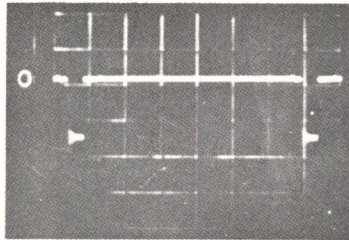
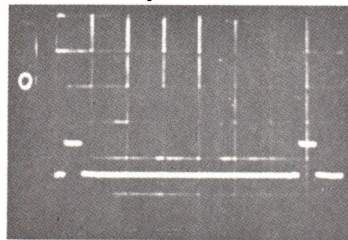
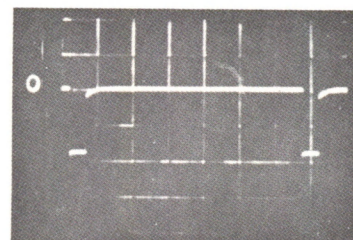
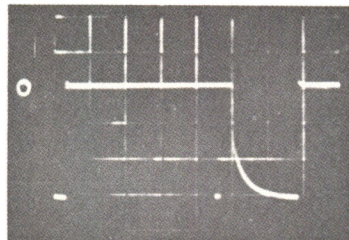
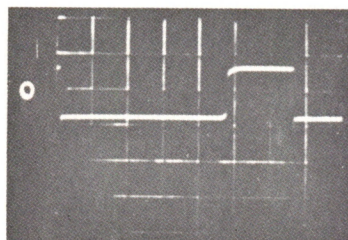
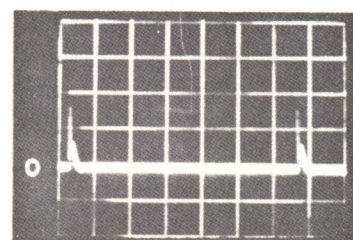
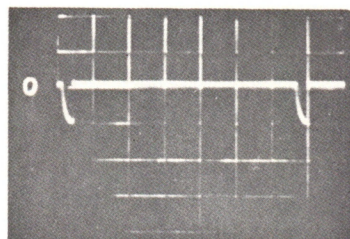
A. TP1, 10 $\mu\text{s}/\text{cm}$,
2v/cm.B. Q6 collector, 10 $\mu\text{s}/\text{cm}$,
5v/cm.C. Q7 collector, 10 $\mu\text{s}/\text{cm}$,
5v/cm.D. Q9 collector, 10 $\mu\text{s}/\text{cm}$,
5v/cm.E. Q9 base, 10 $\mu\text{s}/\text{cm}$,
0.5v/cm.F. Q10 base, 10 $\mu\text{s}/\text{cm}$,
2v/cm.G. Q10 collector, 10 $\mu\text{s}/\text{cm}$,
5v/cm.

Figure 197—Typical Waveforms; Tape Horizontal Circuits

charge across capacitor C7 is applied to the base of Q8. This action causes a positive pulse to be applied to the base of Q8, which cuts Q8 off, and starts the one-shot or unstable period of the multivibrator.

The duration of the unstable period is determined by the discharge rate of C7 through resistors R25 and R35. In 525-625 line TV systems both resistors are returned to -20 volts. However, in the 405-line system R35 is returned to ground and, since the voltage to which C7 discharges is reduced, the unstable period is lengthened. Since, in either system, the period is greater than half of a TV line the multivibrator divides by two during the 9H interval of vertical

blanking. Thus, the circuit removes all vertical components from the tape sync signal.

The output of the horizontal multivibrator, from the collector of Q9, is a 15 volt (approximately) negative horizontal pulse whose positive going edge is timed with the leading edge of tape sync (figure 197D). This pulse is fed to P1-29, and to a differentiating network consisting of C8, R31 and CR4. The output at P1-29 provides tape horizontal sync to the ATC Reference Module 226. The output of the differentiating network (figure 197F) triggers horizontal delay multivibrator, Q10, Q22.

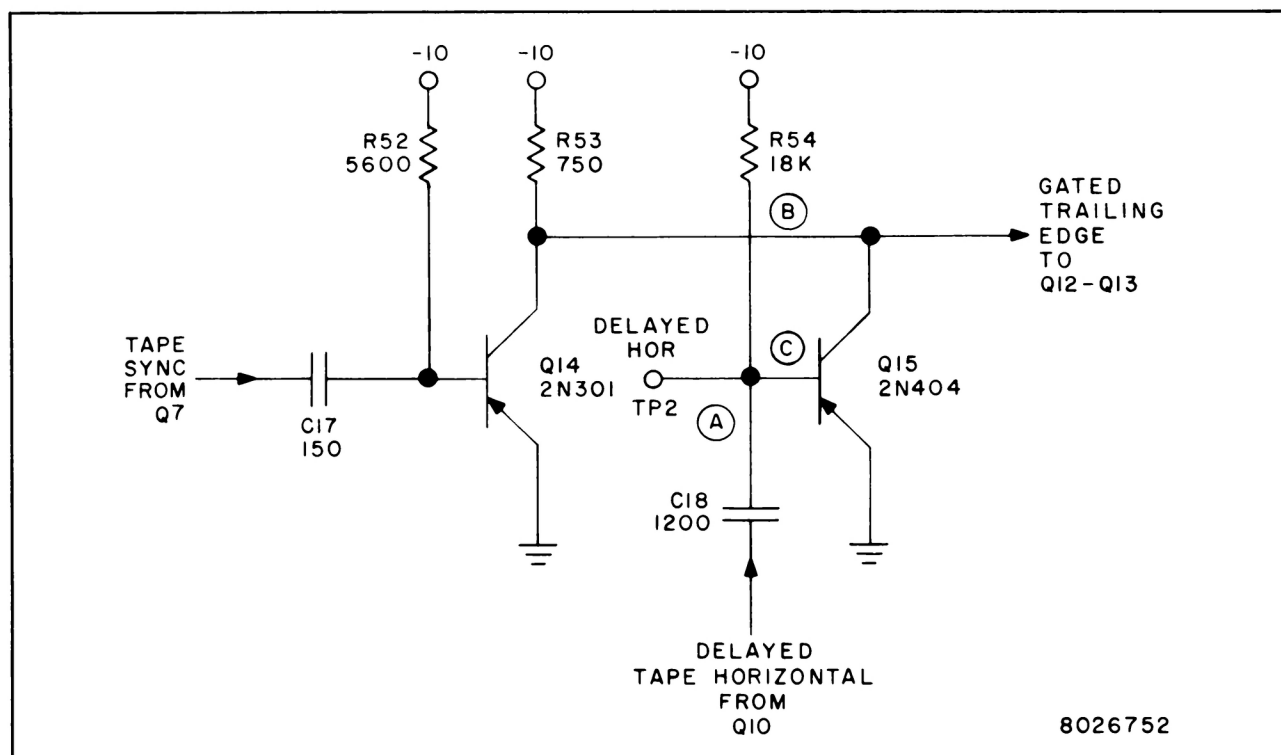


Figure 198—Trailing Edge Gate

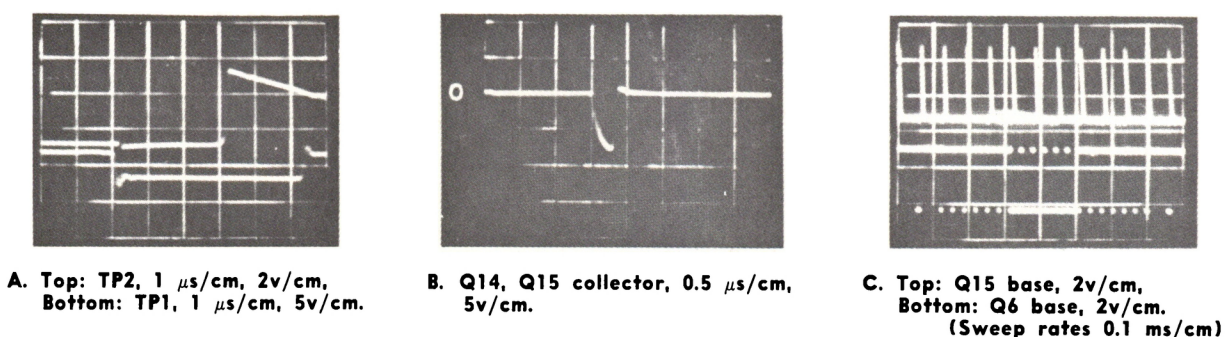
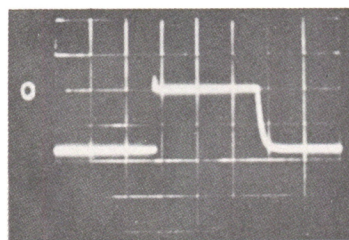
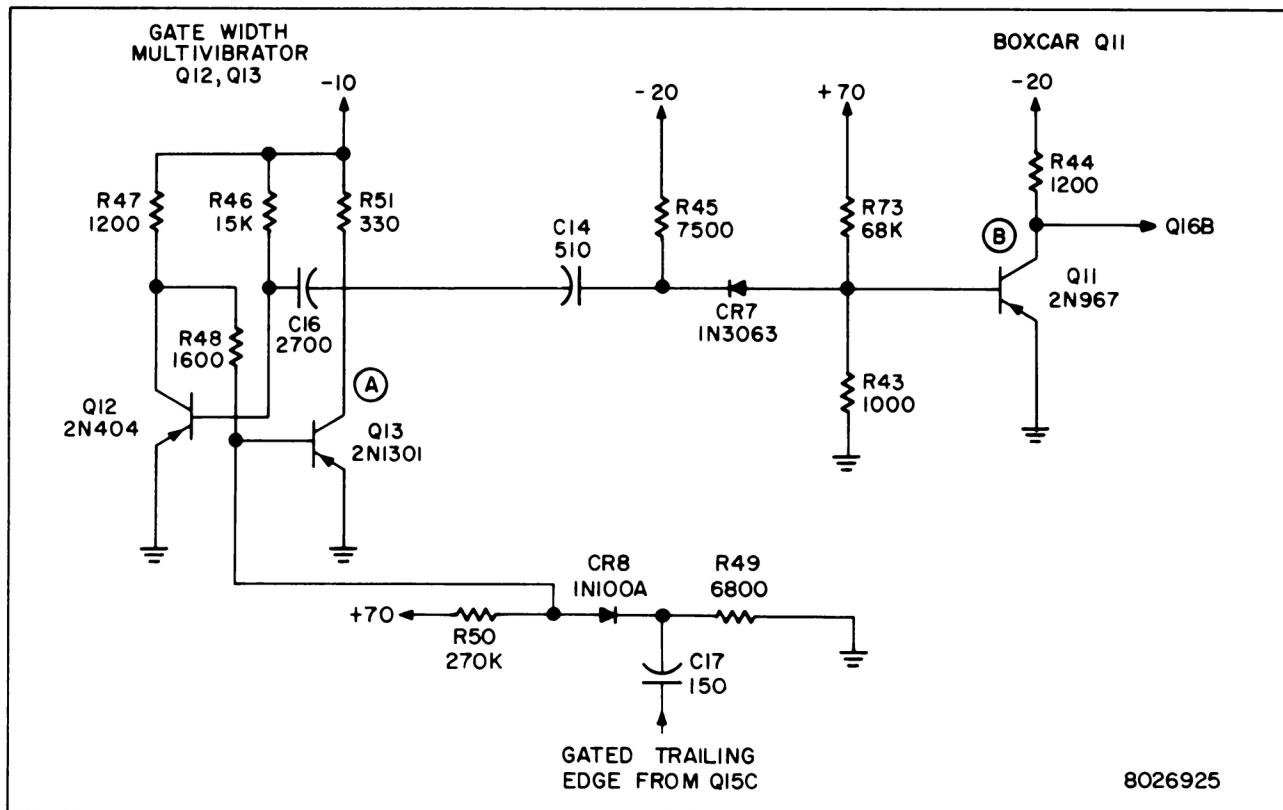
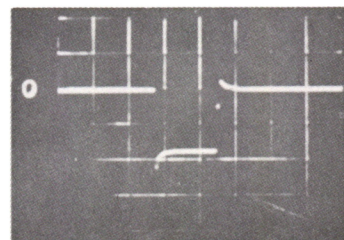


Figure 199—Typical Waveforms; Trailing Edge Gate



A. Q13 collector, 10 μ s/cm, 5v/cm.



B. Q11 collector, 1 μ s/cm, 5v/cm.

Figure 201—Typical Waveforms; Gate Width Multivibrator and Boxcar

3. Horizontal Delay Multivibrator (Q10, Q22).

The action of Q10 and Q22 is similar to that of the horizontal multivibrator, Q8, Q9 except that the circuit is triggered by the positive going edge of the differentiated waveform from CR4, and the width of the output pulse is adjustable. The duration of the unstable period is determined by the charging rate of capacitor C9. This rate depends upon the adjustment of GATE DELAY potentiometer, R32, and the voltage to which resistor R34 is returned through the HN bus. In 525-625 line systems the HN bus is at -20 volts. In 405-line systems the bus is grounded and, since the voltage to which C9 discharges is re-

duced, the length of the unstable period is increased.

The collector output of Q10 (figure 197G) is a negative pulse approximately 5 volts in amplitude whose width is adjustable (by GATE DELAY potentiometer, R32) from approximately 2 to 4 microseconds. The width is nominally set at 3 microseconds. The output pulse is differentiated by C18 and R54 and then applied to the base of Q15 in the trailing edge gate (see figure 198). The differentiated waveform may be observed at the DLY'D HOR test point, TP2, on the front panel of module 225 (see figure 199A).

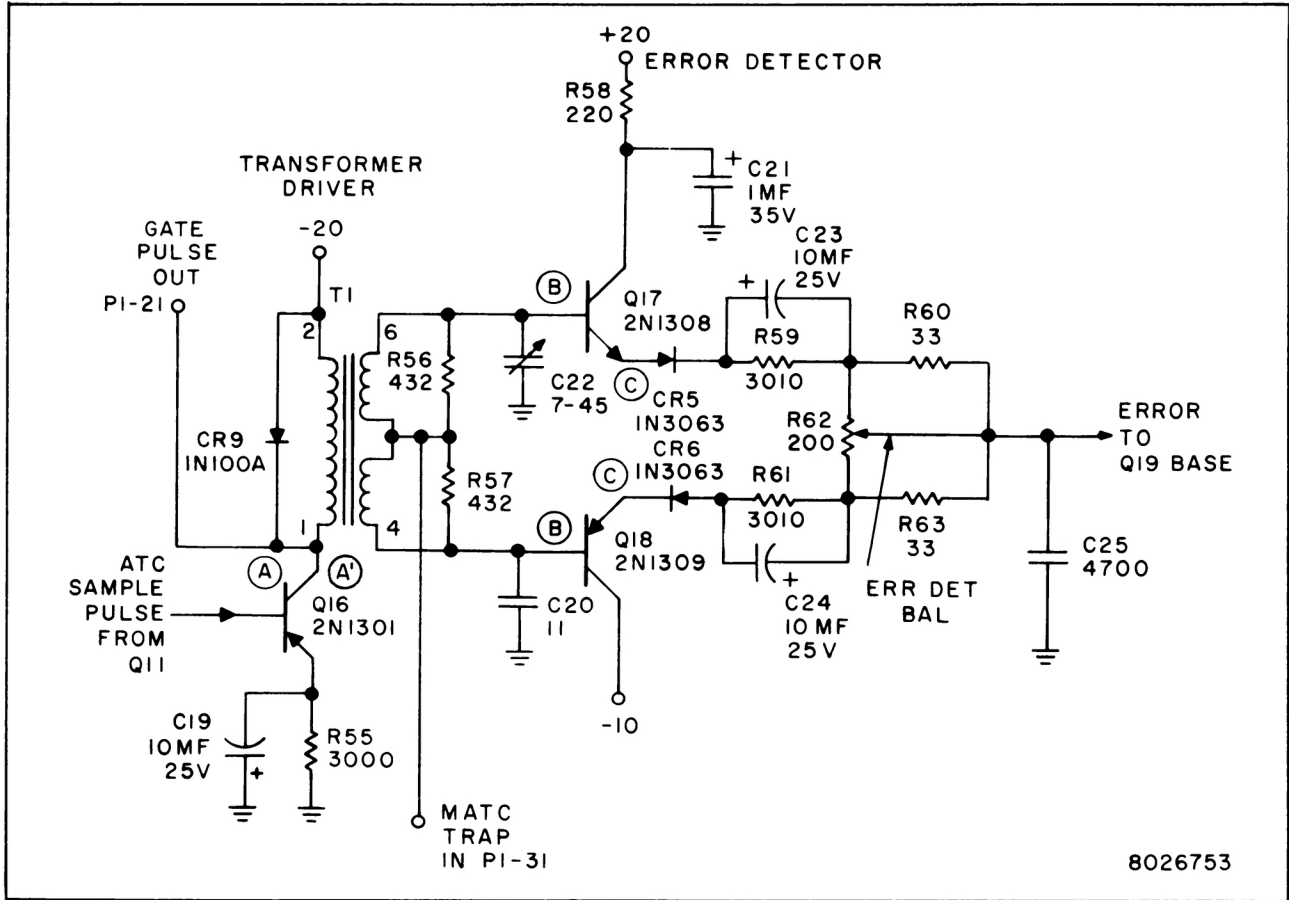
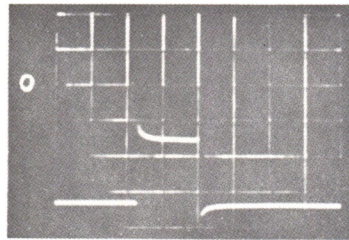
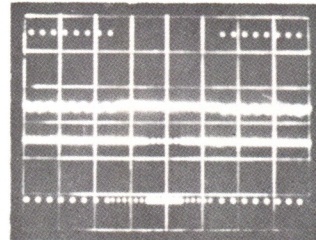


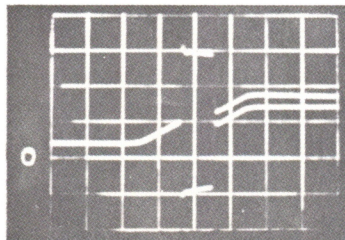
Figure 202—ATC Error Detector Circuit



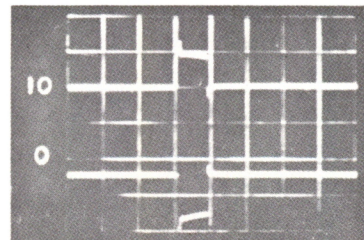
A. Q16 collector, 10 μ s/cm, 5v/cm.



A'. Top: Q16 collector, 5v/cm, Bottom: Q6 base, 2v/cm. (Sweep rates 0.2 ms/cm)



B. Top: Q17 base, 5v/cm, Bottom: Q18 base, 5v/cm. (Sweep rates 2 μ s/cm)



C. Top: Q17 emitter, 2v/cm, Bottom: Q16 emitter, 2v/cm. (Sweep rates 1 μ s/cm)

Figure 203—Typical Waveforms; ATC Error Detector Circuit

ATC Sample Pulse Circuits

1. Trailing Edge Gate (Q14, Q15).

As shown in figure 198 the trailing edge gate consists of a pulse former, Q14 and a pulse gate Q15. Normally, both transistors are conducting and the two collectors, which are tied together, are at ground. The delayed horizontal pulse applied to the base of Q15 starts nominally 3 microseconds after the leading edge of tape sync and is relatively broad (see figures 199A and C). This pulse cuts Q15 off, but the collector cannot immediately go to 10 volts because Q14 is still conducting when the pulse arrives. However, when the tape sync pulse is applied to the base of Q14 it is sharply differentiated and the positive going spike cuts Q14 off.

The resulting output of the trailing edge gate, on the collectors (figure 199B), is a negative going 7-volt pulse, approximately 0.5 microseconds wide, whose leading edge is timed with the trailing edge of tape sync. This pulse is differentiated by C17 and R49 (see figure 200), and the positive going spike is clipped by diode CR8. The negative going spike triggers the gate width multivibrator, Q12, Q13.

2. Gate Width Multivibrator (Q12, Q13).

The configuration, mode of triggering, and operation of the gate width multivibrator are the same as those of horizontal multivibrator, Q8, Q9. After the multivibrator is triggered by the differentiated gate pulse from CR8 it runs for 30 microseconds and cannot be retrIGGERED during this period. The output on the collector of Q13 (see figure 201A) is a positive pulse approximately 9 volts in amplitude and 30 microseconds wide, whose positive timed edge coincides with the tape sync trailing edge. This pulse is applied to boxcar Q11.

Boxcar Circuit (Q11)

Q11 is normally kept conducting by negative base bias applied through resistor R45 and diode CR7. However, when the gate width pulse is applied, it is differentiated by R45 and C14, and the positive going spike, which is timed with the sync trailing edge, cuts off Q11. As soon as the spike reaches +1.5 volts, normally conducting diode CR7 opens and keeps the base of Q11 from going any further positive. This prevents base-to-emitter breakdown of Q11.

When Q11 is cut off its collector voltage (figure 201B) falls until it reaches the conduction level of normally cut-off transistor Q16. This level is determined by the current requirements of sample pulse

transformer T1. The width of the output pulse depends on C14 and the base bias resistors.

ATC Error Detector and Output Circuits

1. Transformer Driver (Q16).

Q16 is normally cut off and its collector (figure 203A) stays at -20 volts until the pulse from boxcar Q11 causes it to conduct. At this time the collector assumes the same potential as the emitter. The collector load of Q16 consists of the primary of transformer T1. Diode CR9, connected across the primary, prevents inductive ringing.

The output of Q16, which constitutes the ATC sampling pulse, is a 2 microsecond positive going pulse whose leading edge coincides with the trailing edge of tape sync (see figures 203A, A'). This pulse goes to the primary of T1, and also through P1-21 to the ATC Reference module, 226. In module 226 the pulse is used to generate a flat step on the ATC trapezoid. This step improves the accuracy of error detection.

2. Error Detector (Q17, Q18).

Transformer T1 splits the phase of the sample pulse applied to its primary. A positive going pulse from one end of the secondary is applied to the base of error detector Q18, and a negative pulse from the other end, to the base of error detector Q17. (See figure 203B.) The ATC trapezoid from module 226 is applied to the center tap of the secondary winding. (This pulse may be observed at the ATC TRAP test point, TP2, on the front panel of module 226.)

The emitter of NPN transistor Q17 is connected through diode CR5 and resistor R59 to one end of ERROR DETECTOR BALANCE potentiometer, R62. Similarly the emitter of PNP transistor Q18 is connected through diode CR6 and resistor R61 to the other end of the potentiometer. Potentiometer R62 is connected between the junctions of R59, R60 and R61, R63 while its arm is connected to the junction of R60, R63. This junction is also connected to the base of emitter follower Q19.

When the sample pulses first arrive, both Q17 and Q18 conduct. However, capacitor C23 across R59, and C24 across R61 rapidly charge up and produce bias voltages which allow the transistors to conduct only at the tips of the sampling pulses. Between sample pulses the capacitors cannot discharge because the only discharge path is through the 1-megohm emitter resistor of Q19.

The opposing sample pulses (see figure 203C) cancel each other at the arm of R62, and the output of

the circuit consists of a dc voltage equal to the level of the ATC trapezoid during the sampling interval. This voltage remains constant throughout each TV line until the arrival of the next sampling pulse, which starts at the trailing edge of tape sync. The voltage depends on the phasing between sample pulse and trapezoid. If the pulse moves up on the slope the voltage goes more positive and if the pulse moves down, the voltage goes more negative.

If no timing error exists the sample pulse occurs approximately at the center of the trapezoid slope and the corresponding dc output at the base of Q19

(figure 205A) is approximately +4 volts.

Two adjustments are provided in the error detector circuit, trimmer C22 (between the base of Q17 and ground) and ERROR DETECTOR BALANCE potentiometer R62. The trimmer permits balancing the input capacity of the error detector transistors. It is set to balance the rise time of the opposing sample pulses at the output of the error detector. R62 permits balancing the two outputs so that transients which occur during the sampling period cancel each other at the arm.

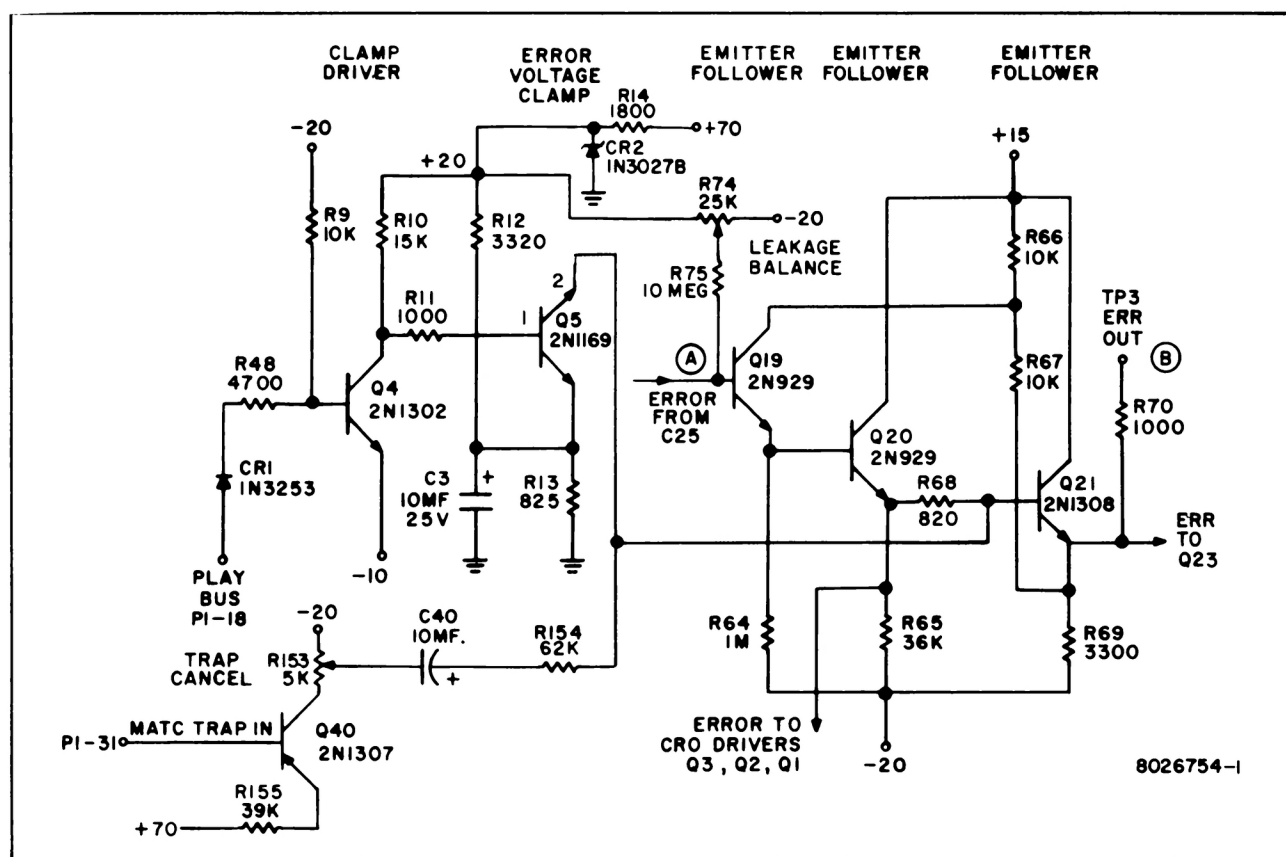
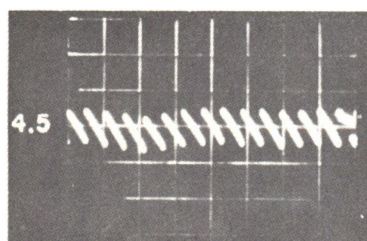
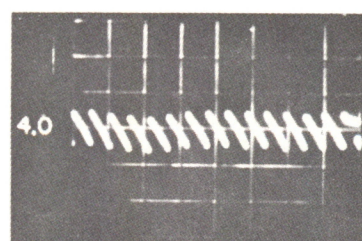


Figure 204—Output Emitter-Followers and Error Voltage Clamp



A. Q19 base, 1v/cm.



B. TP3, 1v/cm.

Figure 205—Typical Waveforms; Output Emitter-Followers and Error Voltage Clamp

Emitter-Followers (Q19, Q20, Q21)

The error detector output signal (see figure 204) passes through three emitter followers (Q19, Q20, and Q21, to the base of Q23 on board number 2, which is the input to the non-linear amplifier (NLA). The output of Q21 may be observed at the ERROR OUT test point, TP3, on the front panel (see figure 205B).

CRO Drivers (Q3, Q2, Q1)

The signal from the second emitter follower, Q20, is fed to transistor Q3. This stage has no gain and merely acts as an inverter. Q2 reinverts the signal and provides gain which can be adjusted by the CRO CAL potentiometer, R5. This potentiometer is set so that when the error is 1 microsecond, the amplitude of the error signal on the CRO is 100 I.R.E. units. Q1 is an emitter follower which drives the signal into the 75 ohm termination of the CRO.

Error Voltage Clamp Circuit (Q4, Q5)

The error voltage clamp circuit, which consists of driver Q4 and bidirectional switch, Q5, is controlled by the PLAY bus (see figure 204). This bus is at ground in PLAY, AUDIO REC, and CUE REC and at -26 volts in all other modes. The base of NPN transistor Q4 is returned to -20 volts through R9 and to the PLAY control bus at P1-18, through R48 and diode CR1.

When the PLAY bus is grounded CR1 conducts, and causes the base of Q4 to go slightly positive with respect to its emitter. The transistor then conducts and its collector voltage goes to -10 volts. This voltage cuts off NPN bidirectional switch Q5. Since the base of Q21 is then free to follow the ATC error detector signal applied to its base the ATC system functions normally.

When the PLAY bus is at -26 volts CR1 is cut off and the base of Q4 is negative with respect to its emitter. Thus, Q4 is cut off and its collector, which is returned to +20 volts through R10, is positive. Q5 then conducts and clamps the base of Q21 to +4 volts. This prevents noise and other interference from being applied to the ATC system when the machine is in STOP and holds the delay of the variable delay line on module 223 constant approximately in the center of its range.

MAINTENANCE, MODULE 225, BOARD 1

CRO Error Calibration Adjustment

1. Install a test tape containing a monoscope pattern. Place module 225 on an extender. Turn the ATC

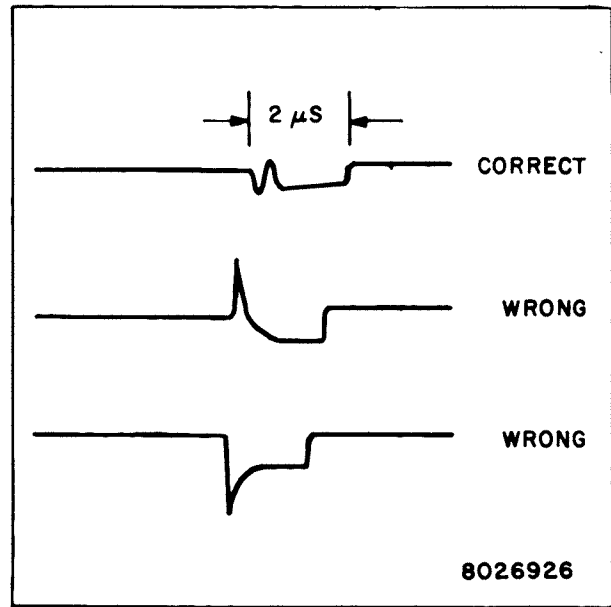


Figure 206—Waveforms for Adjustment of R62 (at TP3 of Module 223)

function selector switch, S1, on module 223 to the NORM position.

2. Place the machine in PLAY, with the guide servo on MANUAL.

3. Press the DEMOD OUT button of the picture monitor. Adjust the PB GUIDE POSITION control on the guide servo module counterclockwise until the portion of the vertical wedge at approximately 330 lines is displaced five black lines, including the first black line. This displacement corresponds to a timing error of approximately 1 microsecond.

4. Press the ATC ERROR button of the CRO and set the CRO sweep at a vertical rate. The error signal will appear as a number of slanting dotted lines. Adjust the CRO ERROR CALIBRATION potentiometer, R5, on module 225, until the amplitude of any one slanting line on the CRO graticule is 100 I.R.E. units.

Error Detector Adjustments (R62, C22, R74)

1. Install a test tape containing a monoscope signal. Place module 225 on an extender.

2. Trigger the oscilloscope with vertical drive, and set up the sweep for A delayed by B operation.

3. Place the recorder in PLAY, with the guide servo on MANUAL. Connect oscilloscope to the minus side of C23 and then to the plus side of C24 and adjust R62 so that the amplitudes of the sample pulses are equal.

4. Move probe to TP3 (ERROR OUT) press the ATC ERROR OUT button of the CRO and set the CRO sweep at a vertical rate. Adjust the PB Guide POSITION control on the guide servo module clockwise for an error of approximately 1 microsecond (amplitude of any one slanting line on CRO graticule equal to 100 I.R.E. units). Set time base of oscilloscope to $1 \mu\text{s}/\text{cm}$ and adjust trimming capacitor C22 for minimum amplitude of the transient appearing at the left side of the step as shown in figure 206.

5. Play tape with minimum error adjusted by vacuum guide and delay line adjustments.

6. Adjust, R74, Leakage Balance until the slope occurring during the vertical interval is minimized to a horizontal line. See figure 206A.

7. Replace module in the machine.

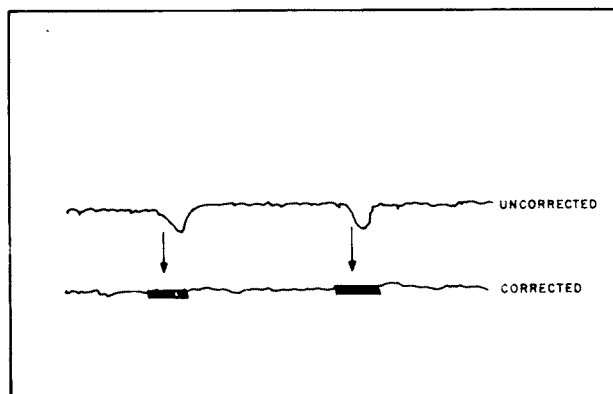


Figure 206A—Adjustment of R74, Leakage Balance

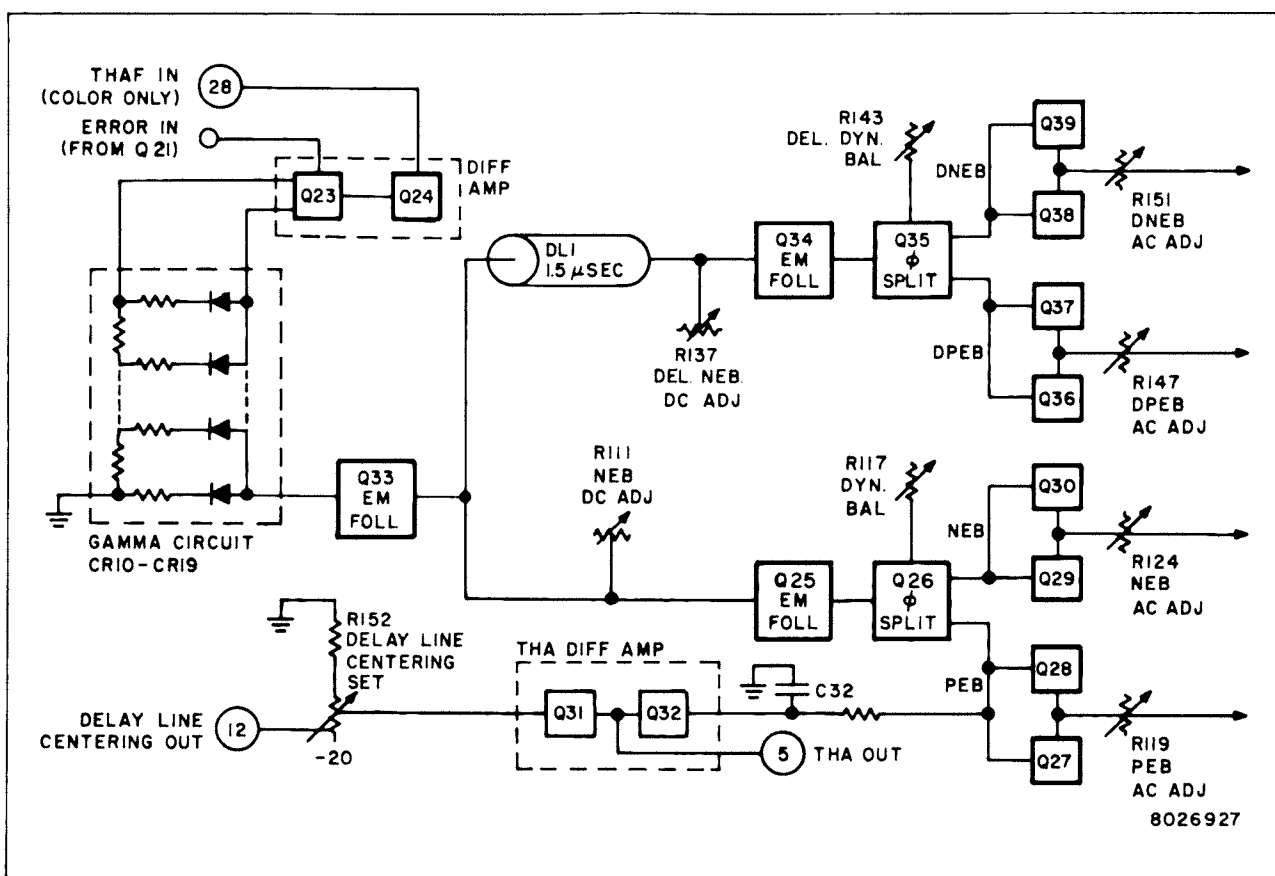


Figure 207—Block Diagram, NLA Circuits, and THA Differential Amplifier (Module 225, Board 2)

CIRCUITS ON MODULE 225, BOARD 2

Functional Description

(See Block Diagram, Figure 207)

Non-Linear Amplifier

The non-linear amplifier consists of the following circuits:

1. Input differential amplifier (Q23, Q24).
2. Emitter follower (Q33).
3. PEB-NEB circuits consisting of:
 - a. Emitter follower Q25.
 - b. Phase splitter Q26.
 - c. PEB complementary symmetry emitter fol-

- lower Q27, Q28.
- d. NEB complementary symmetry emitter follower Q29, Q30.
- 4. DPEB-DNEB circuits consisting of:
 - a. Fixed 1.5 microsecond delay line DL1.
 - b. Emitter follower Q34.
 - c. Phase splitter Q35.
 - d. DPEB complementary symmetry emitter follower Q36, Q37.
 - e. DNEB complementary symmetry emitter follower Q38, Q39.

The linear ATC signal from Q21 on board 1 of module 225 is fed to the input of Q23 in the input differential amplifier. A dc voltage is fed to the input of the other half of this amplifier, Q24. This voltage establishes the operating point of the amplifier. (The voltage is fixed in monochrome systems, but is varied by the THAF (Tape Horizontal Alignment Fine) voltage in color ATC systems.) A 10-section Gamma circuit consisting of resistors and diodes in the collector circuit of Q23 causes the collector load resistance to vary non-linearly with the input signal. This circuit is carefully designed so that the resulting non-linear gain of the amplifier equalizes the non-linear characteristic of the variable delay line on module 223. The delay line characteristic is linear at the low delay end of the range (high error voltage) and approaches a square law characteristic at the high delay end (low error voltage).

The non-linear output of Q23 is fed to an emitter follower, Q33, for isolation, and then to two groups of circuits, each of which develops a pair of push-pull output signals. The two groups are similar except that one is preceded by a fixed 1.5 microsecond delay line, DL1. As a result, one pair of signals is delayed by 1.5 microseconds with respect to the other pair.

To develop the undelayed signals, the output of Q33 is fed to an emitter follower, Q25, and then to a phase splitter, Q26. The outputs of Q26 consist of two signals, one positive going and the other negative going, whose dc axes are located symmetrically with respect to a level of approximately -10 volts. The positive going signal is amplified by a complementary symmetry emitter follower (CSEF) stage, Q27, Q28, and fed to the positive error bus (PEB) of the first half of the variable delay line on module 223. (This signal is also fed to the THA differential amplifier, Q31, Q32, which is described later.) The negative error signal is amplified by CSEF stage Q29, Q30, and fed to the negative error bus (NEB) of the first half of the variable delay line.

The CSEF stages provide low output impedance on both positive and negative going signals and have low idling current. In addition the circuits follow changes in signal polarity since one of the two transistors will amplify positive signals, and the other, negative signals.

The delayed error signals are developed by fixed delay line DL1, emitter follower Q34, phase splitter Q35, and CSEF stages Q36, Q37 and Q38, Q39. The positive going output signal is fed to the delayed positive error bus (DPEB) and the negative going signal to the delayed negative error bus (DNEB) of the second half of the variable delay line. Operation of these circuits is similar to that of the PEB and NEB circuits, except that changes in the DPEB and DNEB signals are applied to the second half of the variable delay line 1.5 microseconds after the same changes in the PEB and NEB signals are applied to the first half.

Each of the four CSEF circuits operate between zero and -20 volts. The PEB and DPEB signals can vary between zero and -9.9 volts and have a nominal operating point of -7.1 volts with respect to ground. Since the center of the variable delay line is returned to approximately -9.9 volts the PEB operating point is $+2.9$ volts with respect to the center. Similarly the NEB and DNEB signals can vary between -9.9 volts -20 volts and have an operating point of -12.9 volts, which is -2.9 volts with respect to the center.

Each of the four signals drives an individual set of reverse biased Varicap diodes on the variable delay line. The NEB, PEB busses have 42 varicaps each, while the DNEB, DPEB busses have 43. Under zero error conditions the voltages have an absolute value of 2.9 volts with respect to center and the variable delay line is in the center of its delay range. As the absolute value of the error voltage decreases the capacitance of the diodes and the delay of the line increase while the high frequency response of the line decreases. The reverse is true when the absolute value of the error voltage increases.

THA Differential Amplifier

The THA (tape horizontal alignment) differential amplifier, Q31, Q32 compares the DC level of the PEB signal with a fixed reference voltage obtained from a precision voltage divider and produces a current change linearly related to the difference. This error signal is fed back to a delay generator which adjusts the relative phasing between the ATC sampling pulse and ATC trapezoid so that the average position of the sample pulse is in the center of the trapezoid. When this condition is maintained, the dc

level of the PEB signal is in the center of the control range of the variable delay line (+2.9 volts with respect to the dc voltage applied to the center section of the delay line).

NOTE

For additional general information on THA refer to *Basic Principles of ATC, Overall Timing Relations* in the *System* section and *Overall Timing Relations* in the section on module 226.

Circuit Description

Non-Linear Amplifier

A simplified schematic diagram of the input stages at the non-linear amplifier is shown in figure 208. The first stage of this circuit is the input differential amplifier, Q23, Q24. One-half of this circuit, Q23, amplifies the error signal obtained from Q21 on board 1 non-linearly by use of a gamma correction circuit in its collector load. The other half of the circuit, Q24, sets the dc operating point and stabilizes the input impedance of Q23.

The operating point is determined by a dc voltage fed from the junction of voltage divider resistors R82 and R83 to the base of Q24. The emitter of Q24 is connected to the emitter of Q23 by a 300 ohm resistor, R86. Because of this connection, the emitter current of Q23 depends on the difference between the error signal on the base of Q23 and the dc voltage on the base of Q24.

NOTE

In a monochrome ATC system the voltage applied to the base of Q24, and the corresponding operating point, are fixed. However, in a color ATC system the voltage and operating point are shifted automatically by the THAF (Fine Tape Horizontal Alignment) current to keep the color ATC system in the center of its operating range. The THAF current enters module 225 on P1-28 and is fed to the junction of R81, R83, and R84.

The gamma circuit, which is connected in parallel with the collector load resistor, R135, of Q23 has ten sections, each consisting of a diode and two resistors. When no timing error exists, the voltage applied to the base of Q23 from the error detector circuits is approximately +4 volts. Under these conditions four diodes (CR10, CR11, CR12 and CR13) are forward biased, while the remaining six are reverse biased. As long as the timing error is zero the circuit presents a constant load impedance to the collector of Q23. When the voltage on the base of Q23, however, varies due to the error signals, the collector voltage also varies. This action forward biases or cuts off certain diodes, depending on the polarity of the error signal

at that instant. As a result the load impedance at the collector of Q23 changes in a non-linear manner with respect to the linear input error signals. The output characteristics of Q23 actually consist of a number of straight line segments of varying slopes which approximate a curve.

The output of Q23 (figure 209A) is fed to emitter follower Q33 for isolation. The emitter of Q33 is returned to -20 volts through two circuits in parallel. One of these circuits consists of fixed resistors R113, R112, and potentiometer R111 (NEB DC ADJ). The other circuit consists of resistor R136, 1.5 microsecond delay line DL1, resistor R138, and potentiometer R137 (D'LYD NEB DC ADJ). The junction of R113 and R112 is connected to the base of emitter follower Q25 and the junction of DL1 and R138 to the base of emitter follower Q34.

The emitter of Q25 is connected to the base of phase splitter Q26 (see figure 209B), which provides two output signals of opposite phase, one at its emitter and the other at its collector (see figure 209D). The dc level of the signal at the emitter can be adjusted by the NEB DC ADJ potentiometer, R111 in the input circuit of Q25. The dc level of the collector is more positive than that of the emitter by the drop across the transistor. DYNAMIC BALANCE potentiometer, R117, in the collector circuit of Q26 permits adjusting the two output signals to the same amplitude.

The emitter of Q34 is connected to the base of phase splitter Q35 (figure 209C). The two outputs of Q35 (figure 209D) are delayed behind the corresponding outputs of Q26 by the 1.5 microsecond delay line, DL1. D'LYD NEB DC ADJ potentiometer R137 adjusts the dc level of the signal on the emitter of Q35. D'LYD DYNAMIC BALANCE potentiometer, R143, permits adjusting the two signals for equal amplitudes.

Each of the four output signals goes through an individual CSEF stage to a corresponding bus on the variable delay line on module 223. The undelayed signals go to the NEB and PEB on the first half of the line, and the delayed signals to the DNEB and DPEB on the second half of the line.

Figure 210 shows the CSEF stage Q27, Q28, which supplies the output signal to the PEB. Q27 is an NPN and Q28, a PNP. The two bases are tied together and the two emitter resistors are ac coupled to each other by a capacitor, C30. One output signal is taken from the side of C30 connected to the emitter resistor of Q28 and fed out through P1-19 to the PEB on module 223. Another output is taken from the opposite side of C30 and fed to Q32 of the THA

differential amplifier (figure 211A). PEB AC ADJ potentiometer R119 in the emitter circuit of Q27 permits adjusting the rise times of the PEB to match those of the NEB.

On positive step transitions of the input signal, NPN transistor Q27 acts as an emitter follower and supplies the output signals. At the instant of transition PNP transistor Q27 is cut off. On negative going step transitions the PNP supplies the output signals and the NPN transistor is cut off.

The other three CSEF stages (Q29, Q30 for the NEB, Q36, Q37 for the DNEB, and Q38, Q39 for the DPEB) are similar to Q27 and Q28 except that no connection is made to the THA differential amplifier. Each of these circuits contains an individual potentiometer in the emitter circuit of the NPN stage. NEB AC ADJ, R124, is adjusted in conjunction with PEB AC ADJ, R119, to balance the rise times of the undelayed error busses. DPEB AC ADJ, R147, and DNEB AC ADJ, R151 perform a corresponding function for the delayed error busses.

CAUTION: All of the potentiometer adjustments in the non-linear amplifier are critical. Refer to the section entitled Setup Procedure for Non-Linear Amplifier before touching any of these adjustments.

THA Differential Amplifier

The THA differential amplifier consists of two NPN transistors, Q31 and Q32 (see figure 210). The two emitters are returned through equal resistors, R130 and R133, to -20 volts and are connected to each other through resistor R131. The collector voltage of Q32 is limited by a diode, CR20. The base of Q31 is returned to the junction of LINE CENT potentiometer R152 and resistor R128, which form part of a precision voltage divider between -20 volts and ground. The negative dc voltage (approximately -9.9 volts) which is fed to the center section of the variable delay line is taken from the other side of R128. R152 permits accurate centering of the delay line return voltage between the dc axes of the PEB and NEB signals. This control also sets the THA reference voltage on the base of Q31 to the correct value with respect to the center voltage.

A sample of the undelayed positive error signal is taken from one side of C30 in CSEF circuit Q27, Q28, and fed through a filter consisting of R134 and C32 to the base of Q32. The filtering removes all high frequency components from the PEB signal and leaves only the dc component.

If the PEB voltage on the base of Q32 is the same as the reference voltage on the base of Q31 no current flows through R131. If the base voltage of Q32 is different from the voltage on the base of Q31 a current flows in R131 which either reduces or increases the collector current of Q32.

The THA output signal is taken from the collector of Q32 and fed through P1-5 to contacts of relay K2 on the ATC Reference Module, 226. K2 feeds the THA signal to either of two delay control stages depending on whether the system is in the internal or external mode. In the internal mode (tonewheel or switchlock) contact K2A switches the signal to delay control stage Q18 in the ATC reference circuits on module 226. This stage has the effect of varying the timing of the AFC multivibrator which generates the ATC trapezoid. Thus, the phase relationship between tape sync and the AFC reference provides maximum ATC correction range.

In the external mode (Pixlock) K2A switches the THA signal to delay control stage Q15 on the Line-lock module, 316A in the Pixlock servo system. This circuit causes the headwheel motor to advance or retard the tape video signal at a slow rate corresponding to changes in the THA current. This action, in turn, changes the phase of the tape sync from which the ATC sample pulse is made. As a result, proper phase relationship between tape and AFC reference is provided and maximum ATC correction range is achieved.

In either mode, the THA loop reaches a state of equilibrium when the dc level of the signal applied to the PEB is $+2.9$ volts with respect of the delay line centering voltage. Under these conditions, the average position of the ATC sample pulse is in the center of the ATC trapezoid and the dc level of the ATC error detector output on board 1 of module 225 is approximately 4 volts with respect to ground.

If the horizontal phase of the tape video signal tends to drift, so that the average position of the ATC sample pulse is no longer the center point of the trapezoid, the dc level of the error detector output tends to go either more or less positive than $+4$ volts, depending on the direction of drift. This produces a change in the PEB dc level which causes a current to flow in R131. The resulting change in the collector current of Q32 unbalances the THA loop. The delay generator in the loop then changes the average phase relationship between the ATC sample pulse and trapezoid until equilibrium is restored.

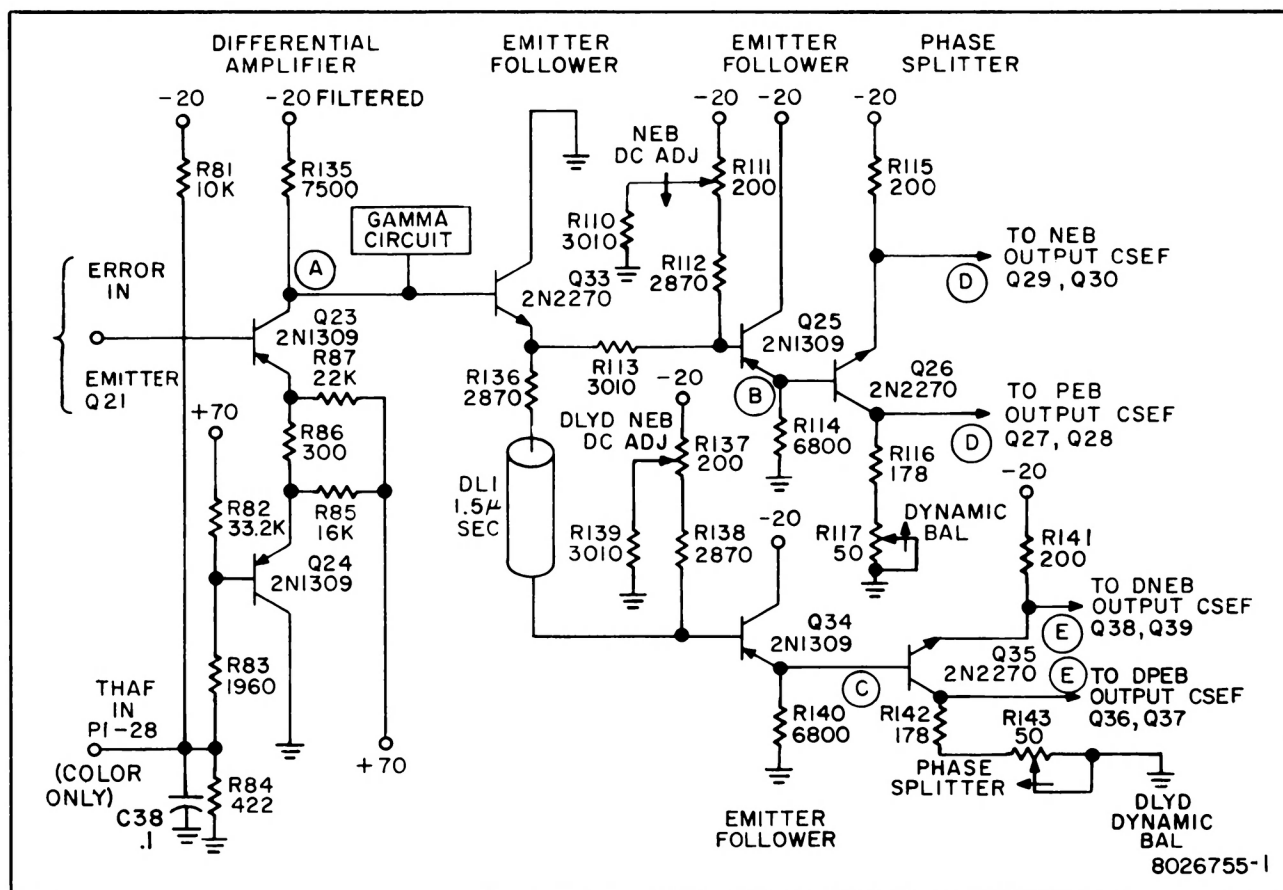
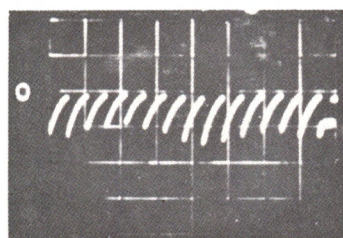
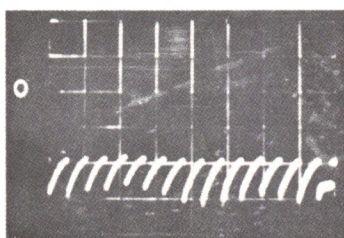


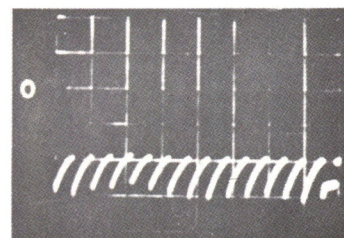
Figure 208—NLA Input Stages



A. Q23 collector, 10v/cm.



B. Q26 base, 5v/cm.



C. Q35 base, 5v/cm.

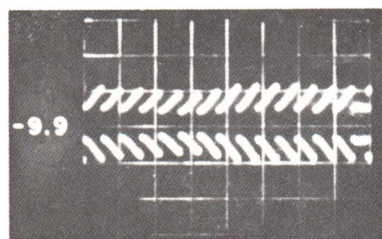
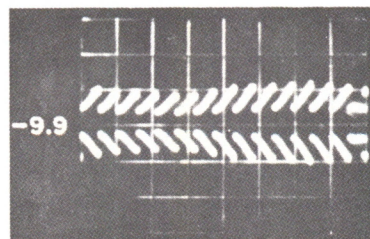
D. Top: Q26 emitter, 5v/cm,
Bottom: Q26 collector, 5v/cm.E. Top: Q35 emitter, 5v/cm,
Bottom: Q35 collector, 5v/cm.

Figure 209—Typical Waveforms; NLA Input Stages

NOTE

Since the THA circuit is a closed loop the dc voltage at the base or collector of Q32 will not appear to move when it is observed with a voltmeter.

In the external mode (Pixlock) the AFC circuit on module 226, board 1 by means of switchable delay circuit Q3 causes the center of the ATC trapezoid to occur in advance of the trailing edge of local sync. The effect of the THA circuit on the headwheel servo system then advances the phase of tape sync until its trailing edge, which coincides with the leading edge of the ATC sample pulse, occurs, on the average, in the center of the trapezoid.

ADJUSTMENTS, MODULE 225, BOARD 2

The non-linear amplifier has been carefully adjusted at the factory and should not be readjusted unless components have been replaced or the settings have been changed.

CAUTION: All adjustments on the non-linear amplifier are critical.

Equipment Required

The following equipment is required for adjusting the non-linear amplifier:

1. Oscilloscope having scales of direct sensitivity of 50 mv/cm and 1v/cm, such as the Tektronix 531 or 535.
2. Vacuum Tube Voltmeter (VTVM) having a sensitivity of at least 1 volt full scale, such as the Hewlett-Packard 410B.
2. Sine wave generator with floating output terminals and separate ground (required only for dynamic range test).
4. Source of bias voltage consisting of a 6-volt battery with a 5 K ohm potentiometer connected across it.
5. Bridging matched resistors consisting of two 19.6 K ohms, 1% 1/2 watt resistors connected in series with minigator clips at each end.
6. Clip leads.
7. 100 mmf, 25 v capacitor.

Adjustment Procedures

The following procedures should be performed in the indicated order.

1. Preliminary Centering Voltage Adjustment.
 - a. Insert module 225 in an extender with the NLA

facing up. Connect VTVM between ground and the junction of R128 and R129.

- b. Adjust R152 for a meter reading of -9.8 volts.
- c. Disconnect meter.

2. Dynamic Range Test (See note following step 2b).

- a. Remove module 225 from the extender. Lift and bend out of the way the center conductor connected to the base of Q23. Reinsert the module in the extender with the NLA side up.

- b. Measure base voltage of Q24 and set bias from battery to the same voltage (approximately 3.8 volts). Connect minus side of bias source to module ground and plus side (pot arm) to one terminal of the sine wave generator. Connect the other terminal of the generator to the base of Q23 and recheck battery bias. Make certain that generator is in "floating" connection with respect to ground.

NOTE

If a sine wave generator is not available steps 2b through 2f may be omitted.

- c. Set generator at any frequency between 1.2 kc and 20 kc. Turn the output control to zero.

- d. Connect oscilloscope ground to module ground. Set oscilloscope sensitivity at 2 volts per centimeter and adjust sweep to display 10 to 12 cycles of signal over 10 centimeters of the scale.

- e. Connect direct probe of oscilloscope to PEB (positive side of C30). Increase sine wave output of generator until signal on PEB is 7.5 ± 0.5 volts peak-to-peak, and is not distorted. The undistorted signal should appear as shown in figure 212. Flattened peaks will indicate limiting.

- f. Repeat step e for the NEB (C31+), DPEB (C35+), and DNEB (C36+), to insure that all busses are capable of the proper dynamic swing.

3. Static-Dynamic Balance Adjustments.

- a. Connect plus lead (pot arm) of bias source to the base of Q23 and minus lead to module ground. Measure voltage at base of Q24 and set bias battery voltage for the same reading.

- b. Connect a single lead from TP3 (VERT) on the Reference Generator module, 312, in series with a 100 mf, 25 volt isolation capacitor, to the base of Q23 (no ground should be used). Set oscilloscope sensitivity at 1v/cm. Connect bridging resistors from the NEB (C31+) to the PEB (C30+) and connect direct probe of oscilloscope to center point of bridging

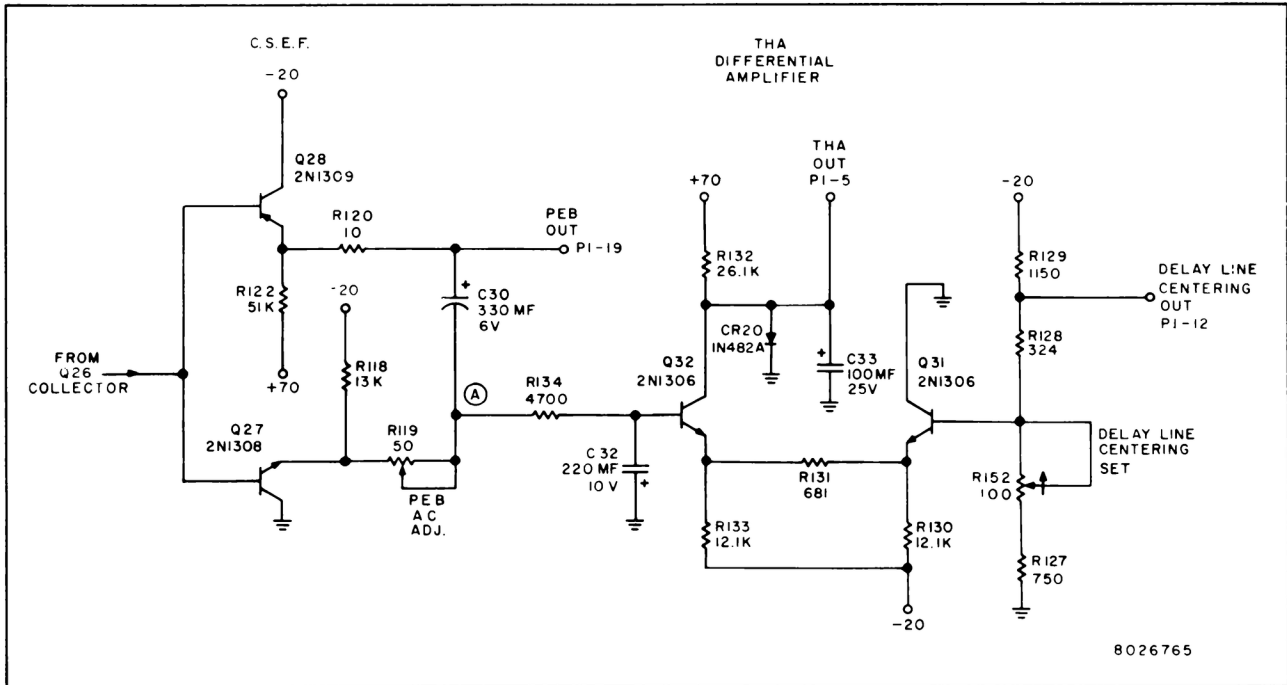
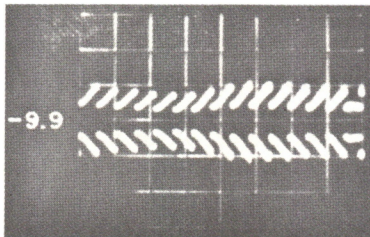
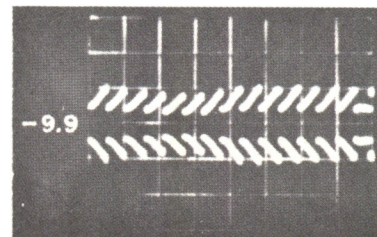


Figure 210—NLA Output CSEF and THA Differential Amplifier



**A. Top: Junction R119, C30 (PEB),
5v/cm.
Bottom: Junction R125, C31 (NEB),
5v/cm.**



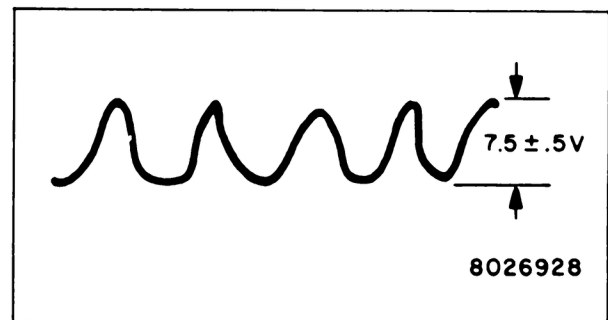
**B. Top: Junction R145, C35 (DPEB),
5v/cm.
Bottom: Junction R149, C36
(DNEB), 5v/cm.**

Figure 211—Typical Waveforms; NLA Output CSEF and THA Differential Amplifier

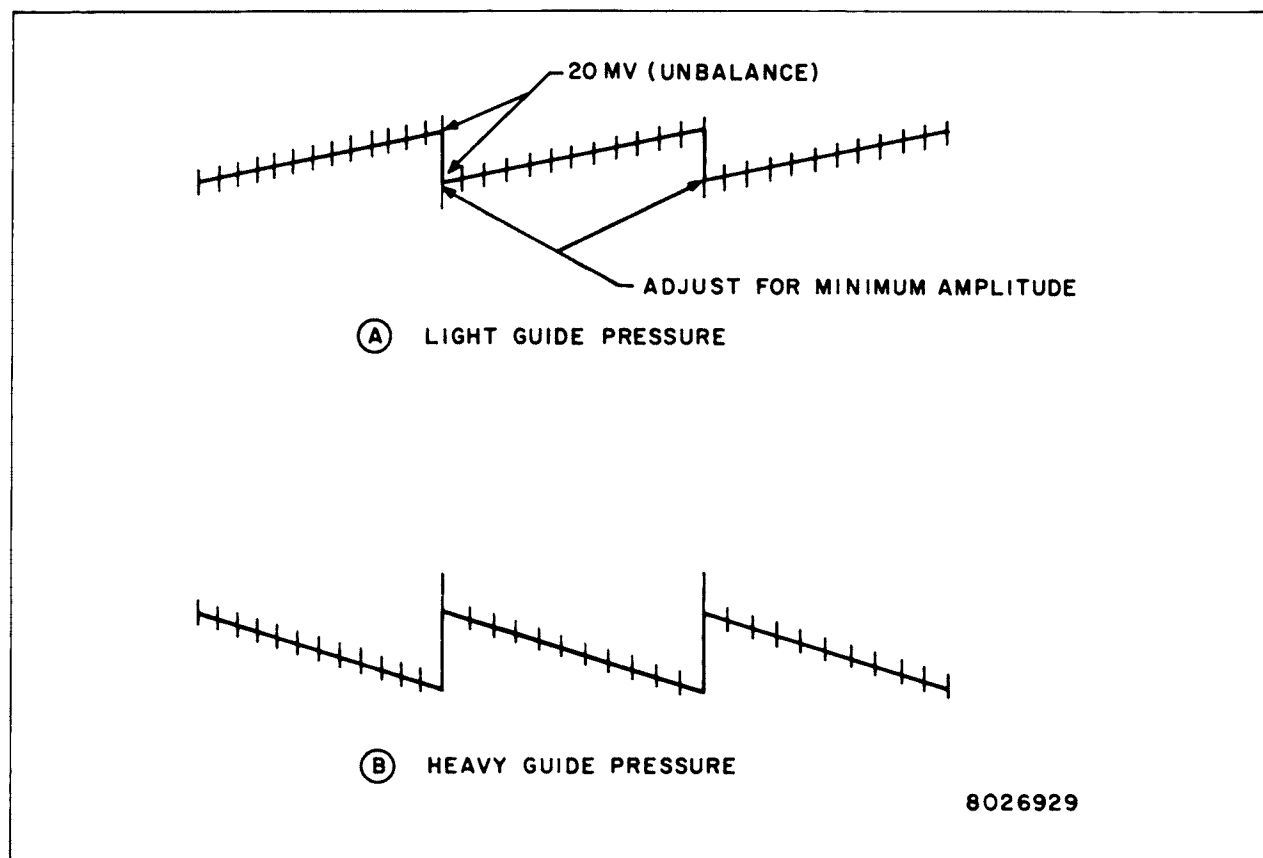
resistors. Ground the other lead of the probe. Set oscilloscope sensitivity at 50 mv/cm and sweep to 5 msec/cm. Adjust R117 for minimum signal on oscilloscope. After the adjustment the signal should be smaller than 20 mv peak-to-peak.

c. Move bridging resistors to the DNEB (C36+) and DPEB (C35+) and adjust R143 for minimum output as in step b.

d. Connect bridging resistors from the NEB (C31+) to the PEB (C30+). Connect ground lead of VTVM to the delay line centering junction of R128 and R129 or terminal 12 on P1. Set meter sensitivity



**Figure 212—Waveform for NLA
Dynamic Range Test**



**Figure 213—Waveforms for Adjustment of R119, R124, R147, R151
(Taken at Center Tap of Test Bridging Resistors)**

to maximum (lowest range) and calibrate meter for zero reading. Connect other meter lead to center point of bridging resistors and adjust the centering potentiometer R152 for zero reading on meter. (This adjustment is critical and its accuracy greatly depends on the sensitivity of the meter used).

e. Ground base of Q33 with clip leads. Adjust meter for 1 volt full scale and check the zero setting accurately. Leave ground lead of meter at junction of R128 and R129 or terminal 12 of P1 and connect other meter lead to the NEB (C31+). Adjust R111 for a reading of -0.5 volts. Switch meter polarity to positive and readjust zero setting. Move meter lead to PEB. The reading should be $+0.5 \pm 15$ mv.

f. Switch meter polarity to negative and recheck zero setting. Connect meter lead to DNEB (C36+) and adjust R137 to read -0.5 volts. Switch meter polarity to positive and recheck zero setting. Apply lead to DPEB (C35+) it should read $+0.5$ volts ± 40 mv (unbalance may be slightly higher than 40 mv at this stage).

g. Remove ground from base of Q33 and check

bias voltage at base of Q23. Reset bias, if necessary, to the same voltage as the base of Q24, and reconnect reference. Repeat steps 3b, c, and d.

h. Connect bridging resistors from the DNEB (C36+) to the DPEB (C35+). Connect meter between the delay line centering point (junction of R128 and R129, or terminal 12 of P1) and the center tap of the bridging resistors. The meter reading obtained is the offset of the DNEB and DPEB with respect to the NEB and PEB. If the offset reading is greater than plus or minus 10 mv adjust R152 to reduce the offset reading to this value. (The final offset reading must be of the same polarity as the initial total offset reading).

i. Remove the lead between the base of Q23 and TP3 of module 312, but leave the plus lead of the bias source connected to the base. Check to make certain that the bias voltage is the same as in step 3g. With meter still connected as in step 3h swing the bias through the range of $+3$ to $+4.8$ volts while observing meter reading continuously. Meter should not read more than ± 40 mv.

j. Move bridging resistors to the NEB (C31+) and PEB (C30+) and reconnect meter to center tap of bridging resistors. Swing bias from +3 to +4.8 volts as in the preceding step. Again, the meter should not read more than ± 40 mv. Remove meter connections from module.

k. Remove module from extender and restore all connections at the base of Q23.

l. Reinsert module 225 in the extender. Connect the bridging resistors between NEB (C31+) and PEB (C30+), and connect direct coax leads from oscilloscope to the center tap of the bridging resistors and ground. Trigger oscilloscope at a horizontal rate, set oscilloscope timing to 2 microseconds per centimeter and sensitivity to .02 volts per centimeter.

m. With monoscope tape on recorder, and guide servo in manual, place recorder in PLAY mode. Press ATC ERROR button of CRO and produce 1 μ s error by turning PB GUIDE control on module 221 to the left (light pressure).

n. The pattern on the oscilloscope should be similar to figure 46A. Adjust R119 (PEB AC ADJUST) and R124 (NEB AC ADJ) for minimum transients and noise. Measure and record the unbalance between NEB and PEB. (The amplitude of the unbalance is the offset between horizontal lines, ignoring the spikes.) The unbalance should not exceed 20 mv.

o. Adjust PB GUIDE POSITION control for a heavy pressure producing an error of 1 microsecond. The pattern on the oscilloscope should then be similar to figure 46B. Retouch R119 and R124 as in 3n.

p. Connect the bridging resistors across the DNEB and DPEB and adjust R147 (DPEB AC ADJ) and R151 (DNEB AC ADJ) for minimum transients and noise as in 3n and 3o. (R151 is the bottom potentiometer. Do not disturb the setting of R152.) Then observe the DNEB-DPEB unbalance on the oscilloscope. The unbalance should be no greater than 20 mv. If the unbalance is greater repeat the adjustments of R111 and R137 as in 3e and 3f.

q. When the conditions specified in 3e and 3f are met recheck the unbalances on the oscilloscope as in 3o and 3p and adjust R143 (DPEB BAL) until the DNEB-DPEB unbalance equals the NEB-PEB unbalance. *Do not adjust R117 to correct for the difference in the unbalances.*

4. Trap Cancellation Adjustment.

This is best accomplished in the Mod-to-Demod condition in the Stop mode since the jitter during playback obscures the effect.

a. Place module 225 on the bench and connect a short clip lead from the junction of CR1 and R8 to ground. (This unclamps Q5.)

b. Insert the module in the extender with R153 on the upper side being sure the clip lead doesn't short circuit to anything. (Miniature insulated clips may be required, or solder in, temporarily, a short piece of hookup wire.)

c. With the machine in Mod-Demod, the error signal can be observed at the NEB or PEB test point on module 223. (Use a high gain scope.) Adjust R153, trap cancellation, until the error is a straight line from one sample pulse to the next. Expand scope to observe the horizontal period. Remove the clip lead and reinsert the module in the machine after adjusting.

ATC REFERENCE (Module 226)

The ATC Reference Module is a single width module with two circuit boards mounted back to back. Board 1 contains the ATC reference circuits, and board 2, a clamped sync separator. The reference circuits produce a trapezoid waveform having the required frequency, phase, and slope to serve as the timing reference for the monochrome ATC system. This trapezoid is fed to the error detector circuits on board 1 of module 225, where its phase is compared with that of the ATC sample pulse, to produce a linear ATC error signal. The sync separator on board 2 extracts sync from the video output of the Monochrome ATC system, for use in the signal processing amplifier and the Color ATC system. This circuit is almost identical to the separator on module 303A, which provides sync to the input of the monochrome ATC system.

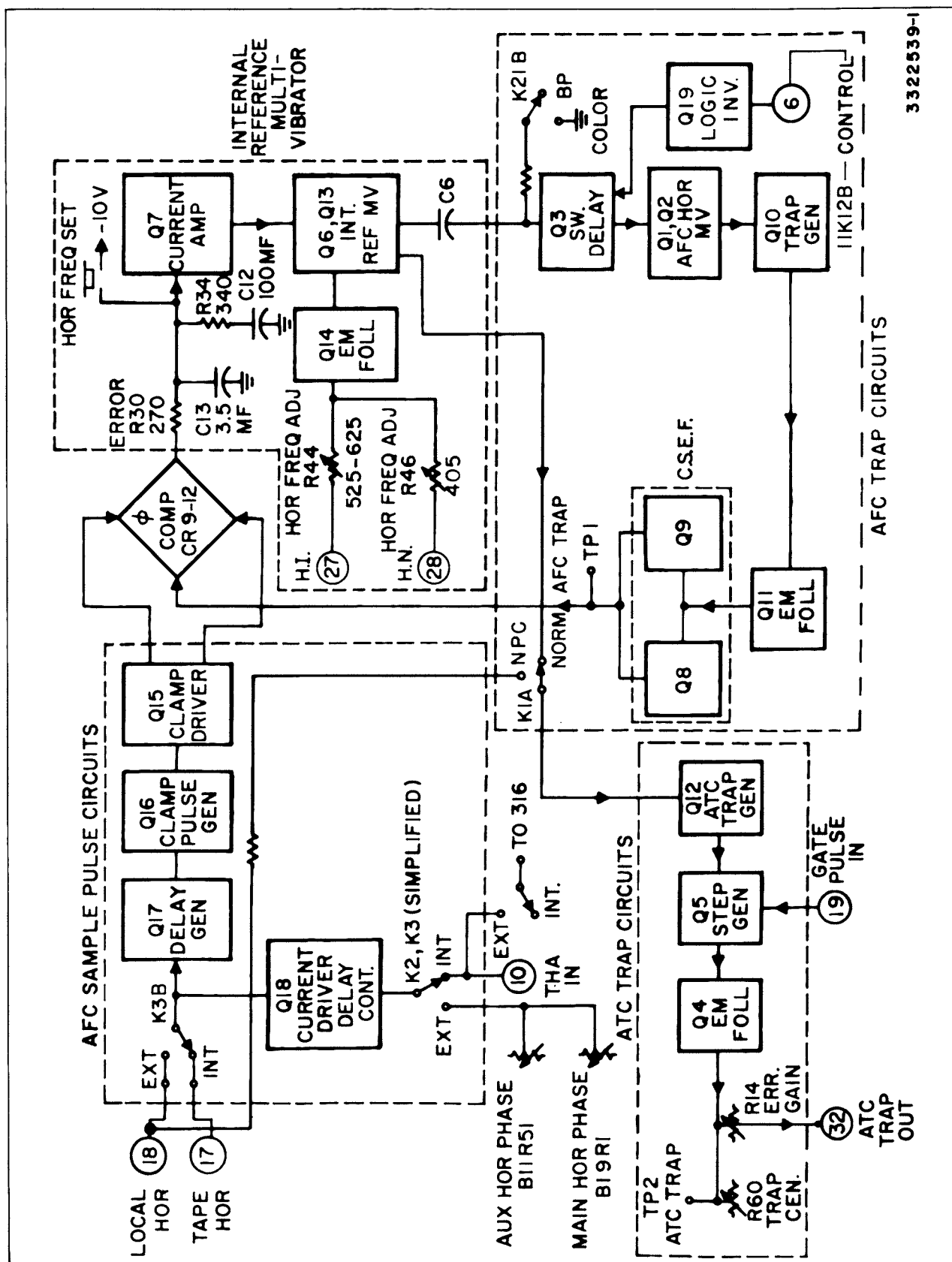
ATC REFERENCE CIRCUITS (Module 226, Board 1)

General

When reading the following description refer to the block diagram, figure 214 and the timing diagrams, figures 215 and 216.

The ATC Reference Circuits consist of the following:

1. Internal-external relays, K1, K2, K3.
2. AFC Sample Pulse circuits (Q18, Q17, Q16, Q15).
3. AFC loop consisting of:
 - a. Diode Quad Keyed Clamp Circuit CR9, CR10, CR11, CR12).



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Figure 214—Block Diagram, ATC Reference Circuits, Module 226, Board 1

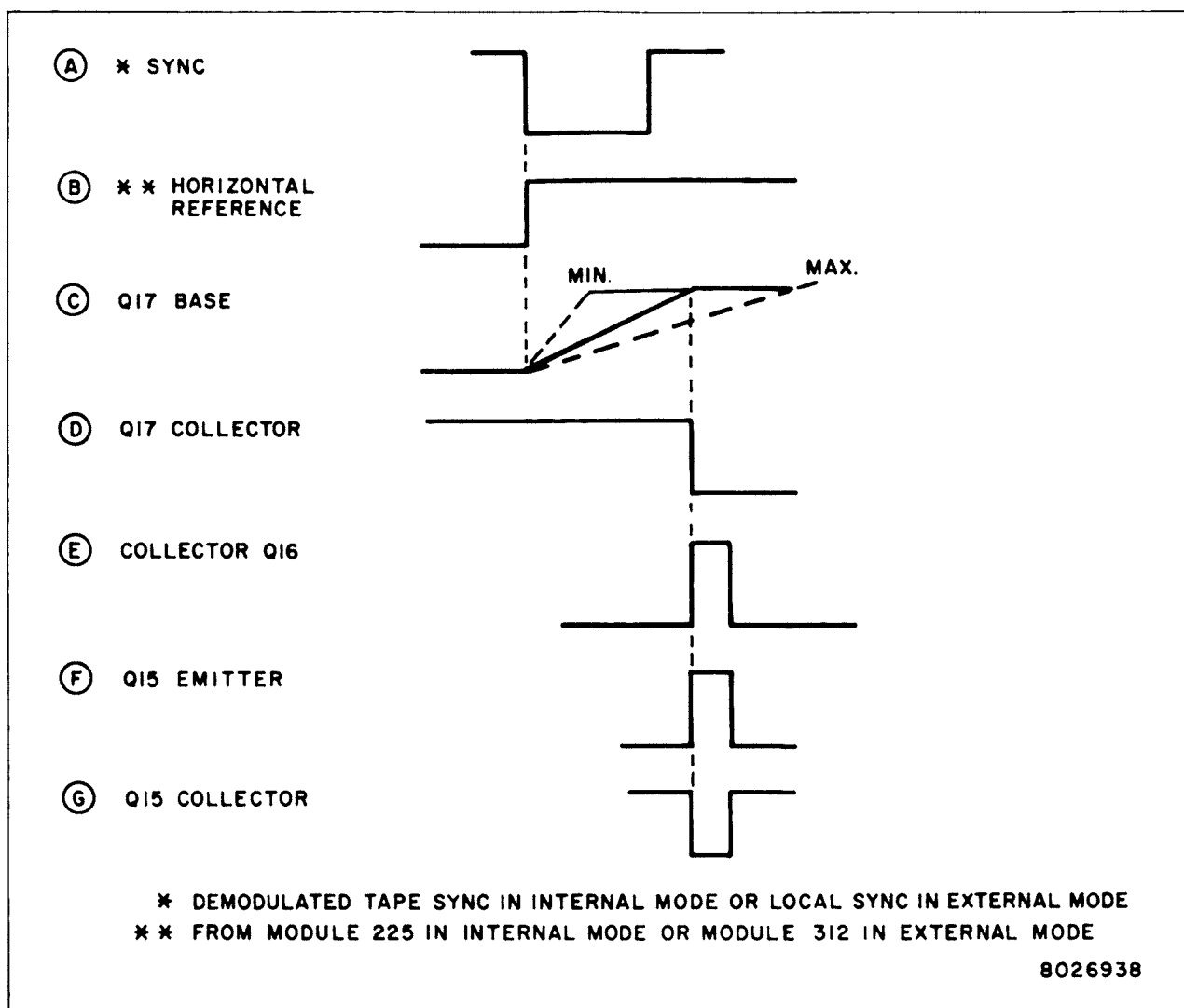


Figure 215—AFC Sample Pulse Timing

b. Internal Reference Multivibrator (Q6, Q13, Q7, Q14).

c. AFC Trapezoid Circuits (Q3, Q1, Q2, Q10, Q11, Q8, Q9).

4. ATC Trapezoid Circuits (Q12, Q5, Q4).

Internal-External Relays (K1, K2, K3)

Reference relays K1, K2, K3 determine the operating mode of the monochrome ATC system. When the recorder servo systems are in the Tonewheel or Switchlock modes, the relays K2 and K3 are de-energized and the ATC system is in the internal mode. If the ATC function selector switch, S1, on module 223 is in the NORM or COL OFF positions and the recorder is in the Pixlock mode, relays K2 and K3 become energized and switch the ATC system to the external mode. When the function selector switch is set on NPC relay K1 is energized and the AFC circuits are switched off.

NOTE

Refer to the functional descriptions in the *System* section for an explanation of the internal and external modes and a detailed description of the reference relay circuits.

AFC Sample Pulse Circuits

The AFC sample pulse circuits consist of a current source Q18, delay generator Q17, clamps pulse generator Q16, and clamp driver, Q15. These circuits produce two narrow sample pulses of equal height and opposite phase which key the diode quad clamp circuit, CR9 through CR12.

In the internal mode reference relay K3B feeds a tape horizontal reference pulse from the ATC Error Detector Module, 225, through P1-17, to delay generator Q17. The timed edge of this pulse (figure 215B) coincides with the leading edge of tape sync at the output of the Demodulator Output Module, 303A.

Q17 produces a delayed pulse which triggers clamp pulse generator Q16. The amount of delay provided by Q17 (figure 215C) is determined by a current generator, Q18. In the internal mode Q18 is controlled automatically by the THA error signal from module 225, board 2, which is switched into the circuit by K2.

In the external mode the circuit action is similar except that the relays are energized. K3B feeds a local horizontal pulse to Q17 instead of the tape horizontal pulse. K2A and K3A connect two horizontal phasing potentiometers to Q18, in place of the THA signal, and feed the THA signal to a delay generator on the Linelock module, 316. The local horizontal pulse originates on the Reference Generator Module, 312. The timed edge of this pulse (figure 215B) coincides with the leading edge of local horizontal sync. The two potentiometers (AUX HOR PHASE, R51, on module 223, and MAIN HOR PHASE, R1, on module 316) permit manual adjustment of the delay provided by Q17 (figure 215C). The THA signal automatically controls the phase of tape sync through the Pixlock system.

The clamp generator, Q16 produces a narrow sample pulse (figure 215E) whose leading edge coincides with the delayed edge of the pulse from Q17 (figure 215D). Clamp Driver Q15 splits the phase of this pulse. The two oppositely phased outputs of Q15 (figure 215F, G) key the diode quad clamp circuit, CR9 through CR12, in the AFC loop.

AFC Loop

The AFC loop consists of diode quad (CR9 through CR12), internal reference multivibrator (Q7, Q14, Q6, Q13) and AFC Trapezoid Circuit (Q3, Q1, Q2, Q10, Q11, Q8, Q9). The purpose of the loop is to reference the frequency and phase of the internal reference multivibrator to the AFC sample pulses.

The diode quad acts like a normally open switch controlled by the sample pulse. During the pulse the switch closes and applies the voltage on the slope of the AFC trapezoid, at that instant, to a long time constant RC circuit, which smooths out rapid timing variations. The resulting smoothed error voltage provides a measure of the average time between the start of the AFC trapezoid and the leading edge of the sample pulse. This voltage is fed to emitter follower Q7 in the circuit of the internal reference multivibrator.

The internal reference multivibrator Q6, Q13 is basically a free running circuit whose frequency can be varied by changing the dc voltage to which the bases of the two transistors are returned. The base

return voltage is obtained from a voltage divider whose end points are connected to two emitter followers, Q7 and Q14.

Q14 provides a dc voltage which can be adjusted manually with one of two potentiometers on the front panel (R44 for 525-625 line standards, or R46 for 405 line standards). The adjustment determines the free-running frequency of the multivibrator.

The output of Q7 depends on the average AFC error voltage from the RC circuit at the output of the diode quad. This voltage determines the deviation of the multivibrator from its free running frequency. A momentary pushbutton marked HOR FREQ SET, on the front panel, holds the base voltage of Q7 constant at -10 volts, when it is pressed. The button is used to inactivate the AFC loop during adjustment of the HOR FREQ potentiometers.

Two outputs are obtained from the internal reference multivibrator. One of these is fed to switched delay stage Q3, in the AFC trapezoid circuits, and the other to ATC trapezoid generator Q12.

The switched delay stage, Q3, produces a pulse whose trailing edge can be delayed with respect to the timed edge of the output of the internal reference multivibrator by one of three fixed amounts depending on the operating mode: zero in the internal mode, approximately 6.5 microseconds in the external mode of monochrome ATC, and approximately 11.5 microseconds in the color ATC mode (see figure 216B). The switching is performed by relay Q19 on module 226, and relay 11K21, on the ATC relay bank.

The differentiated pulse from Q3 (figure 216B) triggers the AFC horizontal multivibrator, Q1, Q2. The timed edge of the multivibrator output (figure 216C), which coincides with the trigger pulse, starts the slope of the AFC trapezoid (figure 216D) by keying trapezoid generator Q10. Time constants in the circuit of Q10 determine the slope of the trapezoid.

From Q10 the trapezoid is fed through an emitter follower, Q11, and a CSEF stage, Q8, Q9 to the diode quad. These stages provide low output impedance and sufficient current gain to drive the quad.

ATC Trapezoid Circuits

The timed edge of the output from the internal reference multivibrator (figure 216A), starts the slope of the ATC trapezoid (figure 216F) by keying trapezoid generator Q12. A flat step, which coincides with the ATC sample pulse (figure 216G) is imposed on this trapezoid by stage Q5. The step increases the

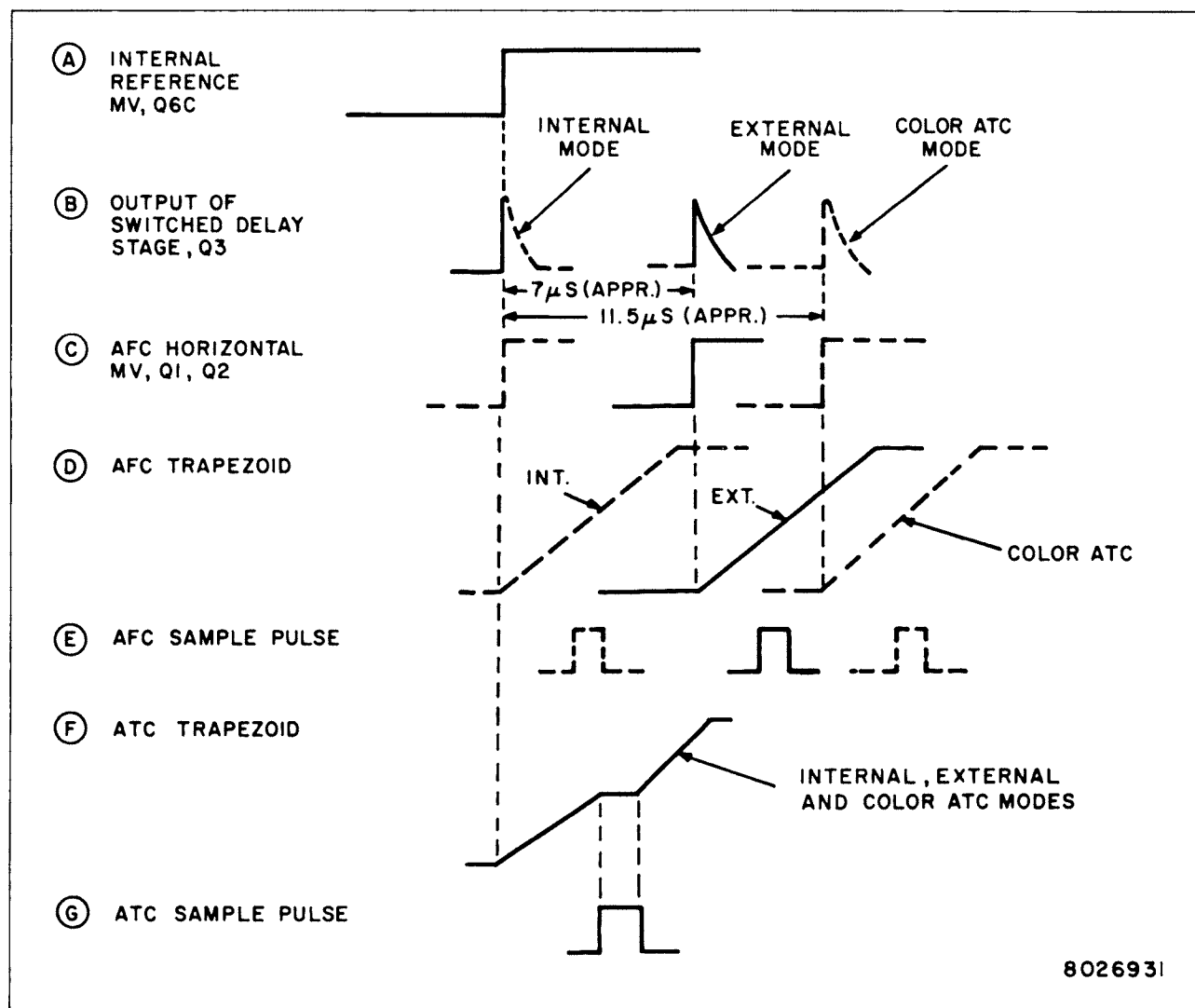


Figure 216—Timing of Trapezoids with Respect to Internal Reference Multivibrator

accuracy of measurement of the ATC error signal on module 225 by holding the trapezoid voltage constant during the sampling interval. Q5 is gated by the ATC sample pulse itself, which is fed from module 225 to P1-19 on module 226.

The timing of the ATC trapezoid (figure 216G) with respect to the AFC trapezoid (figure 216D) is determined by the amount of switched delay provided by Q3. In the internal mode the switched delay is zero and the two trapezoids start at the same time. However, in the external or color ATC modes the ATC trapezoid starts in advance of the AFC trapezoid by the corresponding switched delay (6.5 or 11.5 microseconds).

The ATC trapezoid, with the superimposed step, is fed to an emitter follower, Q4, and then through P1-32, to the ATC Error Detector Module, 225. Two potentiometers are provided at the output of the emit-

ter follower, the ERROR GAIN control, R14, and the TRAP CENT potentiometer, R60. R14 is a front panel operating control which varies the amplitude of the trapezoid. R60 is an internal screwdriver adjustment which permits adjusting the dc operating point of ERROR GAIN potentiometer R14.

OVERALL TIMING OF ATC REFERENCE CIRCUITS

The functions of the ATC reference circuits can be easily understood by examining the timing relations shown in figures 217 and 218.

Internal Mode

Overall timing relations in the internal mode are shown in figure 217. In this mode the primary timing reference is tape sync at the output of module 303A (figure 217A). The timed edge of the horizontal reference pulse (B) fed to delay generator Q17 coin-

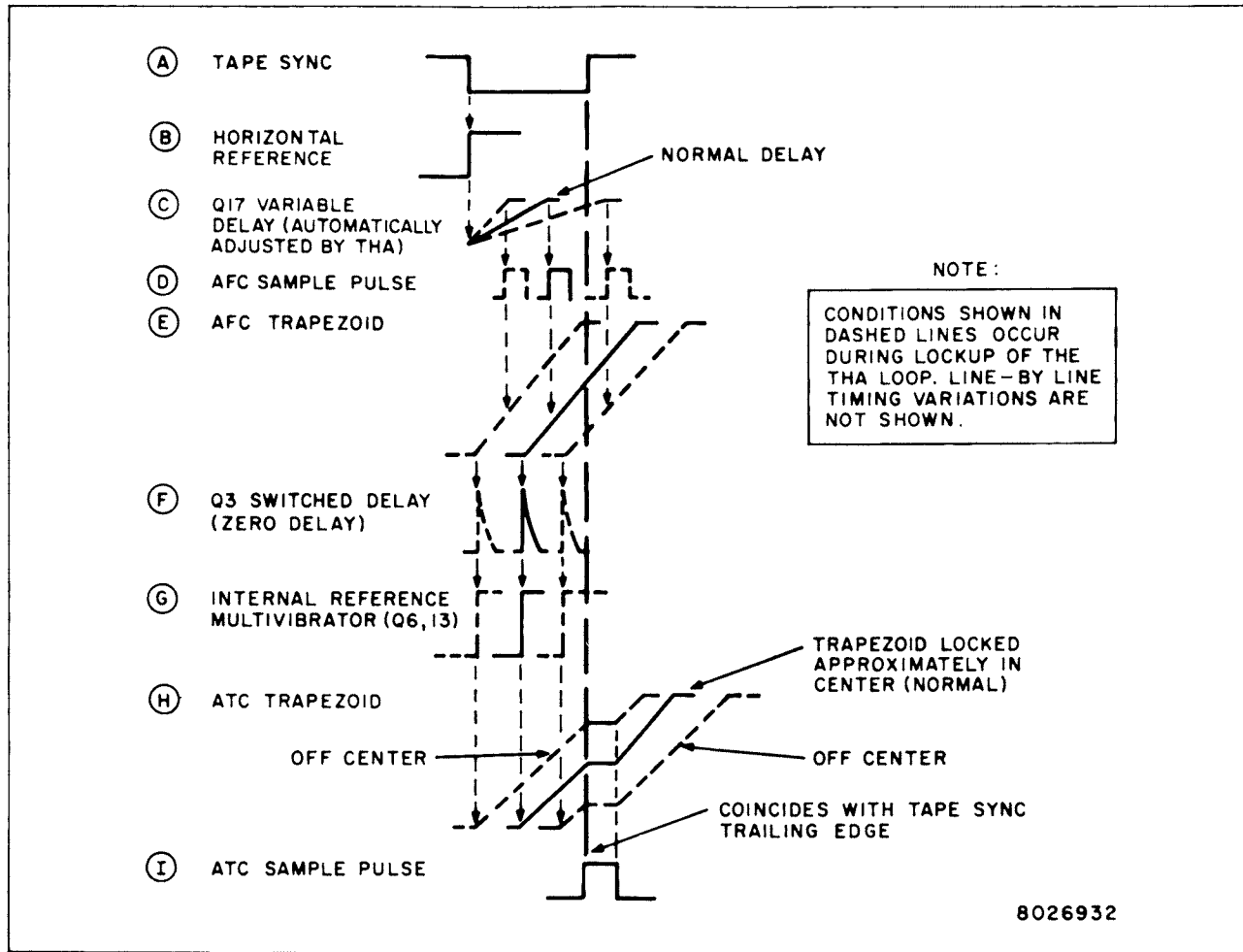


Figure 217—Phasing of Trapezoids with Respect to Tape Sync in Internal Mode (Machine in Play)

cides with the leading edge of tape sync. Q17 delays the AFC sample pulse (D) by an amount depending on current from the THA circuit. The AFC loop adjusts the phase of the internal reference multivibrator (G) so that the AFC trapezoid (E) is approximately centered with respect to the AFC sample pulse. The start of the ATC trapezoid (H) coincides with the timed edge of the internal reference multivibrator output (G) and, since the switched delay (time between F and G) is zero, the two trapezoids start at the same time.

The step on the ATC trapezoid coincides with the ATC sample pulse (I) and the leading edge of the sample pulse coincides with the trailing edge of tape sync. As the THA current varies the delay of Q17, waveforms D through H shift with respect to tape sync. When the THA circuit is in equilibrium the ATC trapezoid (H) will be approximately centered with respect to the ATC sample pulse (I) and consequently, the step will be approximately in the center of the trapezoid. (See waveforms in solid lines in fig-

ure 217.) When the THA circuit is not in equilibrium the step will be either too high on the slope (dotted waveforms on the left) or too low on the slope (dotted waveforms on the right).

External Mode

Timing relations for the external mode are shown in figure 218. In the external mode the primary timing reference is local sync (figure 218A). The timed edge of the horizontal reference (B) coincides with the leading edge of local sync. Q17 delays the AFC sample pulse (D) with respect to the horizontal reference by an amount (C) depending on manual adjustment of the main horizontal phasing control (R1 on module 316) and the auxiliary horizontal phasing control (R51 on module 223). The AFC loop adjusts the phase of the internal reference multivibrator (G) so that the AFC trapezoid (E) is approximately centered with respect to the AFC sample pulse, as in the internal mode. However, the timed edge of the multivibrator output occurs in advance of the start of the ATC trapezoid by the switched delay (approximately

7 microseconds in the external mode or 11.5 microseconds in the color ATC mode). Consequently the AFC trapezoid (H) starts in advance of the AFC trapezoid (E) by the amount of switched delay.

From the preceding, it can be seen that the phase of the ATC trapezoid with respect to local sync (A) depends on the variable delay of Q17, which, in turn depends on the adjustment of the horizontal phasing controls. For a given setting of these controls the THA circuit causes the headwheel servo system to adjust the phase of tape sync so that the ATC sample pulse (I) is approximately centered with respect to the ATC trapezoid. Thus, as the controls are varied, the phase of tape sync also varies. Because the ATC trapezoid is advanced by the switched delay, the phase of tape sync must occur in advance of local sync to maintain centering of the sample pulse. When the phasing controls are adjusted for minimum delay of Q17 (dotted waveforms to the left in figure 218) the advance of tape sync is maximum. Similarly when the delay of Q17 is maximum (dotted waveforms on the right) the advance is minimum. The controls are normally adjusted so that the advance of tape sync is equal to the total fixed video delay between the demodulator output and the processing amplifier output so that the output sync is aligned with local sync.

CIRCUIT DESCRIPTIONS, MODULE 226, BOARD 1

During the following circuit descriptions refer to the simplified schematics, figures 219, 221, and 223, and the accompanying waveforms.

AFC Sample Pulse Circuits

(See figure 219)

1. Current Source (Q18) and Delay Generator (Q17).

During the negative portion of the input signal (figure 220A) Q17 is cut off and C25, in its base circuit charges to -10 volts. At the positive going edge of the horizontal reference pulse, which corresponds to the *leading* edge of sync, CR13 opens and C25 starts discharging. The discharge rate depends on currents from $+70$ volts (through R59) and from stage Q18.

The discharging continues until the base of Q17 goes slightly above the emitter voltage, which is fixed at -3.3 volts by voltage divider R55 and R57. At this point Q17 conducts, the discharging stops, and the collector goes to the emitter voltage, or -3.3 volts. When Q17 is cut off, its collector voltage (figure 220B) determined by voltage divider R56, R58, is $+5$ volts. Therefore the edge of the pulse, at the end of the discharge period is negative going. This edge is delayed behind the positive going edge of the hori-

zontal reference input pulse, or the leading edge of sync, by the length of the discharge period. (See figure 216.)

2. Clamp Pulse Generator (Q16).

The collector output of Q17 is differentiated by C23 and R54, and the negative going differentiated spike cuts off normally conducting NPN transistor Q16. The resulting output on the collector of Q16 (figure 220C) is a narrow positive going pulse whose width is determined by the duration of the spike. This pulse is applied to the base of clamp driver Q15.

3. Clamp Driver Q15.

NPN transistor Q15 is a phase splitter which converts the output of Q16 to two pulses of equal amplitude and opposite phase. These pulses key the diode quad clamp, CR9 through CR12.

Since the phase splitter has equal collector and emitter loads, the emitter voltage is equal to half the supply voltage, or -10 volts, when the transistor conducts. Therefore the transistor is cut off when its base goes more negative than -10 volts. The base of Q15 goes directly to the collector of Q16, which is normally at -20 volts. Therefore Q15 is normally cut off. However, during the clamp pulse, the collector of Q16 rises to -10 volts. Q15 then conducts and produces a positive 10 volt pulse on its emitter and a negative 10 volt pulse on its collector (figure 220D). The leading edges of these pulses are delayed behind the timed edge of either the tape or local horizontal reference (according to the operating mode) by the discharge period of C25 on the base of delay generator Q17.

AFC Loop

1. Diode Quad Clamp Circuit (CR9 through CR12).

The pair of sample pulses from Q15 is applied through 10 mf capacitors (C21 and C22) to two opposite junctions of the diode quad. (See figure 219.) The AFC trapezoid from CSEF stage Q8, Q9 is applied to the third junction. The fourth junction is connected through R30 to the base of current amplifier Q7 in the circuit of the internal reference multivibrator (see figure 221).

The pulses key all four diodes on and allow the voltage on the trapezoid slope at that moment to go through R30, to the base of Q7. C21 and C22 develop bias voltages which allow diode conduction only at the pulse tips. The two sample pulses cancel each other at the output junction and do not appear in the signal.

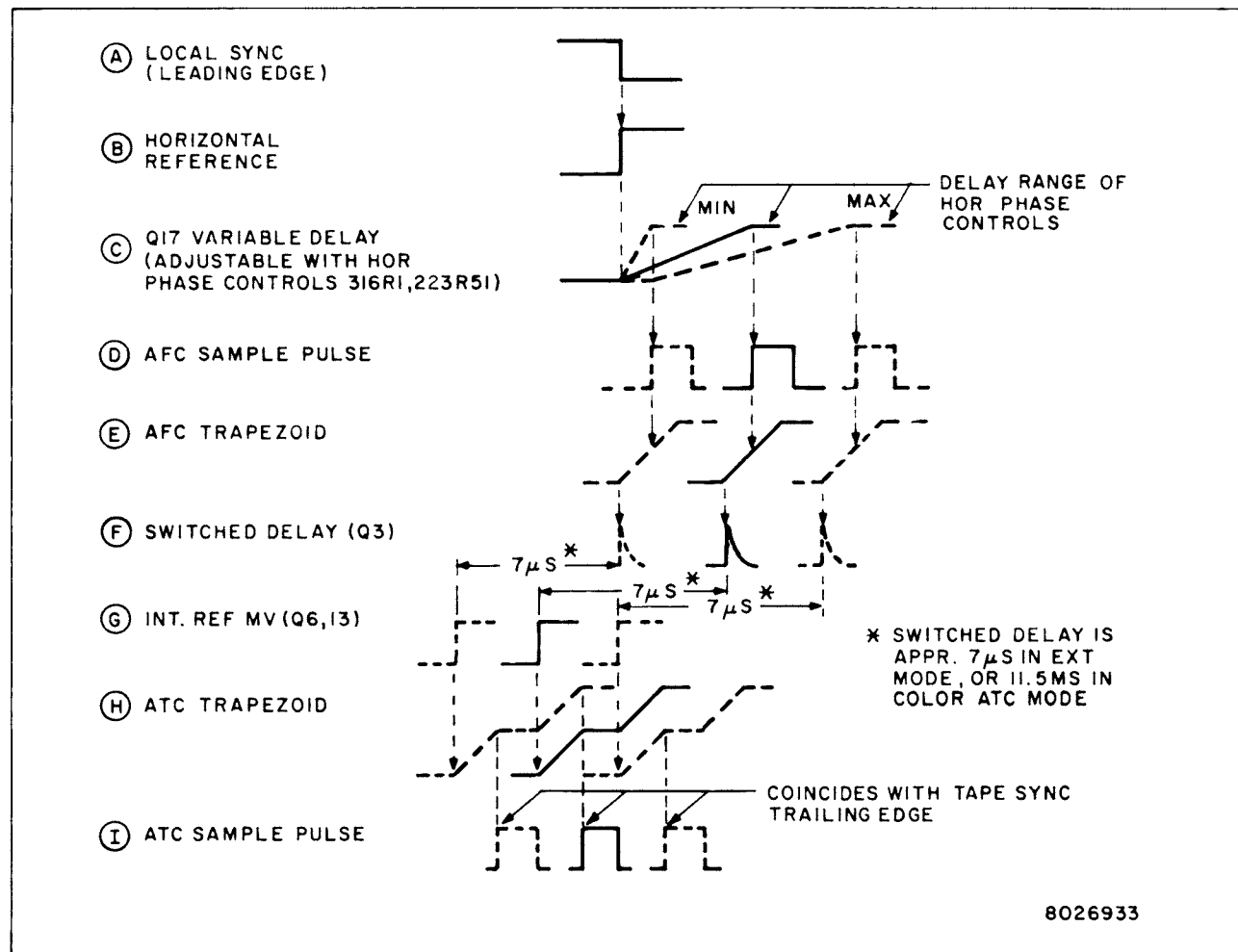


Figure 218—Phasing of Trapezoids with Respect to Local Sync for Three Settings of Horizontal Phase Controls (EXT or COLOR ATC Modes)

During the sampling intervals a charge builds up on 3.3 mf capacitor C13 and 100 mf capacitor C12 which, in conjunction with R30 and R29, form a long time-constant network in the base circuit of Q7. (See figure 221.)

If the incoming horizontal reference signal changes frequency or phase slightly the timing of the AFC sample pulses with respect to the trapezoid applied to the diode quad changes by a corresponding amount. Consequently there is a change in the instantaneous voltage to which the capacitors in the RC network charge. The RC network produces an average voltage taken over a period which is long, compared with the horizontal period. This voltage corrects the frequency and phase of the internal reference multivibrator by changing the operating point of emitter follower Q7.

2. Internal Reference Multivibrator (Q6, Q13, Q7, Q14).

The operation of the internal reference multivibrator is similar to that of the frequency controlled oscillator on the Tape Sync Processor Module, 317. For details on this circuit refer to the instruction book on the TR-22 Servo Systems.

The emitter current of Q13 (figure 222B) constitutes the output of the AFC loop. When this current flows, it enters ATC trapezoid generator Q12 and charges C18 in its collector circuit. When the current stops, Q12 cuts off, and C18 discharges at a slower rate through Q5, to produce the trapezoid slope. Thus the ATC trapezoid (figure 222C) starts when Q13 is cut off. This action is discussed in more detail under *ATC Trapezoid Circuits*.

An additional output, taken from the collector of Q6 (figure 222A), provides the feedback required to complete the AFC loop. This feedback signal goes through C6 to the switched delay stage, Q3, in the AFC trapezoid circuits.

AFC Trapezoid Circuits (Q3, Q1, Q2, Q11, Q8, Q9)

1. Switched Delay Stage (Q3).

Q3 is a bidirectional PNP transistor. (See figure 223.) In the internal mode, relay K3 on module 226, returns one of the two emitter-collector elements to ground. Thus, since the base is returned to -20 volts and the other emitter-collector element, to -10 volts, the transistor acts as an emitter follower. The output of Q6 in the internal reference multivibrator is differentiated by C6, R10, and R11 in the base circuit of Q3. By emitter-follower action the pulse goes straight through without delay. The positive pulse (figure 224A) then passes through C2 and diode CR1 to the junction of R6 and C1 in the AFC horizontal multivibrator.

In the external mode, a positive bias is applied to the base of Q19 from the junction of R153 and R154, which cuts off Q19, which removes the ground connection from the junction of R8, and R9, and allows the two series resistors to return to -20 volts. The circuit then acts as an amplifier. The differentiated pulse on the base turns Q3 off on the positive spike and the output is a negative going pulse between -10 and -20 volts. The differentiating network connected to the base of Q3 causes the width of this pulse to be approximately 6.5 microseconds. After differentiation by C2 and R7, the positive going spike, which provides a delay of approximately 6.5 microseconds triggers Q1 through CR1.

In a color ATC system the circuit acts the same as in the monochrome external mode except that relay K21B returns the junction of R10 and R11 in the base circuit of Q3 to ground instead of -20 volts. This reduces the current available for differentiation and broadens the positive spike. The resulting output pulse is approximately 11.5 microseconds wide, and the triggering pulse for the multivibrator is delayed by approximately 11.5 microseconds.

2. AFC Horizontal Multivibrator (Q1, Q2).

The AFC horizontal multivibrator is a monostable circuit similar to the horizontal multivibrator Q8, Q9 on modules 225, board 1. (See description under *ATC Error Detector Module 225*). Transistor Q1 is normally conducting. When the positive spike from switched delay stage Q3 appears, it cuts off Q1 and starts the one shot period. The resulting waveform on the collector of Q2 (figure 224B) is a pulse between -10 volts and ground whose positive going edge is timed with the trigger pulse. This pulse is applied to the base of AFC trapezoid generator Q10.

3. AFC Trapezoid Generator (Q10).

The AFC trapezoid is produced by the fast charging and relatively slower discharging of capacitor C16 in the emitter circuit of trapezoid generator Q10. During the stable period of horizontal multivibrator Q1, Q2, transistor Q2 is cut off and its collector, which is connected to the base of Q10 is returned to -10 volts. Therefore C16 charges rapidly to -10 volts through the 330-ohm collector resistor of Q2. When the trigger pulse from the switched delay stage occurs, Q2 conducts, and the unstable period of the multivibrator starts. As soon as Q2 conducts its base goes to ground and Q10 becomes cut off. C16 then starts to discharge from -10 volts towards $+70$ volts through 24K ohm resistor R38. The discharge continues until the emitter of Q10 goes slightly above ground. Q10 then conducts and clamps C16 to ground potential. The output at the emitter of Q10 (figure 224C) is thus a trapezoid with a positive slope which starts at -10 volts and ends at ground. The start of the slope coincides with the trigger pulse from the switched delay stage, Q3, and the end of the slope occurs 5 microseconds later.

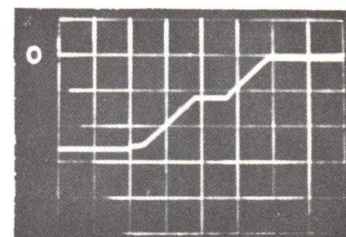
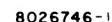
4. Emitter Follower (Q11) and CSEF (Q8, Q9).

The output of the trapezoid generator is fed to emitter follower Q11 for isolation and is then ac coupled to complementary symmetry emitter follower Q8, Q9. The CSEF circuit provides a low output impedance and sufficient current gain to drive the diode quad clamp circuit. The AFC trapezoid at the output of the CSEF may be observed at test point TP1 on the front panel of module 226 (figure 224D). This trapezoid starts at -13 volts and ends 5 microseconds later at -5 volts.

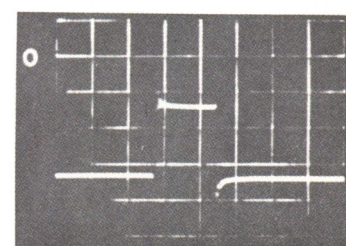
ATC Trapezoid Circuits (Q12, Q5, Q4)

The ATC trapezoid circuits (see figure 221) consist of trapezoid generator, Q12, step generator Q5, and emitter follower Q4. These circuits produce the ATC trapezoid from the output of the internal reference multivibrator and feed it to the ATC error detector on module 225.

The ATC trapezoid is produced by Q12 and Q5. Q12 provides a fast charge path for capacitor C18 in its base circuit when Q13 of the multivibrator is conducting, and Q5 provides a slow discharge path when Q13 is cut off. Q5, which is normally conducting, becomes cut off when the gate pulse, which coincides with the ATC sample pulse arrives from module 225 (figure 222F). During this pulse (2 microseconds) the discharge path of C18 is open and consequently



**C. Q12 collector, 2 μ s/cm)
5v/cm.**



F. Pin 19, 1 μ s/cm, 5v/cm.

Figure 222—Typical Waveforms; Internal Reference Multivibrator and ATC Trapezoid Circuits

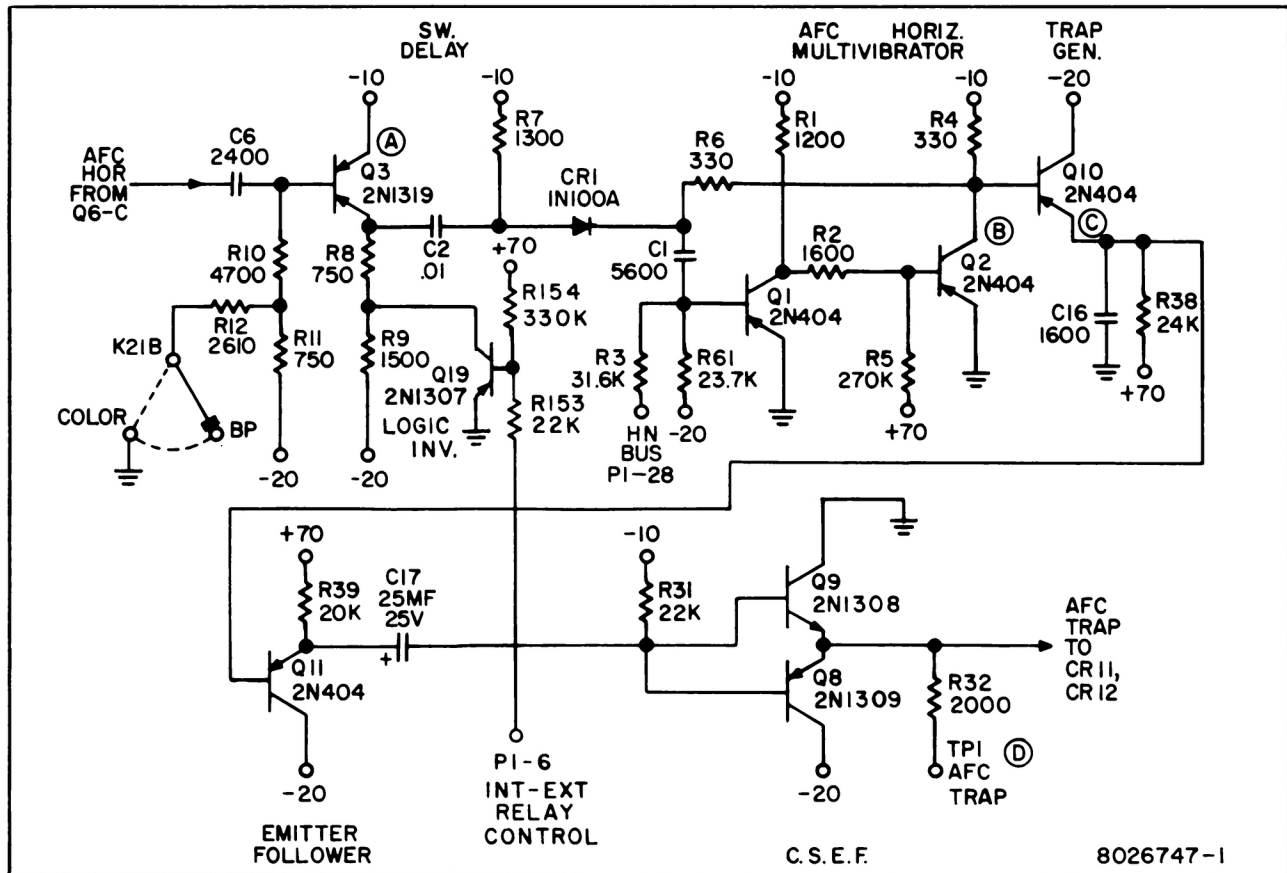


Figure 223—AFC Trapezoid Circuits

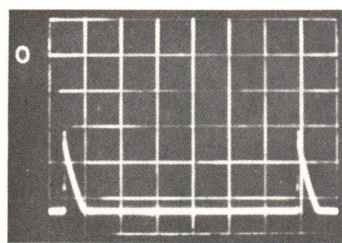
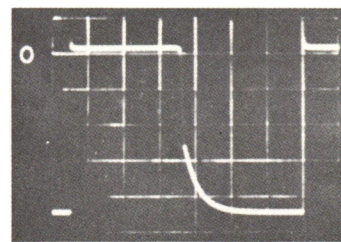
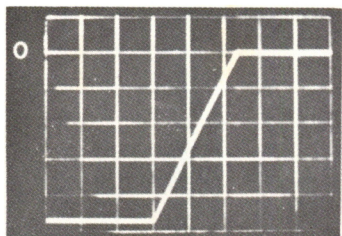
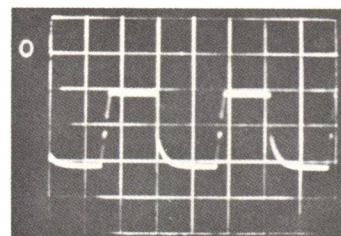
A. Q3 emitter, 10 μ s/cm, 2v/cm.B. Q2 collector, 10 μ s/cm, 2v/cm.C. Q10 emitter, 2 μ s/cm, 2v/cm.D. TP1, 20 μ s/cm, 5v/cm.

Figure 224—Typical Waveforms; AFC Trapezoid Circuits

the charge remains constant. This produces a flat step on the trapezoid slope which coincides with the ATC sample pulse (see figure 222C).

Q12 is an NPN transistor with its base connected to -10 volts and its emitter connected in series with the emitter of multivibrator transistor Q13. When Q13 is cut off its base goes more positive than -10 volts and therefore Q12 is cut off. As soon as Q13 starts to conduct, its base and emitter go slightly more negative than -10 volts. Q12 then conducts and rapidly charges C18 to -10 volts. At the end of one half period of the multivibrator Q13 becomes cut off. Q12 also becomes cut off and C18 starts to discharge, through normally conducting transistor Q5, towards a positive voltage at the junction of R20 and R21 in the emitter circuit of Q5. At some point in this discharge period the 2 microsecond gate pulse from the ATC sample pulse circuits on module 225 is applied through C5 and diode CR2 to the base of Q5. The diode clips the base line of the positive pulse to eliminate crosstalk and noise. The pulse cuts off Q5 and interrupts the discharge path. Since the charge on C18 remains constant during this period, a flat step appears on the trapezoid slope. After the trailing edge of the pulse, the discharging resumes. When the collector of Q12 reaches ground potential diode CR6 conducts and completely discharges C18. Thus the voltage at the collector of Q12 is at a constant level of -10 volts while Q13 is conducting, rises along a positive slope when Q13 starts to conduct, remains constant for 2 microseconds during the gate pulse, and then rises along the slope to ground. Diode CR6 prevents the charging from continuing above ground potential. The voltage remains at ground until Q13 again starts to conduct.

The ATC trapezoid is fed through emitter follower Q4 for isolation and ac coupled through C3 to a dividing network which determines both the amplitude and dc level of the trapezoid. The trapezoid on the emitter of Q4 may be observed at test point TP2 on the front panel (see figure 224D, E). The dividing network contains two potentiometers, R14 (ERROR GAIN) and R60 (TRAP CENT).

The functions of these controls are explained under *General* in this module section.

MAINTENANCE, MODULE 226, BOARD 1

Switched Delay Test

The reference relays K1, K2, and K3, and the switched delay stage, Q3, can be tested as follows:

1. Install a prerecorded tape and place module 226 on an extender.
2. Connect one probe of a dual trace oscilloscope to TP1 (AFC TRAP) on module 226, and the other to TP2 (ATC TRAP).
3. Place the ATC function selector switch on module 223 in the COLOR OFF position.
4. Play back the tape in the tonewheel mode, and observe the dual trace pattern at a horizontal rate. There should be zero delay between the two starting points of the trapezoids, indicating that the ATC system is in the internal mode (see figure 225).
5. Switch the recorder to Pixlock. The delay between the starts of the two trapezoids should change to approximately 6.5 microseconds, indicating that the ATC system has switched to the external mode (figure 226).
6. With the machine in Pixlock, turn the ATC function selector switch to the ATC OFF position. The system should return to the internal mode (figure 225).
7. If the recorder is equipped with color ATC place the ATC function selector in the COLOR ATC position and the TV standards switch on color standards. The delay between the two trapezoids should increase to approximately 11.5 microseconds. Then place the TV standards switch on monochrome standards. The delay should return to approximately 6.5 microseconds.
8. If the recorder is not equipped with color ATC place the function selector in the COLOR OFF position and temporarily ground P1-15 of module 226. The delay should be approximately 11.5 microseconds. Remove the ground. The delay should return to approximately 6.5 microseconds.

NOTE

If the equipment fails the switched delay test check the circuits of reference relays K1, K2, K3 and stage Q3 on module 226, and the ATC function selector switch, S1 on module 223. (Refer to the *System* section for a description of the relay circuits.)

ATC TRAPEZOID CENTERING ADJUSTMENT (R60)

To adjust the centering of the ATC trapezoid proceed as follows:

1. Install a prerecorded tape and place module 226 on an extender.
2. Connect oscilloscope to TP2 (ATC TRAP) on module 226.

3. Place the ATC function selector switch on module 223 in the NORM position.

4. Play back the tape, with the guide servo on automatic.

5. Adjust R60 on module 226 until the step on the ATC trapezoid is approximately 45 percent of the distance from the top of the trapezoid.

6. Turn the function selector to the ATC OFF position. The step should then be approximately in the center of the slope.

MODULE 226, BOARD 2

Board 2 of module 226 contains a clamped sync separator identical to the circuit on board 2 of module 303A, except for the value of resistor R100 in the emitter circuit of Q34, in the video input amplifier circuit (see circuit description in the section on module 303A). On module 226, the value of this resistor was chosen to produce a gain of approximately 2, while in module 303A, the value is selected to produce a gain less than 1. The difference in gain is required because the video input level to the circuit on module

226 is 1 volt, while the input level to the corresponding circuit on module 303A is 2 volts. The symbol numbers of all components on the two circuits are identical. Consequently the schematic diagrams and circuit descriptions given in the section on module 303A also apply to module 226, except for the connections to the input and output of the sync separator.

Video having an input level of approximately 1 volt is fed from relay contact 11K11A in the ATC relay bank, through pin 21 of P1 on module 226 on the input of the sync separator. This video comes from the output of module 303A, in the bypass mode, or module 223, in the internal or external modes of monochrome ATC. In a color ATC system, the video comes from the low pass output of module 325, when the system is in the color ATC mode.

The output of the sync separator goes through pin 29 of P1 in module 229, to relay contact 11K11B. In the bypass mode, this contact is open. In the monochrome or color ATC modes the contact feeds the separated sync to the horizontal AFC module, 227, in the signal processing section and module 325 of the color ATC system.

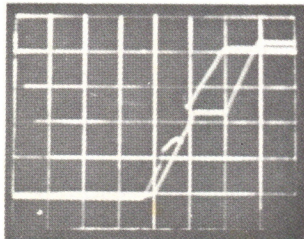


Figure 225—AFC Trapezoid (TP1) and ATC Trapezoid (TP2) in Internal Mode (Zero Switched Delay) $2\mu\text{s}/\text{cm}$, $2\text{v}/\text{cm}$

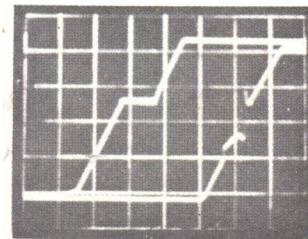


Figure 226—AFC Trapezoid (TP1) and ATC Trapezoid (TP2) in External Mode (Approx. $7\mu\text{s}$ Switched Delay) $2\mu\text{s}/\text{cm}$, $2\text{v}/\text{cm}$